ESCUELA TÉCNICA SUPERIOR DE INGENIERÍA (ICAI)

GRADO EN INGENIERÍA ELECTROMECÁNICA

ESPECIALIDAD ELÉCTRICA

DESIGN AND CONSTRUCTION OF AN ISOLATED DC-DC FLYBACK CONVERTER FOR SOLAR MPPT PURPOSES

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Madrid

Julio 2018

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DESIGN AND CONSTRUCTION OF AN ISOLATED DC-DC FLYBACK CONVERTER FOR SOLAR MPPT PURPOSES

Director: Professor Arijit Banerjee from University of Illinois at Urbana-Champaign.

Author: Daniel Portillo Quesada.

SUMMARY

Introduction

Nowadays, solar power generation is gaining more and more importance in terms of participation of the energy mix of countries all around the world. Despite being a sustainable and renewable source of energy, it is not growing at its maximum pace. This is caused by the problem of efficiency; solar panels have a very low efficiency which makes this kind of generation more expensive than other sources (in addition with high manufacturing costs). However, each year innovative technologies rise to higher than efficiency or to make solar panel costs cheaper making solar power more feasible to invest in so as to swap the energy mix towards a greener one reducing greenhouse effect gasses emissions.

One key component of solar panels that makes them suitable for grid implementation and plays a very important role in efficiency performance, is the power electronics present in solar systems. Not only in terms of losses management but also with control techniques, this technology can make those panels extract more energy from solar irradiance as we are going to address in this project. There are so many options speaking of types of converters to harvest solar energy but the one found to be specially interesting for this application is the DC-DC flyback converter as its unique features satisfy some shortcomings of those solar panels.

Objectives

The main goal of this project is to address effectively the efficiency and performance issues explained in the introduction. The project will be an important part of a more ambitious one as it complements the effort of two other students designing an entire solar power system with a DC-DC converter (this project), a DC-AC converter and a storage system to address the intermittency characteristic of renewable resources.

The flyback converter will be attached directly to the solar panel managing its operation as it can control the characteristic I-V curve of solar panels to extract the most quantity of power possible. This converter is crucial in the solar system designed as it improves the efficiency but also because it will be controlling the voltage in the DC bus which is the common point with which every part of the system will be working.

Speaking more specifically of my project with the flyback converter as the main character, throughout this thesis we will be addressing the electric and electronic features of this power electronics element. Due to constraints regarding time and budget, the control part of this project could not be addressed, and it is delegated to future students willing to fulfill the objective of the whole project as it can work on the flyback converter control but also with the

control ruling the interconnection of the three systems present in the solar power system project.

Methodology

Firstly, we conducted an exhaustive research to find out which was the best option to solve the efficiency issue in solar panels. After choosing the flyback converter due to its reduced losses features and voltage transformation capability, we started the simulation analysis to better understand its operation and how it can fit in the solar power systems. Once the nature of the converter is fully understood, we started to analyze the equations ruling the functioning so as to address the components design.

Secondly, reaching that components design phase, some focus in core components was needed. We decided to start sizing the characteristic transformer of this type of converter as it would fix the voltage level of the DC bus needed to calculate the parameters of the other components. Following, we decided which active component we will be using (MOSFET), and last, we chose the passive components that would complete the proper operation of the device.

Thirdly, we started to build the prototype of the converter in protoboards taking the components from the University depot and from external suppliers. The converter was tested in a low charge point of operation for security reasons. It fulfilled the expectations held but it did not achieve a perfect performance as efficiency could be improved with better quality and customized components. This is another task that can be attained also by future students as time did not run in our favor.

Lastly, the results were presented to our project advisor to show the progress and receive approval for the project closure.

Results

As shown in the correspondent part of the thesis, the results were satisfactory as the converter could increase the voltage levels to reasonable values changing the duty ratio of the converter. With a turns ratio of 1:20 in the transformer present in the converter and an input voltage of 1.5 Volts DC, we obtained a 20 Volts DC signal steady enough.

To make the test, we used a resistor in order to avoid failures in the other converters made by my partners. This means that as we increased the duty ratio, the voltage level increased too and so the power did. With that we know that it can perform well with solar panels in terms of efficiency improvement, but we chose not to test the converter with real solar panels due to safety reasons. Solar panels produce a specific current with a specific irradiance so if we made a mistake we could have burned the circuitry.

Overall, we saw that the converter performed well enough to be a first prototype, but it produced a lower voltage than expected (due to efficiency issues) so some improvements can be implemented.

Conclusion

To sum up, the project demonstrated the premises we thought while conducting the research. This type of converter can increase the voltage to grid levels making it suitable for some solar system configurations as explained in this project (it focuses specifically on microinverters).

This type of converter could end up being an innovative way to improve solar power efficiency making utilities produce more energy. This would result in an increase of solar energy generation as it would be feasible to invest in. It also improves safety for workers (galvanic isolation) and its implementation could result in money saved as it reduces maintenance costs.

DISEÑO Y CONSTRUCCIÓN DE UN CONVERTIDOR DC-DC AISLADO "FLYBACK" PARA TÉCNICAS DE MÁXIMA EXTRACCIÓN DE POTENCIA EN PANELES SOLARES

Director: Profesor Arijit Banerjee de la University of Illinois at Urbana-Champaign.

Autor: Daniel Portillo Quesada.

RESUMEN

Introducción

Hoy en día, la energía solar está ganando más y más importancia en cuestión de participación en el mix de energía de muchos países alrededor de todo el mundo. Aun siendo una fuente de energía sostenible y renovable, no está creciendo al ritmo que podría. Esto es causado por el problema de la eficiencia, los paneles solares tienen una muy baja eficiencia haciendo que este tipo de generación sea más cara que otras fuentes de energía (añadido a los altos costes de producción de paneles). Sin embargo, cada año aparecen nuevas tecnologías y materiales para mejorar la eficiencia de estos paneles o para hacerlos más económicos consiguiendo que la energía solar sea más factible para invertir en ella. Esto lograría mover el mix de energía hacia uno más verde reduciendo la emisión de gases de efecto invernadero.

Uno de los componentes clave de los paneles solares que los hacen adecuados para la conexión a la red y a la vez juega un rol importante en la mejora de eficiencia es la electrónica de potencia presente en estos sistemas de energía solar. No solo en temas de manejo de pérdidas sino también con técnicas de control, esta tecnología puede hacer que los paneles solares extraigan más energía de la irradiación solar tal y como vamos a abordar en este proyecto. Hay muchas opciones hablando de tipos de convertidores para extraer energía solar pero el que hemos encontrado especialmente interesante para esta aplicación es el convertidor "flyback" ya que sus características únicas satisfacen algunas carencias de los paneles solares.

Objetivos

El principal objetivo de este proyecto es abordar de manera efectiva la eficiencia y problemas de funcionamiento explicados en la introducción. El proyecto va a ser una parte importante de uno más ambicioso ya que complementa el trabajo de otros dos estudiantes diseñando un sistema solar completo con un convertidor DC-DC (este proyecto), un convertidor DC-AC y un sistema de almacenamiento de energía para solucionar el problema de la intermitencia característica de las fuentes de energía renovables.

El convertidor "flyback" será conectado directamente al panel solar controlando su operación debido a que controla la curva I-V característica de los paneles solares para extraer la máxima energía posible. Este convertidor es crucial en el sistema de energía solar diseñada debido a que mejora la eficiencia, pero también porque estará controlando la tensión en el bus de continua, el punto común de todas y cada una de las partes que componen el sistema.

Hablando más específicamente de mi proyecto con el convertidor "flyback" como el protagonista, a lo largo de esta tesis abordaremos y trataremos con la parte eléctrica y

electrónica de este dispositivo de electrónica de potencia. Debido a limitaciones en tiempo y presupuesto de nuestro sistema, el control del sistema no podrá ser estudiado y se deja este trabajo a futuros estudiantes con la voluntad de conseguir el objetivo del sistema completo ya que puede controlar el convertidor “flyback” pero también la interconexión de todos los subsistemas presentes en el proyecto del sistema de generación solar.

Metodología

Primero, llevamos a cabo un análisis exhaustivo para ver cuál era la mejor opción en términos de tipo de convertidor para resolver los problemas de ineficiencia en paneles solares. Después de escoger el convertidor “flyback” por sus reducidas pérdidas y su capacidad de transformar la tensión, empezamos la simulación para entender mejor su operación y cómo podría encajar en sistemas de energía solar. Una vez la naturaleza del convertidor fue totalmente comprendida, empezamos a analizar las ecuaciones que rigen el funcionamiento con motivo de abordar el diseño de componentes.

Segundo, alcanzando esta fase de diseño de componentes, era necesario hacer énfasis en los componentes centrales. Decidimos empezar a diseñar el transformador característico de este convertidor ya que esto fijaría la tensión del bus de continua necesario para el cálculo de otros componentes. A continuación, decidimos qué componente activo usaríamos (MOSFET) y, por último, escogimos los valores de los componentes pasivos que completarían la correcta operación del convertidor.

Tercero, empezamos el montaje del prototipo del convertidor en una protoboard escogiendo los componentes del almacén de la Universidad, pero también de proveedores externos. Este convertidor fue probado en un punto de operación de baja carga por motivos de seguridad. Este test cumplió las expectativas que se tenían previamente pero no consiguió un perfecto funcionamiento ya que la eficiencia podía ser mejorada con componentes de mayor calidad o personalizados para nuestro proyecto en específico. Esta también es una tarea pendiente que puede ser llevada a cabo por futuros estudiantes debido a que el tiempo no corría a nuestro favor.

Por último, los resultados fueron presentados al director del proyecto para enseñar el progreso y recibir la aprobación para concluir el proyecto.

Resultados

Como se muestra en la correspondiente parte de la tesis, los resultados fueron satisfactorios ya que el convertidor pudo incrementar el valor de la tensión de salida con valores razonables cambiando el “duty ratio” del convertidor. Con una relación de transformación de 1:20 en el transformador y una tensión de entrada de 1,5 Voltios de corriente continua, obtuvimos 20 Voltios de corriente continua suficientemente constante.

Para hacer la prueba, usamos una resistencia arrollada al convertidor para evitar fallos en caso de interconectar otros convertidores de compañeros. Esto significa que al aumentar el “duty ratio” se aumentaba la tensión y con ello la potencia disipada en la resistencia. Con esto sabemos que puede operar bien con paneles solares en términos de mejora de eficiencia, pero decidimos no probar el convertidor con paneles solares reales por motivos de seguridad. Los paneles solares producen una corriente específica con una irradiación dada y por ello si se cometiese un fallo, se podrían quemar los circuitos.

Resumiendo, vimos que el convertidor funcionó suficientemente bien para ser un primer prototipo, pero produjo un voltaje menor al esperado (por problemas de eficiencia) y por ello las mejoras mencionadas previamente podrían ser implementadas.

Conclusión

En resumidas cuentas, el proyecto demostró las premisas que se nos vinieron en mente mientras que desarrollábamos el proyecto. Este tipo de convertidor puede aumentar el voltaje hasta niveles de la red haciéndolo deseable para algunas configuraciones en sistemas de energía solar como se explica a lo largo del proyecto (se centra específicamente en microinversores).

Este tipo de convertidor podría acabar siendo una manera innovativa de mejorar la eficiencia en generación de energía solar haciendo que las compañías de generación produzcan una mayor cantidad de energía. Esto resultaría en un mayor incremento en generación solar ya que sería más factible su extracción. El convertidor también mejora la seguridad para operarios (aislamiento galvánico) y su implementación podría resultar en un ahorro económico ya que también reduce costes de mantenimiento.

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Abstract

The project will consist on the design and building of a DC-DC Flyback converter to increase efficiency in solar panels by tracking the maximum power point given a specific insolation and solar panel temperature. This subsystem, in addition to two othes designed by two other students, will represent the functioning of a solar facility with storage and an inverter to connect the panel to the grid. The DC-DC converter project will involve the study, construction, and results analysis of the electrical part (circuitry and magnetic components) excluding the control of the converter. This work can be carried by another student in future year. The project will include a brief explanation of the background where is located the desired converter, component calculation, simulation, and result analysis from the real circuit constructed.

Subject Keywords: DC-DC, converter, MPPT, solar systems, solar PV.

To my beloved ones.

Without them I would not be the person I am today. They are the reason why I managed to walk this difficult road. This thesis would have never been finished without your support.

I would also like to thank my laboratory partners and friends Juan Carlos Martin Valiño and Alberto González Ortega for being there at every moment helping us all to accomplish this project.

Special thanks to Professor Arijit Banerjee and Kevin Colravy for their invaluable help and effort they have put to make this project work.

Contents

1. Introduction

1.1. Statement of purpose

Now days, we are witnessing a big transition from fossil fuel energy generation towards a greener and more sustainable one involving resources such as wind or solar light. These cleaner energy resources present undeniable benefits like the low cost of operation (free fuel), their module feature giving the possibility to increase capacity easily, or the fact that they are carbon-free power generation resources.

Climate change and global warming are threats that have entered the global scene in the last decade in terms of energy production. Our world is sustained by traditional means of energy production involving fuel burning such as carbon, oil or natural gas, which have produced an appreciable increase of global temperature leading to events such as natural life extinction or ice melting in the poles. Scientists noticing those changes in our world have raised awareness of the current situation, encouraging governments and companies to boost other ways to supply energy conserving the environment.

Efficiency is a key point to address so as to make sustainable resources suitable to invest in and develop to produce energy. This is the main objective of this project: approach the photovoltaic power generation to give a different way of power extraction optimization in solar panels. Maximum Power Point Tracking (MTTP) technology is already implemented in utility-scale facilities but also in behind-the-meter grid-connected systems supplying energy to the customer's side of the meter. This shows that DC-DC conversion in solar power has become important for efficient and economical energy generation, because one can harness the maximum solar power possible at every moment, increasing profits and sustainability.

This project, as a part of a bigger one, also tries to address the storage issue that is preventing renewable generation to fully substitute fossil fuel energy production. One of the main problems for renewable

generation is the variability in the resources from which energy is harvested. A system able to redistribute energy delivery to the grid during peak demand hours would be very advantageous in terms of economics due to the time-of-use rates applied, because the facility could deliver the energy during peak demand periods when energy price is higher; it would be also favorable to meet the demand at every time, storing energy at low demand periods and releasing it in the opposing case, making it possible to lower frequency restoration techniques applied to fossil fuels.

These issues encouraged me, and the other two students involved in the solar facility project, to conduct this project. I found attractive the subsystem that I am in charge in particular since flyback converters are used in appliances or electronic devices. They have a great potential in other fields such as solar power… it has several advantages, which are presented next.

This project will involve the design and construction of a DC-DC flyback converter aimed to be used in maximum power point tracking (MPPT) techniques so as to extract maximum power from a solar panel given specific conditions of operation. I will be in charge of the electrical part regarding the circuit design and hardware construction, but regrettably I will not be working on the control system ruling the converter to meet the maximum power point (MPP) automatically due to the limited time and the fact that the control would require a lot of time and effort to develop, as I am a power engineer with less knowledge in that field. This project also aims to give purpose to this subsystem, being a part of a bigger generation system, but we will not be implementing a control for the whole system making, each subsystem interact with each other in multiple conditions of operation (i.e. irradiance, demand, or storage charge levels). Those control systems could be studied and developed by future students with enough ambition and concern to achieve that difficult and demanding task.

1.2. Project scheme

Figure 1 shows a global scheme of the entire solar system project, and highlighted in red the main scope for this project in particular:

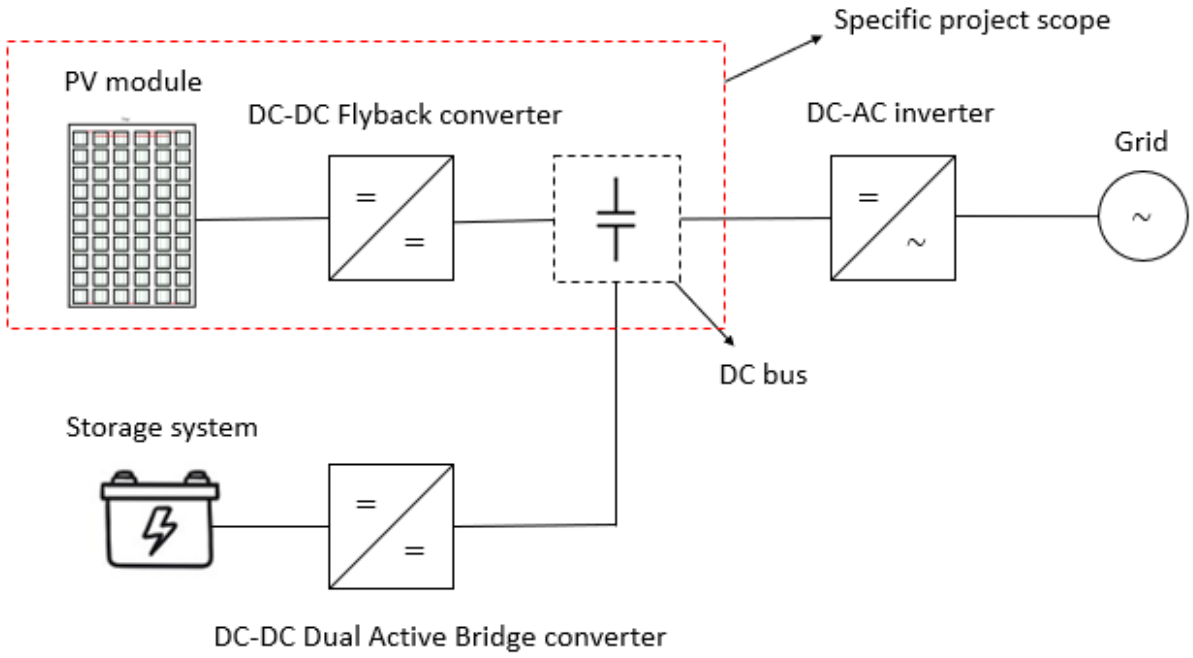

Fig. 1. Entire system diagram.

1.3. Goals and benefits

There are some main objectives and benefits to this project:

- Optimization of power generation in PV systems.
- Stability in operation when suffering big irradiance changes.
- Adjustment of the turns ratio allow to have every possible output voltage no matter what the input voltage is.
    - The utility can save money that would be spent in a big and expensive transformer placed in the output of the inverter in order to higher the voltage to AC-grid levels.

    - The converter chosen is suitable for the rising trend of microinverters (explained in next sections).
- Galvanic isolation between the PV panel and the AC-grid.
    - This will produce the disappearance of common mode currents. [1].
- Safer for workers to manipulate the panel in maintenance periods for instance.
- Possibility to operate as a buck-boost converter with a wider range of voltages in a lower duty ratio operation, due to the transformer's presence.
- Bring new points of view of configurations in DC-DC MPPT converters to keep the good work on reducing the human carbon footprint.

2. State of the art

2.1. Principles of solar energy extraction

To understand the actual technology regarding solar power generation, we must first understand to its principles. Solar panels generate energy producing DC current and voltage; this phenomenon happens due to the most basic structure that drives the process of energy extraction. As kidneys have nephrons as their functional unit, solar panels have the p-n junction as the simplest structure driving the process of solar light harnessing. The most used semiconductor in solar cells is silicon. It is composed of two parts; the upper part is made of type n doped silicon. This means that it has more free electrons than normal silicon. The lower part is made of p-type doped silicon, which has less free electrons than the pure silicon. When coupling those two parts, free electrons in the n layer enter the vacancies present in the p layer. They create a potential difference that remains like that the whole life of the cell. Figure 2 extracted from [2] shows that phenomenon.

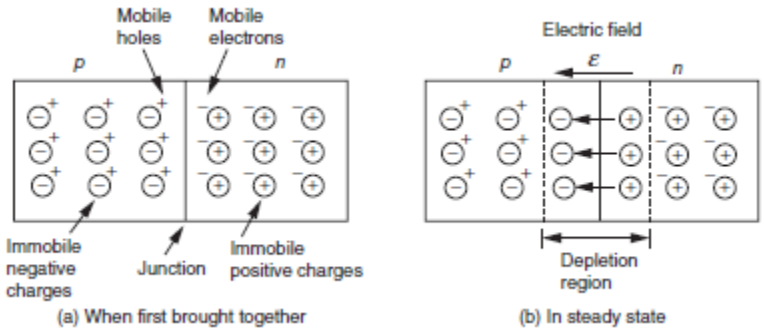

Fig. 2. Phenomenon occurring when coupling the p-n junction [2].

The electric field created when coupling the junction makes the intermediate zone become a diode, allowing only the flow of electrons from the region p to region n. That changes when photons hit the solar cell and extract electrons from the matrix, as the opposite event happens, electrons stacks in the n region (becoming a negative pole) while vacancies appear in the p region (creating a positive pole). At that point, one can connect a light bulb to the cell for instance and make it work like a power source. This is more

effective near the depletion region, which is very thin, and because of that solar cells are built very thin. In other words, a solar cell is an energy generator with a diode inside.

It is obvious that solar cells themselves cannot supply a considerable amount of energy as they are very small. To generate a more reasonable amount of power, these solar cells are grouped in modules and those modules in arrays as shown in Figure 3.

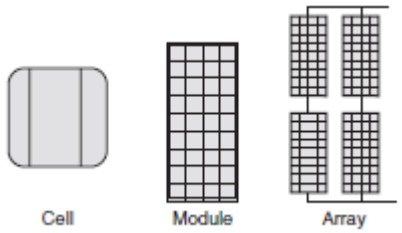

Fig. 3. Photovoltaic cells, modules, and arrays [2].

Solar modules, as a combination of photovoltaic cells, are ruled by the characteristic I-V curve. That means that given a specific irradiance and panel temperature, the module works with a specific curve showing the current it supplies depending on the voltage in its terminals. MPPT technology harnesses that characteristic by changing the equivalent impedance seen by the panel and with that, move the point of operation of the I-V curve. In the end, as Ohm's law states, $R = \frac{V}{I}$ so changing that resistance value we can obtain different values of voltage and current.

Figure 4 can be an example of I-V curve for a 100 W PV panel:

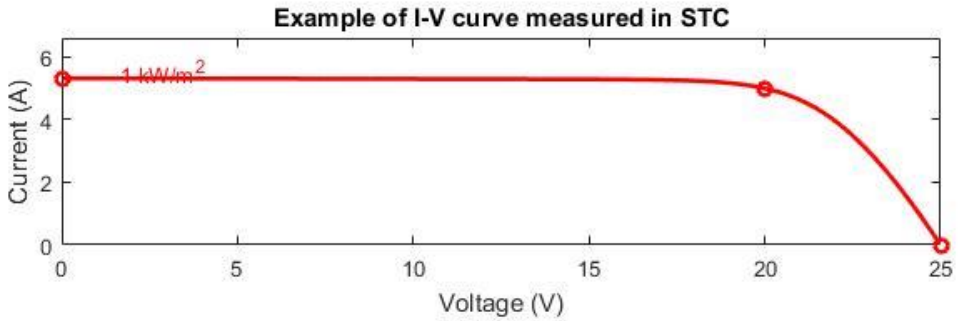

Fig. 4. I-V curve for a generic solar panel in STC.

This theoretical curve is measured under standard test conditions (STC), which means that the measurements were taken with the solar panel at 25 ℃ and receiving 1 kW/m^2. The readings that can be extracted from that curve in Figure 4 regarding the consequences of changing the equivalent impedance connected to the panel are the following:

$$Open - circuit \rightarrow R_{eq} = \infty \rightarrow V = V_{oc} = 25\,V\ ;\ I = 0\,A \rightarrow P = 0\,W$$

$$Short - circuit \rightarrow R_{eq} = 0\,\Omega \rightarrow V = 0\ V\ ;\ I = I_{sc} = 5.3\,A \rightarrow P = 0\,W$$

$$MPP \rightarrow \begin{cases} V_{MPP} = 20\,V \\ I_{MPP} = 5\,A \end{cases} \rightarrow R_{eq} = \frac{20}{5} = 4\,\Omega \rightarrow P_{MPP} = 100\,W$$

These readings shows the potential that a MPPT has in terms of optimization of power generation in solar panels. Changing the equivalent resistance in every moment, given any operating conditions gives an extraordinary advantage in terms of efficiency. This will be addressed later in the next section.

Another feature regarding the I-V curve of the panels is that it changes with the irradiance and with the panel temperature. The more irradiance the panel receives, the grater it will be the current and voltage generated by the panel. With temperature, the opposite will happen but only with voltage. The higher the temperature of the panel, the lower the voltage the panel is able to give. This is shown in Figure 5:

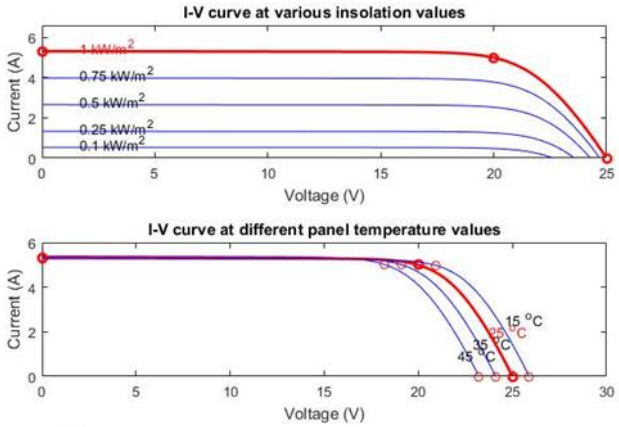

Fig. 5. I-V curves changing panel temperature or irradiance and maintaining the other parameter constant.

Last, we have the array structure characteristic feature. It is related to the positioning of modules that form that array. The arrangement of modules in an array is not arbitrary as depending on how modules are connected, the output of the array will change. Connecting modules in series make the voltage of the output be the sum of voltages of the modules and when connecting them in parallel, the current is the one summing in this case. One can control the expected output of the array by making a configuration of modules in series and in parallel as both strategies can be mixed. Figure 6 shows how the I-V curves change depending on the connection of the arrays.

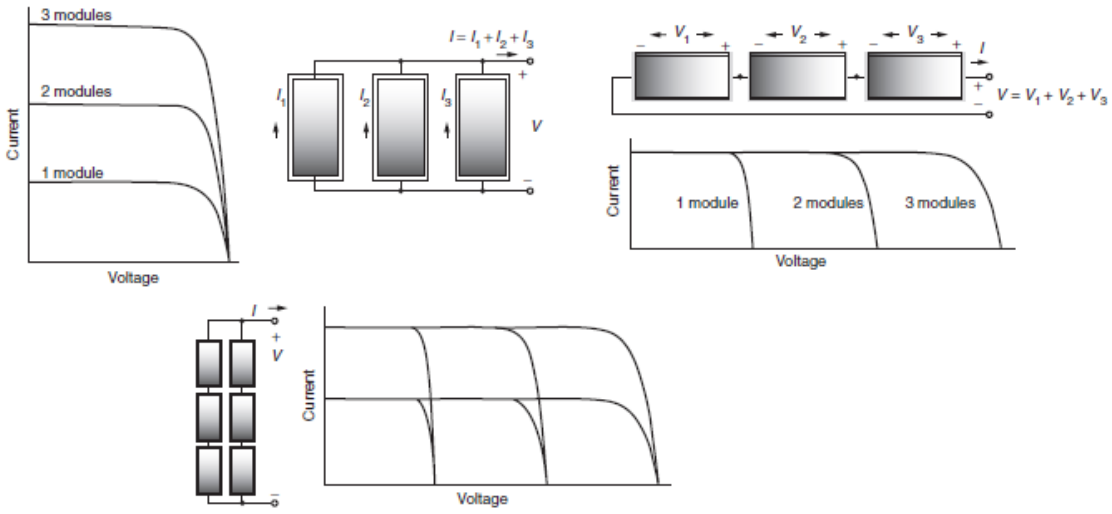

Fig. 6. In-series, parallel and mixed configuration of modules with their equivalent I-V curves [2].

Figure 6 shows how the parameters are stacked depending on the arrangement chosen for the array. This feature is very important in solar facilities design because depending on how the connection of the modules is, or to say in other words, how arrays will be, the power conditioning unit (PCU) that is composed by the DC-DC converter plus the inverter will need to have different characteristics. That PCU is the component driving the maximum power point tracking technique addressed in this project.

2.2. MPPT DC-DC converters today

The heart of those MPPT controllers is indeed DC-DC converters, which are quite simple circuits capable of higher or lower the voltage supplied by the solar panel. That task was very difficult to execute before the creation of high-power, field-effect transistors (FETs) in the 1980s and insulated-gate bipolar transistors (IGBTs) in the 1990s. Those transistors make it possible to change the output voltage by controlling the duty ratio of the switch. Most common DC-DC converters are the buck and the boost converter. A buck converter operates to lower the voltage with respect the input and boost converter does the opposite task. These are simple representations of those converters:

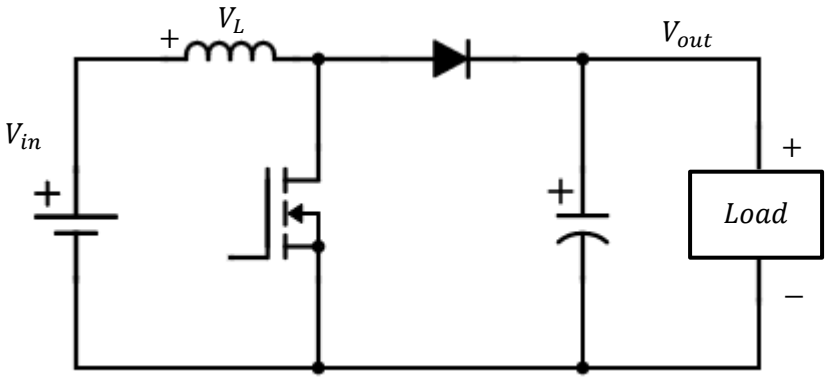

Fig. 7. Design of a boost converter.

Figure 7 represents the circuit of a boost converter. It has a MOSFET transistor as mentioned before. That transistor will be the one regulating how much we want the output current to be higher. The transfer function of this specific converter shown in Equation 2.1:

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{2.1}$$

With D being the duty ratio that we are applying to the transistor. It can take values from 0 to 1, which will alter the time the diode is turned on. Watching that transfer function, we can deduce that the higher the duty ratio, the higher our voltage will be.

Figure 8 shows the circuit design for a buck converter.

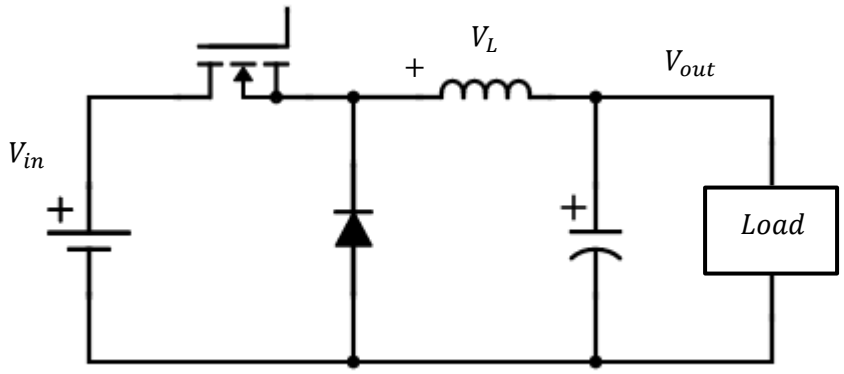

Fig. 8. Design of a buck converter.

In this case the transfer function relating the output with the input is given by Equation 2.2:

$$\frac{V_{out}}{V_{in}} = D \tag{2.2}$$

Noticing that D can take values from 0 to 1, starting in the maximum value where the input is equal to the output, as soon as we reduce that duty ratio, the output voltage will drop to the point it can be zero.

These two converters are the simplest ones as they are only able to higher or lower the voltage separately, none of both converters can do those two tasks together. This is a constraint when implementing them in solar MPPT controlling because a solar array can have a wide variety of input voltages depending on its arrangement or even the light and panel conditions. For that reason, the most frequently and more popular used converter is the buck-boost. As its name hints, that DC-DC converter is able to higher and lower the output voltage with respect the input one.

The design for a buck-boost converter is represented in Figure 9:

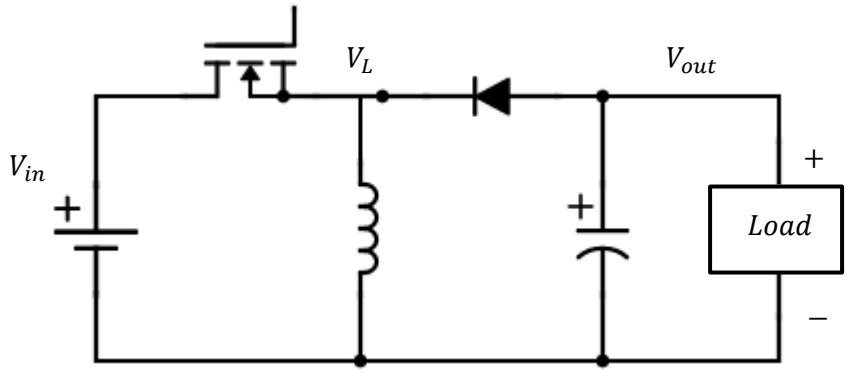

Fig. 9. Design of a buck-boost converter.

This design is still very simple, having the same components, but it has a larger range of operation. We will fully derive the expression of this converter, but in the end, this work could be applied to the other two DC-DC converters showed in Figures 7 and 8. The only consideration we have to take into account is that average voltage in an inductor in the periodic steady state is zero. With that in mind, we proceed to make the calculations:

$$When\ FET\ is\ ON \rightarrow V_L = V_{in}$$

$$When\ FET\ is\ OFF \rightarrow V_L = V_{out}$$

Then:

$$\langle v_L \rangle = V_{in} \cdot D + V_{out} \cdot (1 - D) = 0;\ \frac{V_{out}}{V_{in}} = -\frac{D}{(1 - D)} \tag{2.3}$$

The negative sign only indicates that the polarity in the output is reversed. With the rest of the expression we can notice that now this converter can operate increasing and decreasing the voltage.

$$D = 0 \rightarrow \frac{V_{out}}{V_{in}} = 0$$

$$D = 1 \rightarrow \frac{V_{out}}{V_{in}} = -\infty$$

$$D = 0.5 \rightarrow V_{out} = -V_{in}$$

When we increase the duty ratio, the output voltage increases (with negative sign) noting that with a duty ratio of 0.5 the value of the voltage in the input is the same as in the output (with different polarity).

Any kind of DC-DC controller modifying the output voltage can be used as an MPPT. The principle is simple, modify the duty ratio so as to change the equivalent impedance connected to the solar panel and with that, force the panel to supply its maximum possible power. To analyze the power extracted from a solar panel we can study its P-V curve. It is basically extracted by remaining the abscises axis the same and then multiple values of current and voltage in the I-V curve to obtain the ordinates axis representing the power extracted. Those curves have the shape showed in Figure 10:

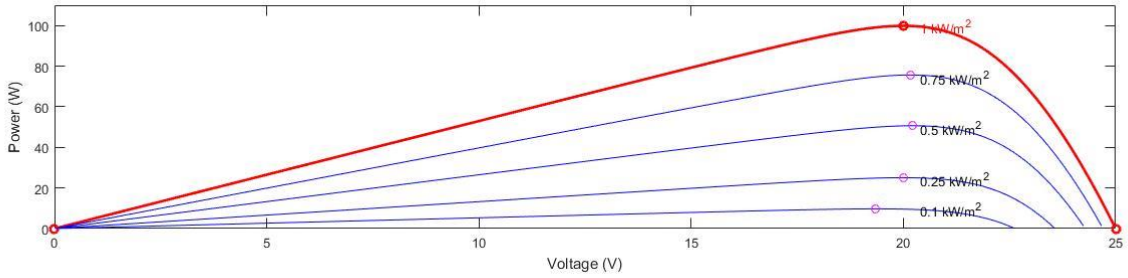

Fig. 10. Example of P-V curve at different value of irradiance.

Figure 10 gives an example of different MPP depending on the irradiance received by the panel at a constant temperature. If temperature increases, the maximum power extracted would decrease with the MPP voltage doing the same. In the case of different irradiance, we do not have a simple tendency like with temperature. When decreasing the irradiance receiving, it is obvious that we will extract less power, but the MPP voltage will follow a parabolic shape finding its maximum voltage value when we reach an irradiance value of 0.5 kW/m^2.

2.3. Alternative solutions for solar MPPT

In the last decade, a different way of MPPT technology has become trendier and it is increasing its use in solar power facilities all over the world. This is the case of the microinverters. Conventionally, solar modules were connected with different configurations forming arrays with the characteristics explained above. Microinverter technology focuses on using a power conversion unit with less rated power in each module trying to increase efficiency to the maximum. Each panel has its own inverter meaning that the operation of one module will not condition the power extracted from other, in addition, the inverter would have to work with a lower input voltage and current stress. Microinverters give an exceptional solution for panel shading as they extract power from each module separately. First, let us see which are the conventional solutions that we can avoid by using this alternative MPPT technology. The first one is depicted in Figure 11:

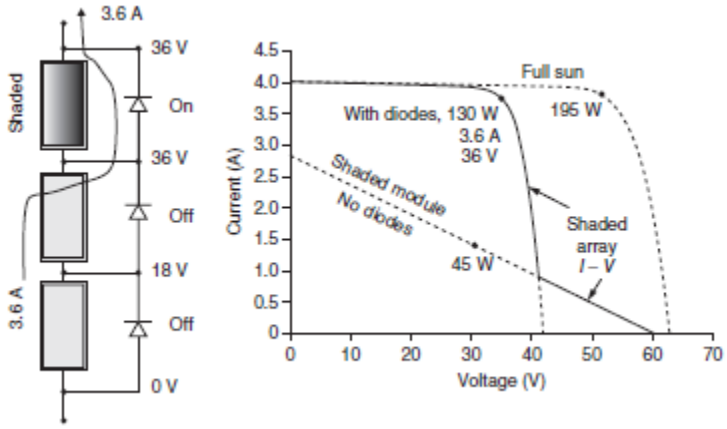

Fig. 11. Capability of bypass diodes to mitigate panel shading [2].

The module shading happens because of a cloud passing above the panel or dust retained in the surface of the panel having consequences in the array operation. As modules in series share the same current flowing through them, when a module is shaded, it will not produce energy operating as a short-circuit. This would prevent the modules in series with him to produce energy as the current cannot flow in that branch. This problem is solved using bypass diodes. Those diodes are connected in parallel with each panel giving a secondary path for the current when a module is blocking the current.

Another problem solved using microinverters is the presence of reverse current as a consequence of defective or shaded panels in one branch. If an array suffers from reverse current, this means that current generated by other modules is not going to the converter but to another branch of the array. This is usually solved using blocking diodes that would prevent the current from flowing in that direction maintaining the current in a zero value. The second example of alternatives for panel shading is given by Figure 12.

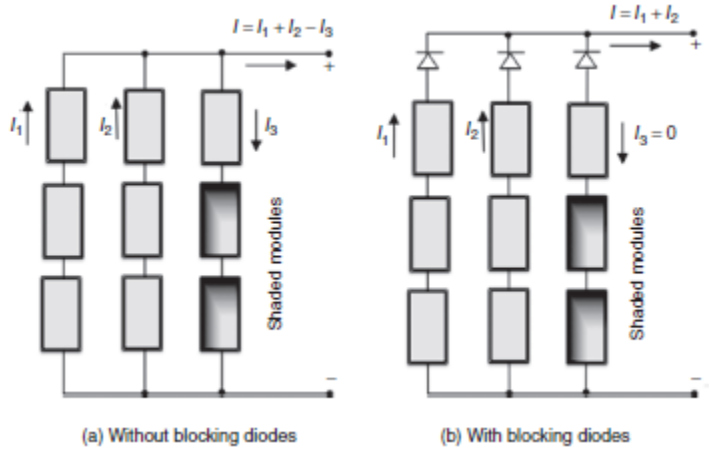

Fig. 12. Potential of using blocking diodes in every branch of an array [2].

For these two examples where the panel shading affects the operation of a solar array, we can understand the impact of solving those issues by using microinverters instead of conventional PCUs. Adding diodes to the arrays increases the probability of component failure as we have implemented another element susceptible of breaking in the medium/long term.

Microinverters have a big importance in this project as flyback converters fit perfectly in the operation conditions of those microinverters. Flyback converters are suitable to be used in devices of around 200 Watts and because of that they are used in electronic devices (i.e. phone chargers or power supply in PCs) but have a big potential in solar energy applications. As microinverters work with modules separately, our type of converter is perfect managing with low power input. It has also the advantage of modules alone not supplying high voltages so when trying to equalize the output voltage of the inverter to the grid voltage, the Flyback converter can easily complete that task without high duty ratios in the transistors thanks to its transformer, that gives more margin of operation for our converter.

The schematics shown in Figure 13 give us an example of how a central inverter arrangement looks, in comparison with a microinverter.

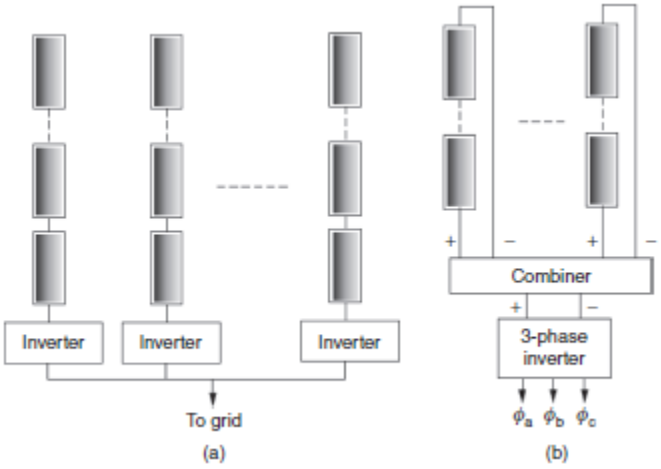

Fig. 13. Comparison between microinverters and central inverters in solar power systems [2].

In the case of extracting solar energy in behind-the-meter systems such as domestic or business applications, it makes more sense to implement those microinverters. In solar energy extraction for subsistence purposes, the output power is not as high as in utility-scale facilities due to the smaller size of the panels used. It is not the same using panels in deserts than in the rooftop of your company, here the space availability comes to play. When trying to obtain energy to supply your daily need, you need those panels to be the most efficient as possible because the place you are living may not be ideal in terms of solar irradiance.

Speaking with numbers, microinverters give a lot of advantages in comparison with central inverters which are the conventional mean of power conversion regarding solar energy extraction. Due to the reasons explained above of microinverters avoiding the usage of diodes (bypass or blocking), they can higher the power output from 5% to 25% meaning a great increase in efficiency and savings for homeowners or big energy sellers. To give an example of why this happens, shading only a 9% of a solar system with a central

inverter can lead to a decrease in the energy output of at most 54%. This is a huge power loss showing why microinverters are gaining market power in these last years.

In terms of costs, it is logical to think that microinverters are more expensive because you have to use more of them depending on the number of modules you are operating with. In average, central inverters cost around $0.40/W-p (dollars per W-peak) while microinverters cost more or less $0.52/W-p. This information does not mean that inverters are overall more expensive. We have to take into account the warranty of each inverter and the installation costs. In terms of the warranty, microinverters are much better because as they deal with less power, they suffer less stress during its operation lasting for around 20 to 25 years while central inverters last for 10 to 15 years meaning that they will have to be replaced more frequently increasing costs. Addressing the installation costs, microinverters are simpler and less time-consuming cutting installation costs by a 15% more or less. These figures show the tremendous advantages of microinverters in comparison with conventional central inverters.

To reduce the initial cost of the microinverters, since 2011 dual-microinverters have been released to the market. Its functioning is as simple as their name indicate, they do the same things as microinverters but with two modules. This reduces the initial costs but sacrificing performance. These kind of microinverters are suitable depending on the type of solar system as in some cases they should be taken into consideration.

More additional advantages of microinverters could be the increased safety they give because they operate with single modules with lower voltage in their terminals. Besides, owing to the fact that they operate at lower output power, they will dissipate less heat meaning that they do not need ventilation systems to cool down the components. That will result in a suppression of noise in their operation. One last important feature they give is their ease to expand the solar systems, as they are managing modules separately you can add capacity to your system by adding new module-microinverter units.

2.4. Solar MPPT control techniques

As said in the introduction, this project will not cover the control programming and implementation to drive nor the subsystem nor the whole interconnected system. However, it is important to address the most common MPPT control techniques to help future students executing that task when seeking for information in this project.

In solar applications, MPPT controllers work all with the same reading procedure but they differ from each other in the algorithm that they follow in order to attain the MPP. Every DC-DC converter with MPPT has sensors in the terminals of the module or array reading the value of the voltage and current. When obtaining those values, they enter in the algorithm giving a command that will change the duty ratio of the converter trying to move the point of operation towards the MPP. Next, those different algorithms making each type of control unique learned from [3] will be addressed. Figure 14 shows how these control systems work.

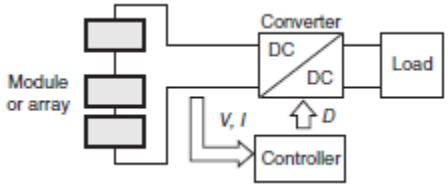

Fig. 14. Basis of an MPPT controller for solar power systems [2].

First, a very simple and straightforward method called “Perturb and observe” or “Hill climbing” is introduced. That consists on making small changes in the duty ratio and see if the power obtained is higher or not. If the move made the power decrease, then the duty ratio will be changed in opposition to the previous iteration. This method is commonly used because of its ease of programming and implementation but its disadvantage is that it will produce oscillations in the output power as it is always changing to verify that the panel is operating at the MPP. The logic algorithm of “Hill Climbing” is represented in Figure 15.

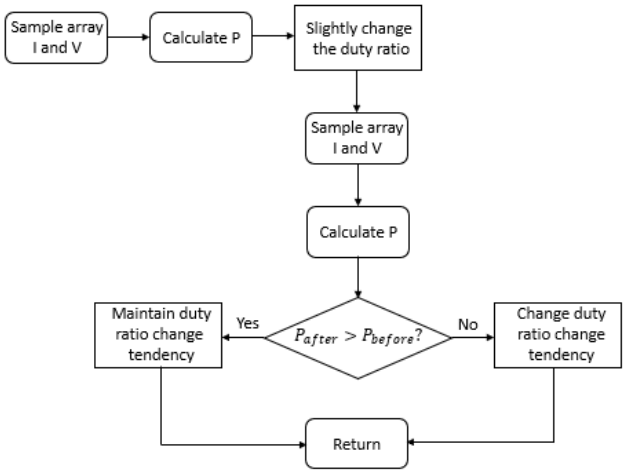

Fig. 15. Algorithm for Perturb and observe control technique.

The next control technique important to mention is called “Constant voltage” but some authors call it the “Open voltage” technique due to its nature. In this type of control, the controller first changes the duty ratio to obtain a very high equivalent impedance (with a duty ratio value of zero) and then it measures the open-circuit voltage value of the module. After this, the duty ratio is changed to obtain a value of the input voltage near the open-circuit voltage multiplied by a factor of 0.72. This factor has been extracted empirically as it is usually the value of the MPP voltage. Then, the controller makes slight changes in the duty ratio to try to maintain that value of voltage constant. The algorithm for the “Constant voltage” control technique is addressed in Figure 16.

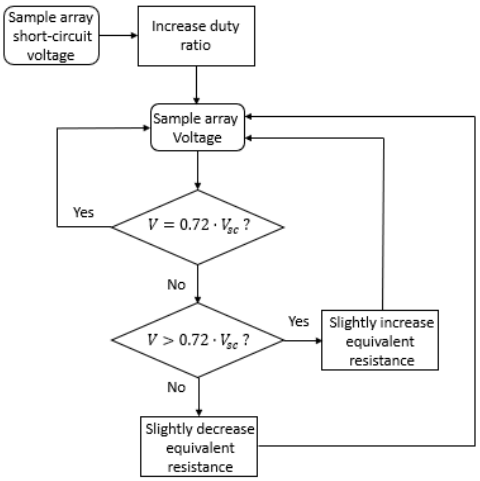

Fig. 16. Algorithm for Constant voltage control technique.

Last, there is another control algorithm called “Incremental conductance” which is more based in mathematical principles and tries to be more precise with less iterations. Basically, the control manages to find the maximum power point in the P-V curve by differential methods. The basis is the following showed in Equation 2.4:

$$MPP \rightarrow \frac{dP}{dV} = 0 \rightarrow P = V \cdot I \tag{2.4}$$

Deriving the power expression in Equation 2.4 returns:

$$\frac{dP}{dV} = V \cdot \frac{dI}{dV} + I \cdot \frac{dV}{dV} = I + V \cdot \frac{dI}{dV}$$

We can make an approximation by changing the derivatives for increments:

$$\frac{dP}{dV} \approx I + V \cdot \frac{\Delta I}{\Delta V} = 0 \rightarrow -\frac{I}{V} = \frac{\Delta I}{\Delta V}$$

That expression will be the core of the algorithm. The control will always be reading the voltage in the terminals of the panel and it suffers a variation due to irradiance changes, the controller will start to compute analysis. The controller will be driven by comparing the expression extracted above and make changes in the circuit if the incremental conductance changes. The algorithm of this type of control is represented in Figure 17.

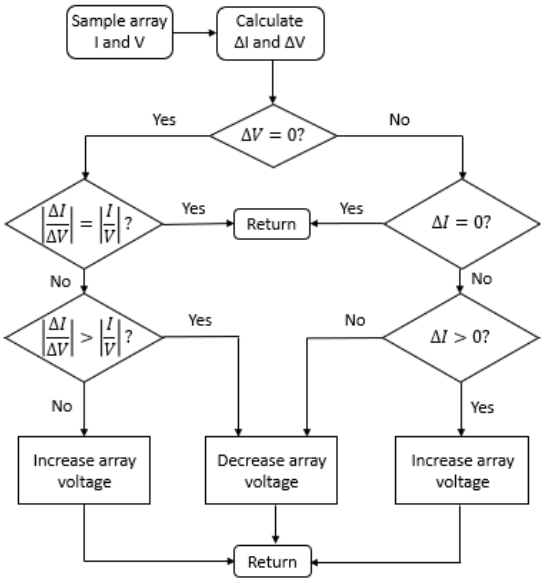

Fig. 17. Algorithm for Incremental conductance control technique.

This type of control requires more computation in the controller due to its algorithm being more complicated. However, it can track the MPP faster than other techniques as each perturbance is corrected at once with the algorithm. As the operation point is dynamic it will also cause oscillations in the output power but smaller than in the Perturb and observe technique. It will also need another requirement; the operation point must be placed in the MPP at the start of the algorithm so as to make corrections and return to that point again. If this is not accomplished, the controller will be moving the operating point towards one that does not maximize the power extraction.

2.5. Solar power evolution

In these two last decades, the solar power capacity of countries all over the world has increased exponentially. This has been caused by the development in solar technology together with the increment in panel manufacturing. This led to an increase in reliability and efficiency in the functioning of solar modules (shown in Figure 18), and a reduction of the price of kWh of energy generated. In addition, other factors that have boosted the solar energy generation are net metering and incentives given by governments encouraging investors to begin solar generation projects supporting solar PV installations in many countries.

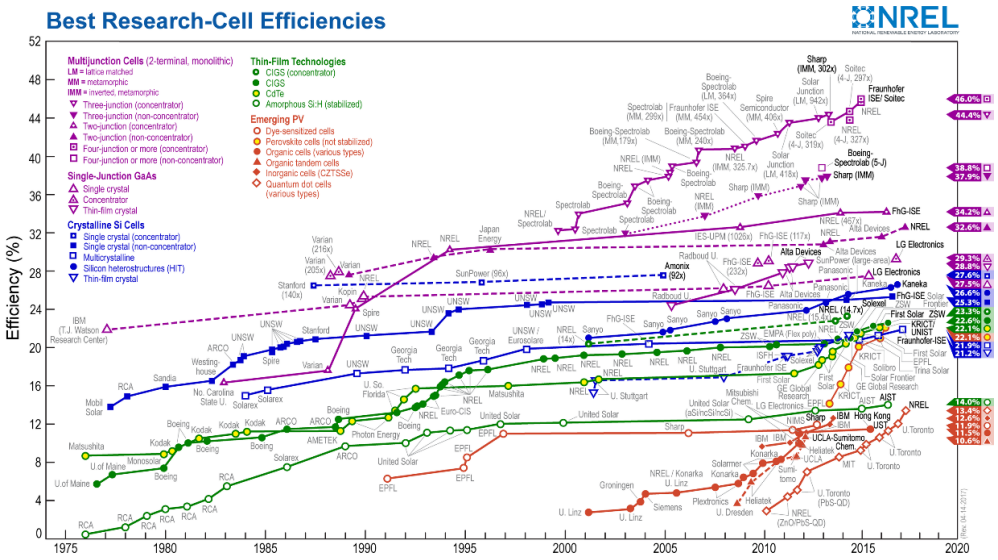

Fig. 18. Increase of solar panel efficiency over the years.

Analyzing Figure 18, we can distinguish each type of solar panel in terms of material and technique used in its manufacturing due to the range of efficiency levels they present. Green lines represent thin-film technology panels made of amorphous silicon, CIGS (copper indium gallium), CdTe (selenide and cadmium telluride), and polymer organic, for instance. These types of solar panels present a low price of manufacturing but also a low level of efficiency (around 5%).

Another type of technology used is Bulked-type or Wafer-based (blue curve), panels made of mono-crystalline silicon, poly-crystalline silicon or poly-crystalline band. This technology has opposite features

than the other mentioned, those panels can perform with high efficiency (from 20% to 25%) but they have higher manufacturing costs due to the shortage of silicon supply during the last years.

The purple curve shows the evolution of the cutting-edge manufacturing technologies speaking of efficiency. That technology is called multijunction cells, whose name is self-explanatory. These kinds of solar panels perform the best but a very high cost. Their efficiency can almost reach the 50% which in comparison with the previously mentioned 5% in thin-film technologies shows the enormous development that has been achieved. That technology needs years of research and improvement of manufacturing techniques to reduce its costs and become economically feasible to be used in real solar systems.

Last, the orange curve shows emerging PV technologies that as expected, they have low efficiency for the moment. More research and development will be needed to know if those technologies can flourish and become reasonable and innovative ways to generate solar PV energy.

Over the years, solar power capacity has been increasing as more and more countries are joining the cause of increasing their solar energy generation share. At the moment, more than a hundred countries are producing solar energy within their borders. Talking about history, Japan was the leading country in terms of solar PV capacity when this type of energy generation started growing from the bottom. Then, around 2000, Germany and Europe, in general, took that leading place due to big government funding, boosting their solar production at an impressive pace. This hegemony changed with the emerging economy of China, the industrial development that the country is conducting needs a vast amount of energy to be carried. For that reason, they are investing in cheap energy resources such as coal but also in solar PV systems as they possess a big amount of land to place those solar parks and concern about the environment is rising. China has been established as the first world power in terms of solar PV capacity.

The significant amount of money that has been injected into solar projects has led to this situation with almost one third of energy share possessed by Chinese companies.

China has become a big solar panels producer due to its low manufacturing costs and economies of scale. This has helped this country reach the capacity numbers it has nowadays. Germany has also been established as one of the leading countries in term of panels manufacturing despite being much smaller as a country having less land to be filled with panels. Other two powerful countries with respect solar panels manufacturing are the USA and Japan. One characteristic of the production of Japan is that it is

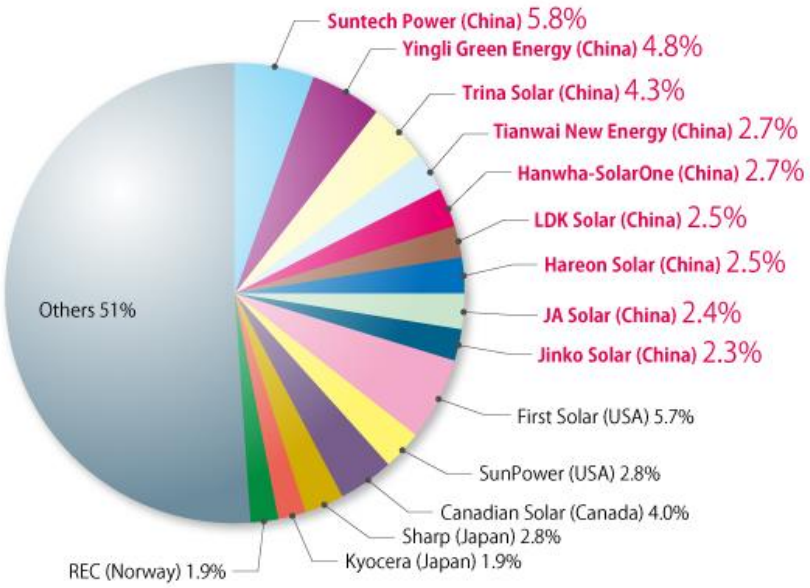

Fig. 19. Energy production share by companies.

leading the development of solar PV technology developing cutting-edge solar panels but a higher cost. Each country has its characteristics when producing the infrastructures driving solar energy extraction, but the big efforts and money invested make them be the top four solar energy producers in the world. Nowadays, China is the leader in solar energy capacity share followed by Germany, Japan, and the USA.

Addressing the situation of the USA in solar PV capacity it is surprising that they are not producing that much quantity of energy despite being the first world economic power. It is simple, they are relying more in wind power generation instead of solar power, however, big companies in the USA have the potential to grow fast making this country one of the fastest growing markets.

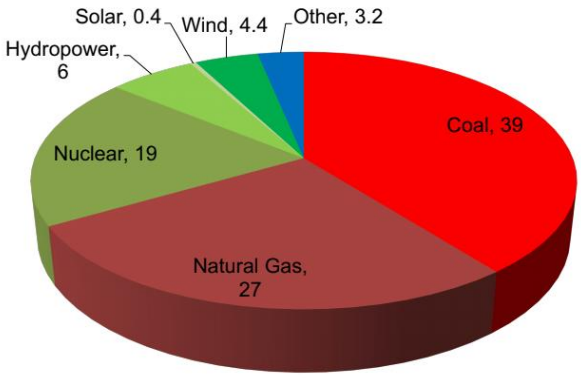

Fig. 20. US electricity generation by 2014.

As shown in Figure 20, renewable energy generation share is hold by hydropower and wind power. Nuclear power has maintained constant representing a 20% of the energy share over the years by increasing capacity factors of the nuclear plants without a significant number of plants being commissioned. Conventional and polluting energy generation is shifting towards greener resources, but with the actual issue of storage in the horizon. This outlook shows how important is to study solar power possibilities as right now it is not exploited at its maximum potential and have an enormous perspective of growth.

3. Principles of Flyback DC-DC converter.

Flyback converters are a type of DC-DC converters with a special feature, they possess galvanic isolation. This is achieved with a transformer in the middle of the circuit storing energy to then release it to the load. The special design of this converter makes the Flyback an indirect converter as it does not have a direct path between the input and the load in any moment of the operation. Its design is showed in the Figure 21:

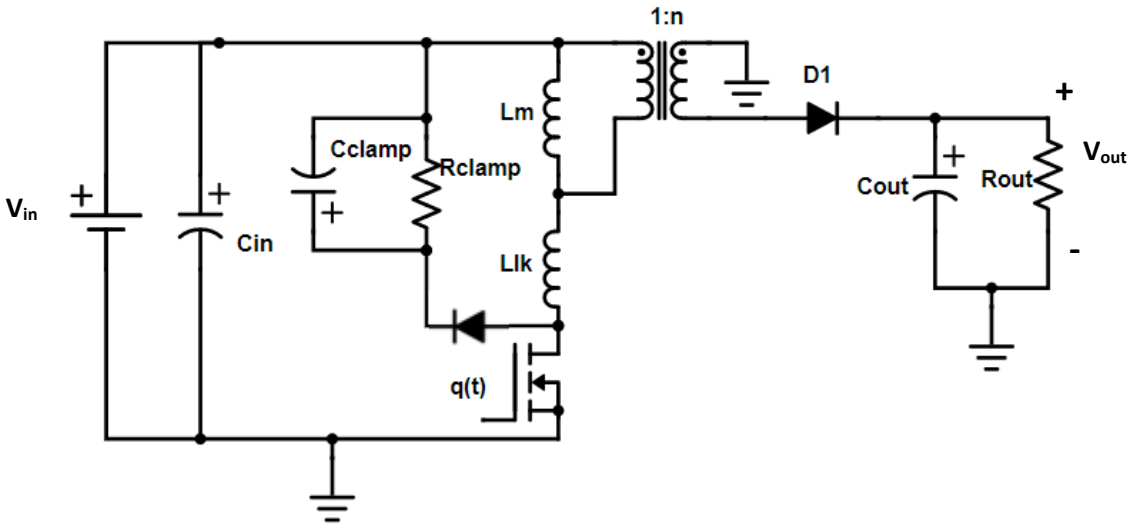

Fig. 21. Flyback circuit design.

The special characteristic that makes this converter different from other isolated ones is the connection of the transformer's secondary windings, as shown above the dot in those windings is reversed. This is the reason why the Flyback operation is indirect. Now, let use derive the transfer function of our converter. The key point to make the calculations is using the inductor voltage or the capacitor current to calculate that transfer function. This is caused because the average current in a capacitor or the average voltage across an inductor must be equal to zero in periodic steady state. We decide to use the inductor's voltage.

First, we analyze the circuit when the FET is conducting with the circuit showed in Figure 22.

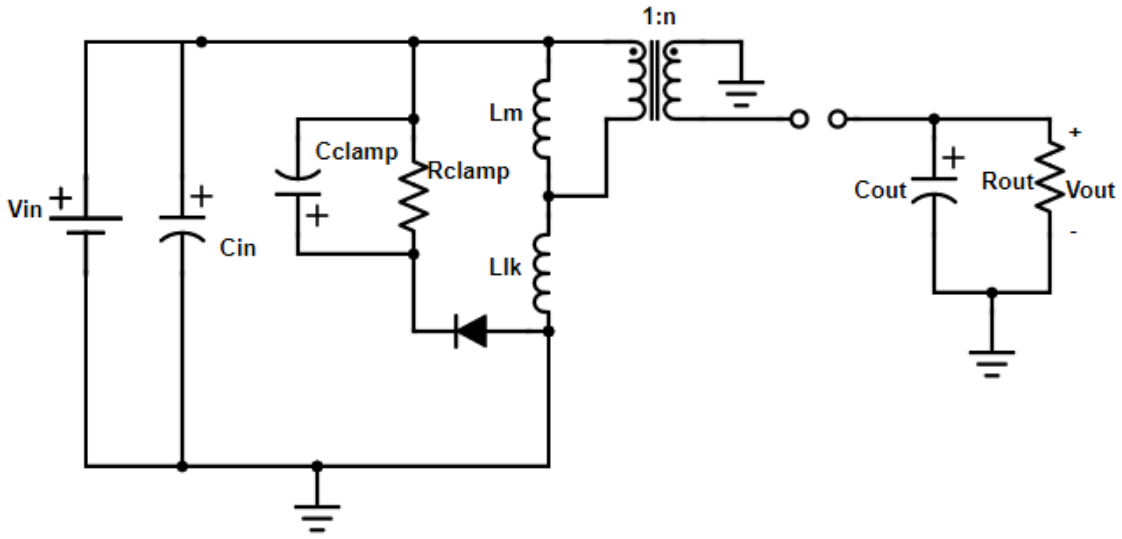

Fig. 22. Converter's state when the FET is turned on.

$$V_L = V_{in} \cdot \frac{L_m}{L_m + L_{lk}} \tag{3.1}$$

This section, we will assume that the transformer is ideal, and the leakage inductance is negligible. The real case will be addressed in the simulations section. With that in mind:

$$V_L \approx V_{in}$$

Now, analyzing the second phase of the converter's operation in which the FET is turned off and the rectifying diode is conducting. This will be studied with Figure 23.

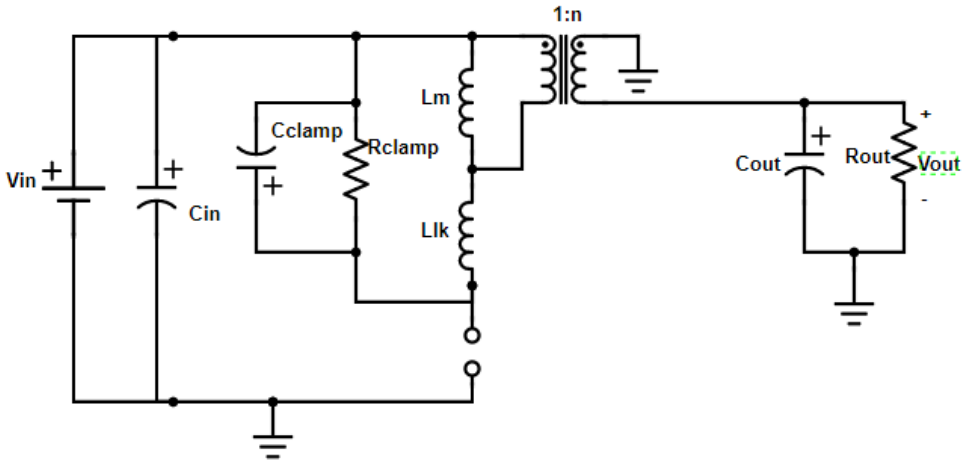

Fig. 23. Converter's state when the FET is turned off.

$$V_L = -\frac{V_{out}}{n} \tag{3.2}$$

Following the average voltage across the inductor rule stated before, the transfer function for an ideal Flyback converter is calculated as showed next:

$$V_L = D \cdot V_{in} - (1-D) \cdot \frac{V_{out}}{n} \rightarrow \frac{V_{out}}{V_{in}} = \frac{n \cdot D}{(1-D)} \tag{3.3}$$

With D being the duty ratio of the FET or in other words, the time when it is turned on during a switching period.

Once we have deduced the most basic characteristic of the converter, the transfer function, we can explain more about the functioning. In the first state, when the rectifying diode is blocking, the magnetizing inductance starts storing energy but without the transformer inducing current in the secondary windings due to the reversed connection. When the transistor turns off and the rectifying diode starts conducting, the magnetizing inductor maintains the current flowing throw it and starts to deliver energy to the load. This is the transition making the converter indirect.

In the first state, the leakage inductance is also charging, and as an inductor it will not allow the current to drop to zero instantaneously. That will force us to implement a clamping circuit to avoid overvoltage in the FET as the leakage current needs a way out. Figure 24 specifies where that clamping circuit is placed.

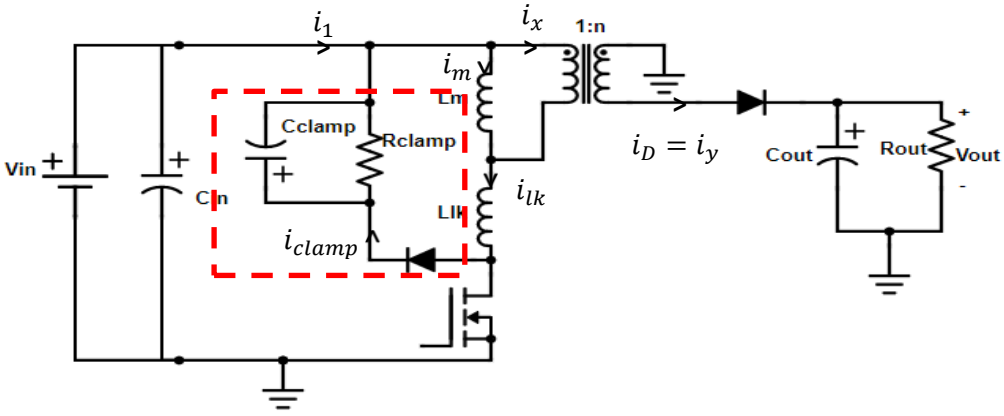

Fig. 24. Flyback converter with the clamping circuit highlighted.

This clamping circuit is needed to redirect the leakage current and dissipate the energy stored in the leakage inductor. As expected, this would lead to a loss of efficiency but obtaining in exchange better safety for our transistor. To further understand the behavior of this circuit, we analyze the currents flowing in each state of the converter.

Following the current notation showed in the last figure, we start deriving the graphs displaying the behavior of each of those currents. As explained before, in the state when the FET is turned on, the current coming from the input is the same as the magnetizing current but when the state changes, the input current goes to zero and the magnetizing current starts to induce in the secondary windings. As the leakage current has special effects and ideally it does not affect the operation of our converter, we will address it in the simulation section where those effects are visible. The rest of currents flowing through the converter are the following showed in Figure 25.

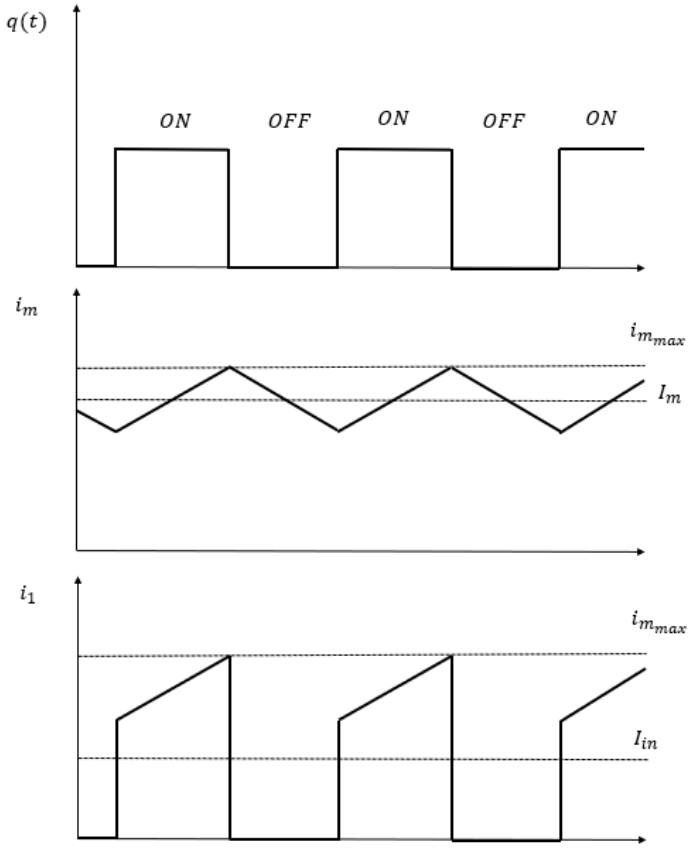

Fig. 25. Currents flowing in the primary side of the transformer.

As depicted in Figure 25, when the FET is turned on, the magnetizing inductor receives a positive voltage and consequently, the current flowing through it increases. When the FET is off the opposite event happens resulting in that triangular waveform. The current coming from the source i_1 shares the same value with i_m when the FET is on but drops to zero in the next state because the switch turns off and blocks the current completely. Now let us address with Figure 26 what happens in the secondary side of the transformer with its induced currents.

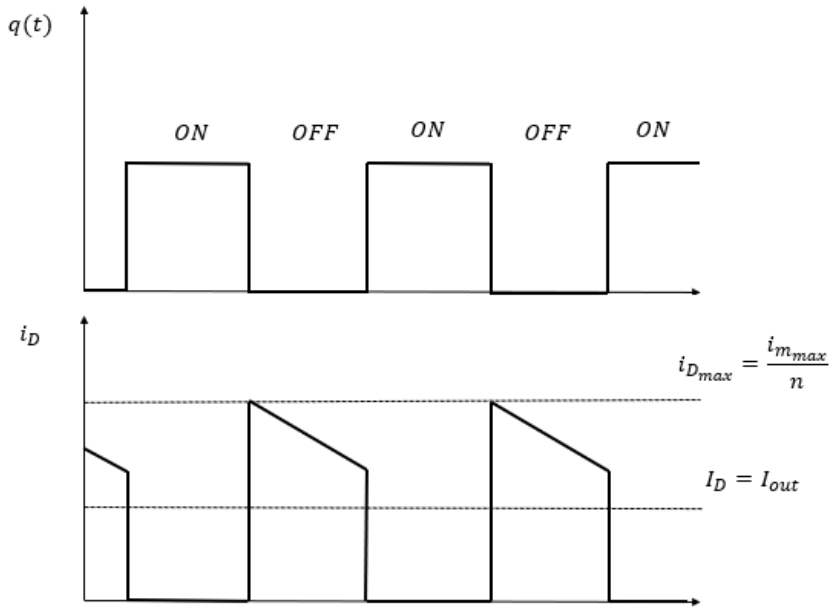

Fig. 26. Current flowing in the secondary side of the transformer.

When the transistor is in its on state, the rectifying diode is blocking the current and because of that it has a value of zero. That changes when the switch turns off and the diode starts conducting. In this situation, the magnetizing current is equal to i_x meaning that it will induce the current i_y in the secondary side of the transformer.

$$i_m = i_x \rightarrow i_x = i_y \cdot n \rightarrow i_y = i_D = \frac{i_m}{n}$$

With the signs of the currents showed in the previous figure, the transformer's currents follow that equation. Doing a KCL in the output node we deduce that I_D will be equal to I_{out} or in other words, the current flowing to the load.

4. Component design

4.1. Switching frequency

The first parameter that will determine the others is the switching frequency. Increasing these parameters is not always good. Despite the fact that it would reduce the ripple in the inductors and capacitors (meaning a smaller size of those components), a high switching frequency increases the switching losses of the converter, which is not good in this low power converter. In addition, a higher switching frequency would negatively affect the clamping circuit as it would make the losses in it bigger.

For those reasons, we chose a big switching frequency but not one big enough to lower the efficiency to unacceptable levels. We will apply a 100 kHz switching frequency to the MOSFET and with that number, we will obtain the other components values.

4.2. Transformer turns ratio

To obtain the relationship between the winding in the primary and the secondary of the transformer, we will use the transfer function of the flyback transformer:

$$\frac{V_o}{V_i} = \frac{n \cdot D}{1 - D}$$

The case with the higher duty ratio, and with that, the highest output voltage will be when receiving low irradiance. Our upper limit irradiance is 1 kW/m^2, this is the value of irradiance with what we are going to measure the parameters. As it is always wanted to track the MPP, we deduce the values of voltage and current with that irradiance for our solar panel showed in the solar panel curves of Figure 27:

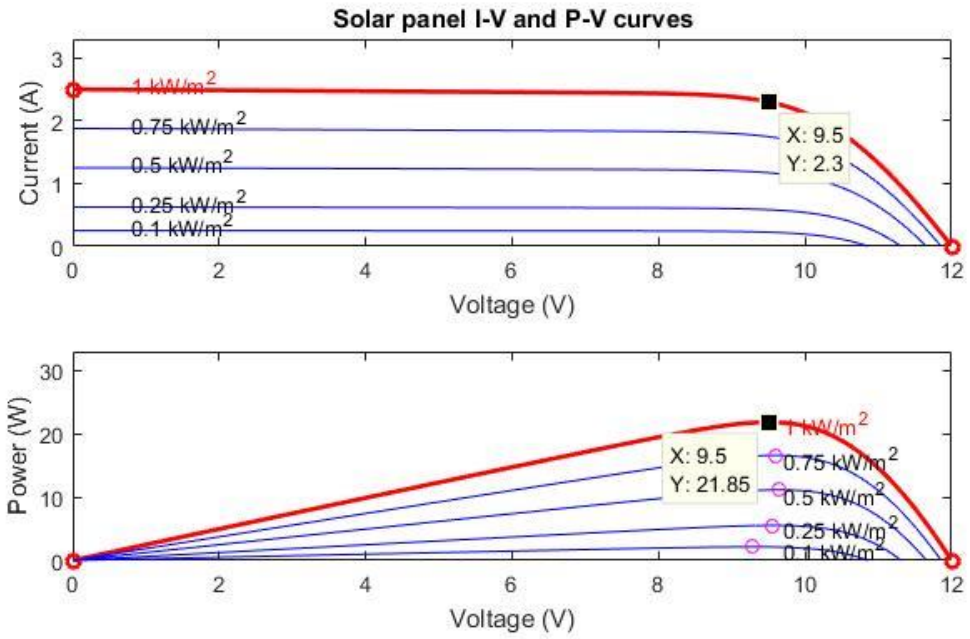

Fig. 27. Characteristic curves of our solar panel.

$$V_{0.1} = 9.5\ V$$

$$I_{0.1} = 2.3\ A$$

Using a value of 10 V to obtain the turns ratio, 200 V in the output are attained. This oversize will protect our components in case of need. For that value of input voltage, I will fix a duty ratio of 0.5.

$$n = \frac{V_{out}}{V_{in}} \cdot \frac{1-D}{D}; n = \frac{200}{10} \cdot \frac{1-0.5}{0.5} = 20 \rightarrow n = 1{:}20 \quad (4.1)$$

In the next section, the components values will be calculated with an irradiance of 1kW/m^2 in order to give safety and stability to our converter.

4.3. Output resistor

Having the turns ratio and the duty ratio fixed for the value of 1 kW/m^2 we will proceed to obtain the value of the output resistor to calculate the equivalent resistance of the converter with that irradiance

and work with that when the irradiance changes, also we have to alter that equivalent resistance. First, we start working with the following equation:

As extracted from [4]:

$$R_{eq} = \left(\frac{1}{D} - 1\right)^2 \cdot \frac{1}{n^2} \cdot R_{out} \tag{4.2}$$

We measure that value of R_{out} in the case of 1 kW/m^2, duty ratio of 0.5, and turns ratio of 1:20 as calculated before. Now, we have to acquire that value of R_{eq} with the I-V curve with 1 kw/m^2 of irradiance. As showed in the turns ratio section, the MPP voltage will be 9.5 Volts and the current 2.3 Amps.

$$R_{eq} = \frac{V_{in}}{I_{in}} = \frac{9.5}{2.3} = 4.13\ \Omega \tag{4.3}$$

Now we combine (4.3) and (4.2) to obtain:

$$4.13 = \left(\frac{1}{0.5} - 1\right)^2 \cdot \frac{1}{20^2} \cdot R_{out} \rightarrow R_{out} = 1652\ \Omega$$

We made that calculation in the case of 1 kW/m^2 because our solar panel will suffer variations in the irradiance due to the shading of the clouds or even because of dust retained in the surface as it happens in the deserts easily. With that in mind, I will explain that selection for the irradiance.

At 1 kW/m^2 the equivalent resistance is 4.13 Ω, and as that irradiance decreases, the R_{eq} that our converter has to follow in order to reach the MPP will increase. Figure 28 shows that statement:

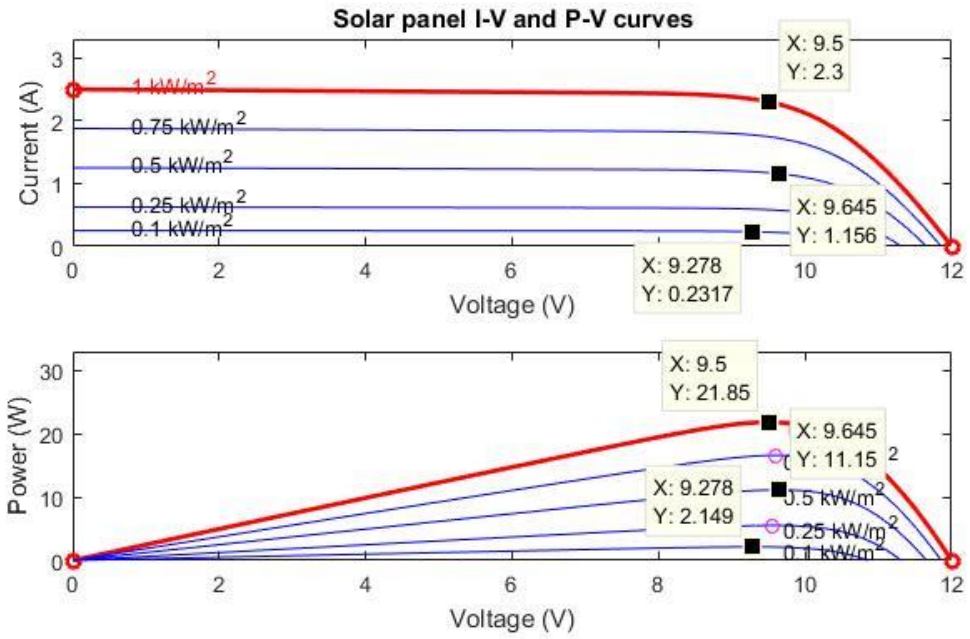

Fig. 28. Solar panel curves with MPP values highlighted.

With the values of voltage and current in the MPP for different irradiance numbers, we calculate the equivalent resistance that the converter must meet in order to extract maximum power:

$$R_1 = 4.13\ \Omega \rightarrow Obtained\ before$$

$$R_{0.5} = \frac{9.645}{1.156} = 8.34\ \Omega$$

$$R_{0.1} = \frac{9.278}{0.2317} = 40.04\ \Omega$$

With that, we deduced that when we decrease the irradiance received, the equivalent resistance raises for that MPP. Now we will assume that in a very sunny day a cloud is shading our solar panel and because of that the irradiance changes from 1 kW/m^2 to 0.1 kW/m^2. When the cloud starts shading, the solar panel

receives 0.1 kW/m^2 of irradiance and our converter has to change the duty ratio in order to meet the MPP. Our new duty ratio will be, using equation (4.2) and $R_{0.1}$:

$$R_{0.1} = \left(\frac{1}{D} - 1\right)^2 \cdot \frac{1}{n^2} \cdot R_{out}; D = \frac{1}{\sqrt{\frac{R_{0.1} \cdot n^2}{R_{out}}} + 1}$$

$$D = \frac{1}{\sqrt{\frac{40.04 \cdot 20^2}{1652}} + 1} = 0.243$$

With that duty ratio at the MPP together with an input voltage of 9.278 Volts, we have the following output voltage:

$$V_{out} = 9.278 \cdot \frac{0.243 \cdot 20}{1 - 0.243} = 59.67\ V$$

As we see, when a huge change of irradiance happens, our components will be safe because of the modeling with the upper limit irradiance. When operating at 0.1 kW/m^2 and the cloud disappears returning to the value of 1 kW/m^2, the contrary will happen. The converter will be operating at an equivalent resistance of 40.04 Ω making the solar panel give an input voltage near the open-circuit voltage of the panel rated at 12 Volts. However, the converter was operating at a duty ratio of 0.243 so the output voltage in the worst case would be:

$$V_{out} = 12 \cdot \frac{0.243 \cdot 20}{1 - 0.243} = 77.04\ V$$

As we can notice, with that configuration our converter operation presents a great stability and safety for the components as huge variations will not produce big output voltage.

4.4. Magnetizing inductance

This is a crucial component of our device because here is where the converter will store energy and then release it to the secondary of the transformer when the MOSFET turns off. This value of the inductance will determine the percentage of ripple current flowing through the magnetizing inductance or L_m. We cannot take an enormous value to eliminate the ripple because we need a reasonable value to build the transformer, and also, because of the leakage inductance or L_{lk} present in every real transformer.

As the value of L_{lk} cannot be measured before the construction of the converter, we will assume that it has a value of the 3% of the L_m. It is true that in a real transformer, the higher the L_m, the higher it will be the L_{lk}. The problem with that leakage inductance is that the bigger it is, we will have bigger commutation time between phases of the MOSFET, reducing the pulses of voltage in the L_m, thus that will lower the duty ratio, and with it, the desired output voltage.

With that in mind, we will sacrifice some percentage of the ripple current in order to avoid that. We also have to consider that L_m has to be sufficiently big to store the energy in it so very low values are unacceptable. We will analyze one state of the MOSFET to deduce the ripple current equation:

The state with FET turned on is represented in Figure 29:

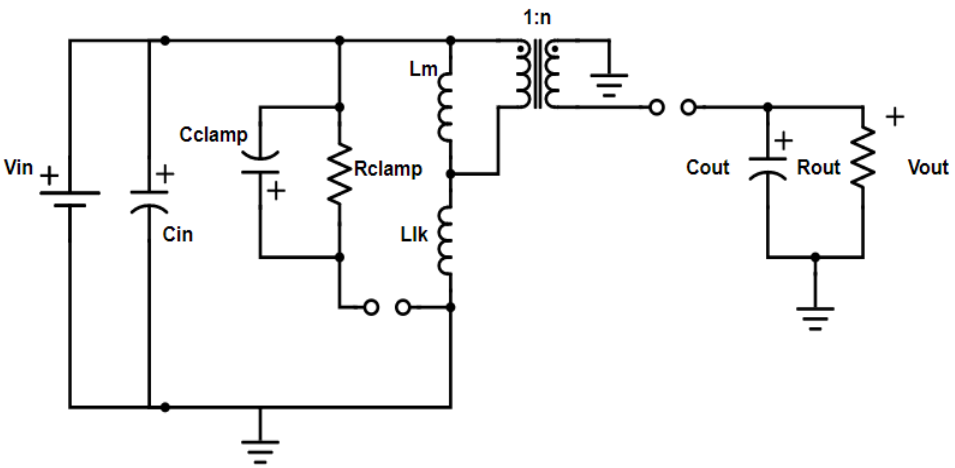

Fig. 29. State of the Flyback converter with the switch turned on.

With the voltage in the magnetizing inductor in one of the states (let us take the one with the MOSFET on) we will calculate the ripple current in that inductor. It does not matter which state we choose because as the average value of an inductor voltage is zero, we will obtain the same value for the ripple current but with different sign.

$$V_{Lm} = V_{in} = L_m \cdot \frac{di_m}{dt} \tag{4.4}$$

As V_{in} is constant, we can change the derivatives by increments.

$$V_{in} = L_m \cdot \frac{\Delta i_m}{\Delta t};\ \mathrm{L_m} = \frac{V_{in} \cdot DT}{\Delta i_m};\ \ \mathrm{L_m} = \frac{V_{in} \cdot D}{\Delta i_m \cdot f_{sw}} \tag{4.5}$$

To make the calculus, we will limit the ripple current to the 50% of the average value of current that will flow through the L_m. The less favorable case will happen with 1 kW/m^2 of irradiance with the solar panel supplying 2.3 Amps at the MPP. The percentage chosen is quite big but is necessary to lower the leakage inductance to the maximum, that ripple will be addressed by the output capacitor to rectify it and have a lower percentage of ripple voltage in the output.

$$\Delta i_m = 0.5 \cdot 2 \cdot I_m$$

We multiply it by a factor of 2 because we are doing the percentage of ripple respect the average value, so the total increment will be the double.

$$I_m = I_{in} + I_d \cdot n = I_{in} + \frac{V_{out}}{R_{out}} \cdot n = 2.3 + \frac{190}{1652} \cdot 20 = 4.6\ A \tag{4.6}$$

$$L_m = \frac{9.5 \cdot 0.5}{0.5 \cdot 2 \cdot 4.6 \cdot 100 \cdot 10^3} = 10.33\ \mu H$$

4.5. MOSFET

The important parameters that should be taken into consideration when choosing the MOSFET are the current and the voltage that that switch will withstand. We will start with the maximum voltage that obviously will appear when the MOSFET is turned off:

$$V_{FET} = V_{in} + \frac{V_{out}}{n} = 9.5 + \frac{190}{20} = 19\ V \tag{4.7}$$

However, for safety issues we will oversize it to the double at least, depending on the MOSFETs that we will find when choosing the components.

$$V_{FET} > 38V$$

For the rated current flowing through our switch when it is turned on, we have Equation 4.8:

$$I_{FET} = i_{m_{max}} = I_m + \frac{\Delta i_m}{2} = I_m + \%RIP \cdot I_m = 4.6 + 0.5 \cdot 4.6 = 6.9\ A \tag{4.8}$$

To select a proper MOSFET for our converter it is also important to take into account the conduction and switching losses because a switch with big power dissipation is unacceptable. This issue will be addressed when choosing the components in later sections.

The MOSFET selected for our operation is a IRF520 with a voltage rating of 100 Volts and a maximum power dissipated of 60 Watts. The power losses will be addressed in the efficiency subsection.

4.6. Rectifying diode.

The diode just like the MOSFET will be chosen depending on the blocking voltage that must suffer and the maximum current flowing through it when it is conducting. In addition, we have to choose a diode with a recovery time low enough to follow our switching frequency. We will start measuring the maximum blocking voltage that will suffer with our parameters:

$$V_D = V_{in} \cdot n + V_{out} = 9.5 \cdot 20 + 180 = 370\ V \tag{4.9}$$

Second, the maximum current flowing through it will be:

$$I_{in_{max}} = 2.3\ A \rightarrow \frac{\Delta i_m}{2} = 50\% \cdot I_m = 0.5 \cdot 4.6 = 2.3\ A$$

$$i_{D_{max}} = \frac{I_D}{1-D} + \frac{\Delta i_m}{2} \cdot \frac{1}{n} = \frac{V_{out}}{R_{out} \cdot (1-D)} + \frac{\Delta i_m}{2} \cdot \frac{1}{n} = \frac{190}{1652 \cdot 0.5} + 2.3 \cdot \frac{1}{20} = 345\ mA \tag{4.10}$$

Finally, for the recovery time we have to observe which is the minimum time the diode will be turned off to account for the time it needs to take to recover after switching it state. Figure 30 shows the behavior of a diode when changing its state:

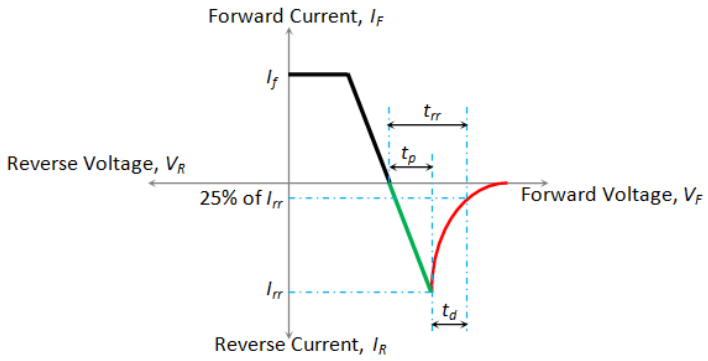

Fig. 20. Behavior of a diode when it turns off.

Then, the reverse recovery time of the diode should be lower than the time it should remain turned down before turning off the MOSFET again.

$$t_{rr} < (1 - D_{max}) \cdot T_{SW};\ \ t_{rr} < (1 - 0.5) \cdot 10\mu s \rightarrow trr < 5\ \mu s \tag{4.11}$$

We choose MUR460 diode which is an ultrafast rectifier with a rating of 4A/600V and a recovery time of 25-35 nanoseconds.

4.7. Resistor-capacitor-diode (RCD) clamp

To design this circuit, first, we will fix the value of the voltage in the clamp. The higher the voltage in this clamping circuit, the better efficiency our converter will have. To design and fix this clamping voltage we use the maximum voltage in the MOSFET as the Figure 31:

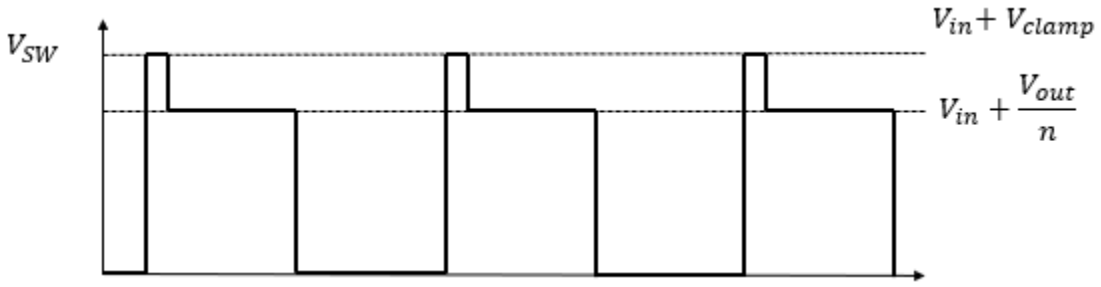

Fig. 31. Voltage across the transistor with a clamping circuit.

Our maximum clamping voltage will occur at the minimum input voltage, then, to protect our switch we will make the calculations with the maximum voltage that can withstand our switch and the maximum input voltage to make that clamp voltage lower:

$$V_{clamp} = V_{SW} - V_{in_{max}} = 38 - 9.5 = 28.5\ V \tag{4.12}$$

Having, that clamping voltage selected, now we have to fix it with component values that we can handle. That will be done selecting the proper clamping resistance. The next step is calculating the dissipation losses in that resistor, that energy dissipated will be the one stored in the leakage inductance:

First, we deduce doing a KCL that:

$$I_{in} = I_{lk} \tag{4.13}$$

And the average energy stored in the leakage inductor is the following:

$$E_{stored} = \frac{1}{2} \cdot L_{lk} \cdot I_{lk}^2 = \frac{1}{2} \cdot L_{lk} \cdot I_{in}^2 \tag{4.14}$$

The power loss in the clamping resistor follows Equation 4.15:

$$P_{loss} = E_{stored} \cdot f_{sw} \tag{4.15}$$

$$P_{loss} = \frac{1}{2} \cdot 0.03 \cdot 10.33 \cdot 10^{-6} \cdot 2.3^2 \cdot 100 \cdot 10^3 = 0.082\ W = 82\ mW$$

Now with that power loss, we calculate the value of the clamping resistor to fix the clamping voltage to a value of 30 V:

$$P_{loss} = \frac{V_{clamp}^2}{R_{clamp}};\ \ R_{clamp} = \frac{28.5^2}{0.082} = 9909.3\ \Omega \rightarrow R_{clamp} = 9.9\ k\Omega \tag{4.16}$$

Now, the only step remaining is the calculation of the clamping capacitor. For that, we have to select a capacitor large enough to make the clamping voltage reasonably smooth. Voltage ripple for clamping circuits are typically limited to 5%-10% of the clamping voltage. This will be achieved with equation 4.17:

$$R_{clamp} \cdot C_{clamp} \gg T_{SW} \rightarrow R_{clamp} \cdot C_{clamp} > 10 \cdot T_{SW} \tag{4.17}$$

This way we will have a very big time constant in the RC circuit of the clamp limiting the voltage ripple.

$$C_{clamp} > \frac{10}{100 \cdot 10^3 \cdot 9900} \rightarrow C_{clamp} > 101\ nF$$

Then, we select a slightly smaller capacitor of 0.1 μF to round the capacitance to a value feasible for the commercial capacitors. This will not change the ripple voltage percentage a lot.

To select the clamping diode, we have to think that the clamp should activate fast because that will avoid stresses in the MOSFET, but it also has to deactivate as soon as possible to interfere to the least extent with the effective duty ratio of the converter when commuting. For that reasons we will choose an ultra-fast diode with a reverse recovery time near 25 ns to improve the working conditions of the converter.

For the capacitors, we get to choose some ceramic-type ones to decrease the ESR the maximum as possible and in addition we will place some of them in parallel. We use 33 nF capacitors with three of them connected in parallel.

For the diode, we will use a MUR120 which is an ultrafast recovery one with a voltage rating of 200 Volts and a recovery time of 25-35 ns.

4.8. Output capacitor

This component will be the one limiting our ripple voltage in the output of our converter. The inductor could help with this task, but due to the presence of the leakage inductance that is not possible. Because of that, our capacitor will have a higher value than it could have but that will not cause troubles anyways. First, let us deduce the equations ruling that ripple in the capacitor voltage:

We will assume that our capacitor is big enough to take all the ripple current letting the load drain constant current at every moment. We will need the current flowing through the capacitor but first let us do a KCL to deduce that current:

$$i_D = i_{out} + i_c \tag{4.18}$$

With 4.18 we also deduce that:

$$I_D = I_{out} + I_c$$

We assumed that all the ripple current goes across the capacitor, those currents have the following waveform represented in Figure 32:

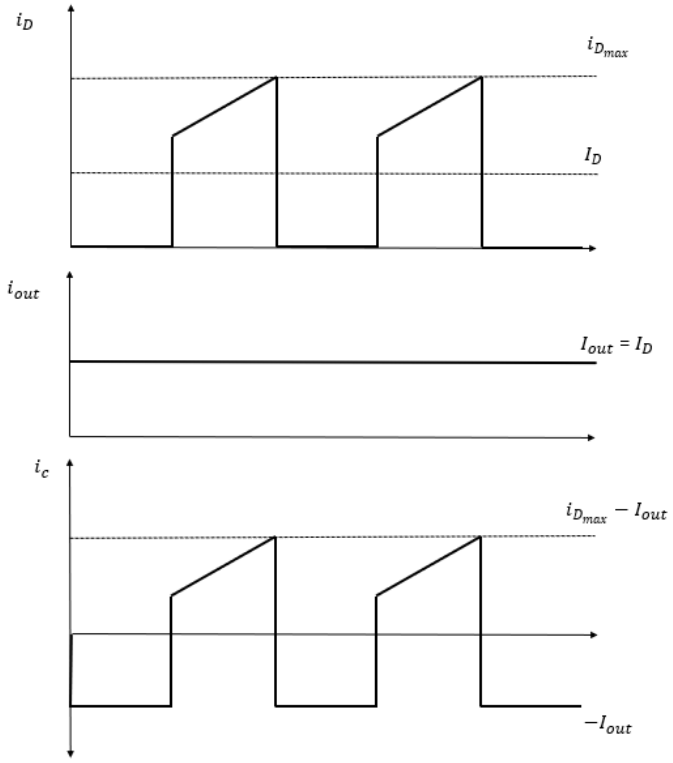

Fig. 32. Currents in the output node.

We know that the average current flowing through a capacitor must be zero as it cannot keep storing charge forever. That way we know that the area above and below the abscises axis in a time period is the same. With that in mind:

$$Q = \Delta v_c \cdot C_{out};\ \int_0^{DT} i_c \cdot dt = \Delta v_c \cdot C_{out};\ -I_{out} \cdot DT = \Delta v_c \cdot C_{out} \tag{4.19}$$

Now we fix the voltage ripple we want in the output. To ensure a smooth DC signal supplied by our capacitor we will state a 2% voltage ripple respect the average value (ramp value of a 4% of the DC value). This will result in:

$$-I_{out} \cdot DT = -0.04 \cdot V_{out} \cdot C_{out};\ \ C_{out} = \frac{I_{out} \cdot D}{f_{sw} \cdot 0.04 \cdot V_{out}}$$

$$C_{out} > \frac{\frac{190}{1652} \cdot 0.5}{100 \cdot 10^3 \cdot 0.04 \cdot 190} \rightarrow C_{out} > \ 76\ nF$$

Extracting that value, we will use a 0.1 μF capacitor to improve even further the ripple as it is not a huge capacitance.

For the capacitor, we also have to calculate the RMS current that is has to withstand. That is done with Equation 4.20 showed in [5]:

$$I_{CO}rms = I_{out} \cdot \sqrt{\frac{D_{max}}{1 - D_{\max}}} = \frac{190}{1652} \cdot \sqrt{\frac{0.5}{1 - 0.5}} = 115\ mA \qquad (4.20)$$

Another reason to make the voltage ripple that tight is because the ESR of the capacitor used. That ESR is the internal resistance of the capacitor that is accounted to be in series with it. That parasitic resistor will increase our voltage ripple so using a security factor when calculating the output capacitor is always good. We will not evaluate that resistance as we will try to use ceramic capacitors making that ESR negligible. In addition, we will place capacitors in parallel reducing the value of the resistance while stacking capacitance.

For these capacitors we choose the same as in the clamping capacitor, ceramic capacitors of 33 nF with three of them connected in parallel to reduce the ESR even more.

4.9. Input capacitor

Following the same work as the one done in section 4.8, firstly we will analyze the currents touching the capacitor node:

With that scheme in mind, we deduce the following KCL in Figure 33:

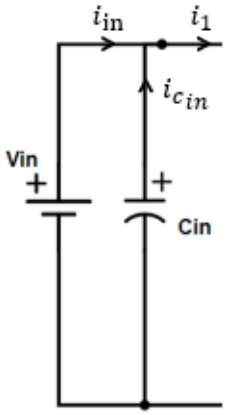

Fig. 33. Schematics of the input node.

$$i_1 = i_{c_{in}} + i_{in} \tag{4.21}$$

$$I_1 = I_{c_{in}} + I_{in} \rightarrow I_1 = I_{in} \tag{4.22}$$

We also know that:

$$i_{in} = I_{in} \rightarrow Pure\ DC\ current$$

$$q(t) = 1 \rightarrow i_{in} = i_m$$

$$q(t) = 0 \rightarrow i_{in} = 0$$

With that deductions, it is easier to explain the importance of the input capacitor. As we can see, i_{in} is not constant and when changing the switch state, it drops to zero abruptly. In real voltage sources there are internal inductances that do not allow the current to do this, so a capacitor is needed to provide that ripple current. This will be explained better with Figure 34:

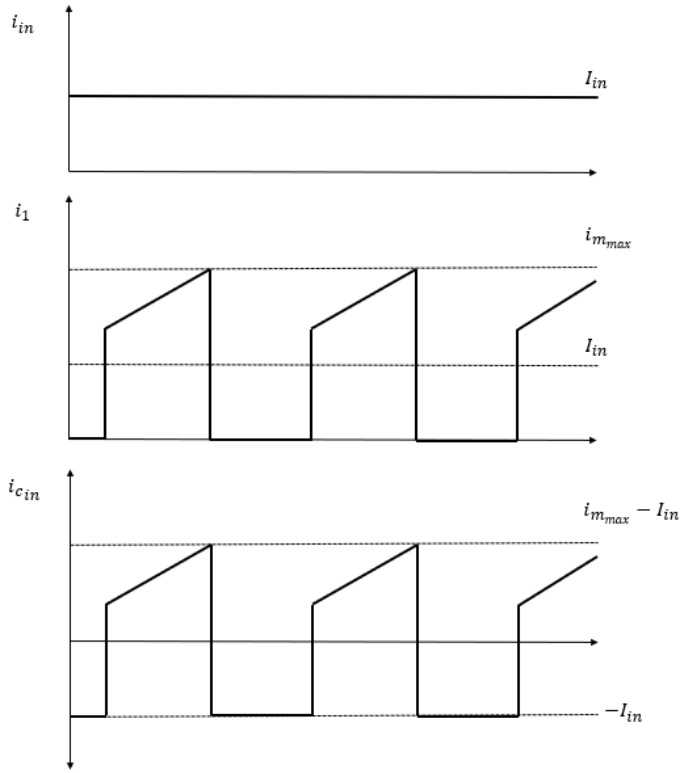

Fig. 33. Currents in the input node.

As seen here, the capacitor will supply the ripple current produced by the inductors in the transformer while i_{in} remains constant. To calculate the input capacitance, we will repeat the work done with the output capacitor:

$$i_c = C_{in} \cdot \frac{dV_c}{dt} \tag{4.23}$$

As said above, the average current though a capacitor is zero, so it does not matter which current section we analyze. We choose the flat one (switch off) to ease the calculations, and with that we can change the derivatives with increments:

$$I_{in} = C_{in} \cdot \frac{\Delta V_c}{\Delta t}$$

We want a ripple of less than a 5% with respect the average value, so this evolves to:

$$C_{in} > \frac{I_{in} \cdot (1 - D)}{f_{sw} \cdot 0.1 \cdot V_{in}} \rightarrow C_{in} > \frac{2.3 \cdot (1 - 0.5)}{100 \cdot 10^3 \cdot 0.1 \cdot 9.5} = 12.1\ \mu F$$

We also have to size the RMS current that will flow through that capacitor with Equation 4.24, also extracted from [5]:

$$I_{CI}rms = I_{in} \cdot \sqrt{\frac{D_{max}}{1 - D_{\max}}} = 2.3 \cdot \sqrt{\frac{0.5}{1 - 0.5}} = 2.3\ A \qquad (4.24)$$

In this case, we need a higher value of capacitance, so we decide to choose ceramic capacitors to reduce the ESR and with that the losses, with a value of 4.7 µF. Just like before we connect three of them in parallel to obtain the desired capacitance.

4.10. Transformer construction.

The most important part to take into consideration is the core that is going to be used. We have to check if we do not enter in saturation zone, if the core can store enough energy for our converter and if our wire will fit in that core. Other things to analyze are the transformer losses including the conduction and core ones. First, we select the core we want to use in the wide selection available. We get to choose the P42/49-3C81-E400, its datasheet is attached in the appendixes. The calculations will be made with the following relevant characteristics showed in Table 1:

Magnetic Core P36/22-3F3-E400		
A_L	Specific Inductance	400±3% nH
A_e	Effective Area	202 mm^2
V_e	Effective Volume	10700 mm^2
le	Effective Length	53.2 mm
g	Air Gap	430 µm
μ_c	Relative Magnetic Permeability of the Core	2000
B_{sat}	Saturation Magnetic Field	450 mT

Table 1. Characteristics of the core used.

For the calculations we will use the next simplified transformer scheme in Figure 35 as we will work with effective magnitudes:

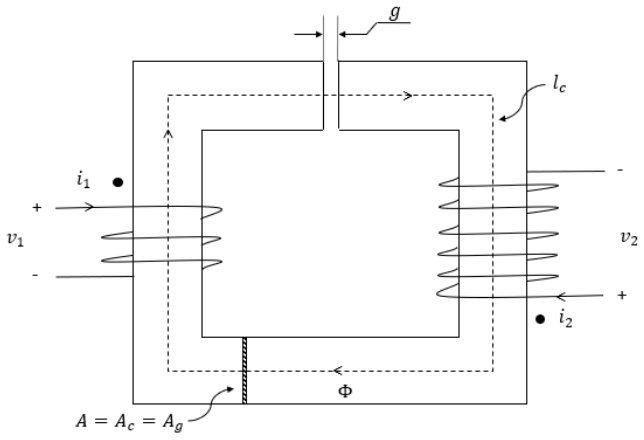

Fig. 34. Simple schematic of a transformer.

We start writing the magnetic circulation equation:

$$H_g \cdot g + H_c \cdot l_c = N_1 \cdot i_1 + N_2 \cdot i_2 \tag{4.25}$$

We also know that:

$$\oiint B \cdot dS = 0 \rightarrow Continuity\ of\ flux \tag{4.26}$$

Then, we deduce that:

$$\Phi_c = \Phi_g \rightarrow B_c \cdot A_c = B_g \cdot A_g \rightarrow \mu_c \cdot H_c \cdot A_c = \mu_0 \cdot H_g \cdot A_g = \Phi \tag{4.27}$$

$$H_c = \frac{\Phi}{\mu_c \cdot \mu_0 \cdot A_c}\ ;\ H_g = \frac{\Phi}{\mu_0 \cdot A_g}$$

Now with (4.25) and (4.27), we can substitute the magnetic circulation equation:

$$\frac{\Phi}{\mu_c \cdot \mu_0 \cdot A_c} \cdot l_c + \frac{\Phi}{\mu_0 \cdot A_g} \cdot g = N_1 \cdot i_1 + N_2 \cdot i_2$$

We can transform it into a magnetic circuit equation with the magnetic flux, reluctance and excitation currents:

$$\Phi \cdot \left[R_c + R_g\right] = N_1 \cdot i_1 + N_2 \cdot i_2$$

$$R_c = \frac{l_c}{\mu_c \cdot \mu_0 \cdot A_c}\ ;\ R_g = \frac{g}{\mu_0 \cdot A_g}$$

Shown in Figure 36 is the equivalent circuit:

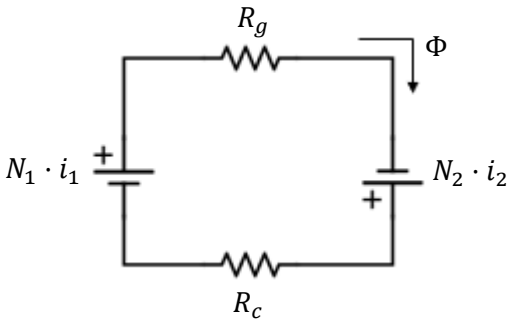

Fig. 35. Equivalent magnetic circuit.

Now, to calculate the value of the inductance with respect to the primary side of the transformer we have to passive the source of the secondary windings resulting in:

$$\Phi \cdot [R_c + R_g] = N_1 \cdot i_1 \rightarrow \Phi = \frac{N_1 \cdot i_1}{R}$$

$$\lambda = N \cdot \Phi \tag{4.28}$$

$$v = \frac{d\lambda}{dt} = \frac{d\Phi}{dt} = \frac{N_1^2}{R} \cdot \frac{di}{dt} \tag{4.29}$$

Relating that equation with the one ruling an inductor we extract that $L_m = \frac{N_1^2}{R}$ with respect to the primary windings.

We also know that $A_L = \frac{1}{R}$, so the number of turns we need in the primary to obtain the value calculated in the magnetizing inductance section:

$$L_m = N_1^2 \cdot A_L \rightarrow N_1 = \sqrt{\frac{10.33 \cdot 10^{-6}}{400 \cdot 10^{-9}}} = 5.08 \rightarrow N_1 = 6\ turns \tag{4.30}$$

$$L_m = 400 \cdot 10^{-9} \cdot 6^2 = 14.4\ \mu H$$

We round to the bigger number because we do not want the ripple to surpass the percentage calculated. As we obtained a 1:20 ratio, the number of turns in the secondary will be 120 turns.

Now we will start proving whether the core chosen is valid for our converter or not.

1. Saturation

In the datasheet of this core, which is made of soft ferrite, it is stated that the saturation magnetic field is 0.45 Tesla. With our converter parameters we will check if we are working out the saturation zone:

$$\Phi \cdot \left[R_c + R_g\right] = N_1 \cdot i_1 + N_2 \cdot i_2;\ B \cdot A_e \cdot R = N_1 \cdot i_1 + N_2 \cdot i_2$$

$$B \cdot A_e \cdot \frac{1}{A_L} = N_1 \cdot i_1 + N_2 \cdot i_2$$

In our converter these are the maximum primary and secondary currents, the worst case would happen when only the primary windings is conducting because there is no induced current in the secondary of the transformer opposing to the flux, according to the Bentz's Law. Then, our peak magnetic field value is:

$$i_{1_{max}} = i_{m_{max}} = 6.9\ A \rightarrow N_1 = 6\ turns$$

Then:

$$B_{max} = \frac{6.9 \cdot 6 + 0 \cdot 120}{202 \cdot 10^{-6}} \cdot 400 \cdot 10^{-9} = 0.08198\ T = 81.98\ mT \rightarrow B_{max} < B_{sat}$$

2. Energy storage

Having an indirect converter means that our core must store enough energy in the core to release it the second phase of the converter operation. Our energy stored in the leakage inductance would be:

$$E_{stored} = \frac{1}{2} \cdot L_m \cdot I_m^2 = \frac{1}{2} \cdot 14.4 \cdot 10^{-6} \cdot 6.9^2 = 3.42 \cdot 10^{-4}\ J \qquad (4.31)$$

The energy stored in a core is calculated as showed next:

$$W = \iiint_{vol} \bar{B} \cdot \bar{H}\, dV = \iiint_{vol} \overline{B_c} \cdot \overline{H_c}\, dV + \iiint_{vol} \overline{B_g} \cdot \overline{H_g}\, dV \tag{4.32}$$

$$W = W_c + W_g = \frac{B_c^2}{\mu_c} \cdot (A_c \cdot l_c) + \frac{B_g^2}{\mu_0} \cdot (A_g \cdot g)$$

We know that $\mu_0 \ll \mu_c$, so the major part of the energy will be stored in the gap. That is the reason why we chose a gapped core. Knowing that we can consider the following assumption:

$$W_g \gg W_c \rightarrow W \approx W_g = \frac{B_g^2}{\mu_0} \cdot (A_g \cdot g)$$

Now it is time to calculate the average magnetic field going across the gap, the storage time is the one in which the current is only flowing in the primary while the current in the secondary windings is zero. This is be the real case when the magnetizing inductance will store energy:

$$\Phi = i_1 \cdot N_1 \cdot A_L = I_m \cdot N_1 \cdot A_L = 6.9 \cdot 6 \cdot 400 \cdot 10^{-9} = 16.56 \cdot 10^{-6}\, Wb$$

$$B_g = \frac{\Phi}{A_g} \rightarrow A_g \approx A_e \rightarrow B_g = \frac{16.56 \cdot 10^{-6}}{202 \cdot 10^{-6}} = 81.98\, mT$$

$$W_g = \frac{(8.198 \cdot 10^{-2})^2}{\mu_0} \cdot (202 \cdot 10^{-6} \cdot 430 \cdot 10^{-6}) = 4.645 \cdot 10^{-4}\, J$$

With those equations we obtain that $W_g > E_{stored}$ so the core will be able to store enough energy in our converter.

3. Space to wind the wire

Before winding the wires, we have to make sure they fit inside the core. First of all, we need to know the cross-sectional area of the primary and secondary windings. According to the maximum current flowing through them ($i_{m_{max}}$ and $i_{D_{max}}$ respectively) and an increase of temperature of 20ºC chosen for security reasons, we obtain with Figure 37 the wires needed in each side of the transformer:

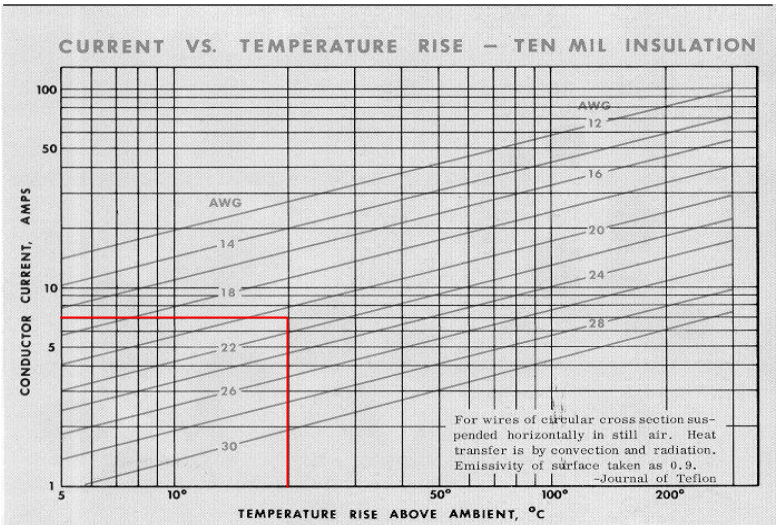

Fig. 36. Current-Temperature correlation for wire selection [6].

For the windings of the primary, as shown in the graph, we will have a maximum current of 6.9 Amps, so we choose a 22 AWG (American Wire Gauge); for the windings in the secondary, we will have a very small current not even reaching the 0.5 Amps, so a 28 AWG should be fine. Converting those units into the International System we get:

$$22\ AWG = 0.3255\ mm^2$$

$$28\ AWG = 0.0810\ mm^2$$

With that areas and assuming the spaces between the wires, we will consider that there is enough space if the packing factor K_f is less than 50%:

$$A = 120 \cdot 0.0810 + 6 \cdot 0.3255 = 11.67\ mm^2 \tag{4.33}$$

The area of the core's window can be obtained with the dimensions of it attached in the correspondent annex:

$$A_w = \frac{29.6 - 16.5}{2} \cdot 14.4 = 94.32\ mm^2 \tag{4.34}$$

$$\frac{A}{A_w} = K_f \rightarrow K_f = \frac{11.67}{94.32} = 0.124 < 0.5 \rightarrow Constraint\ satisfied \tag{4.35}$$

4. Core losses

Having low losses in the core is a crucial aspect of our transformer as we want the best possible efficiency for our converter. Iron has higher saturation values than the ferrite and could have been a good option to have lower constraints in that aspect, however, the way ferrite is made makes this material optimal to reduce core losses.

First of all, we need to understand what the Eddy or Foucault currents are. These are currents flowing in a loop inside the core, induced by changing magnetic fields [7]. We will reduce losses coming from that currents by selecting a 3C81 core material, a kind of ferrite. Ferrite is a ceramic material composed of Fe_3O_2, and mixed with other metallic elements [8], that has a state of powder and it is adhered with an agglutinant. Its powder nature avoids the creation of those Eddie currents decreasing the losses within the core.

Losses will come from Eddie currents formations and the hysteresis, which is the empiric formula measuring that losses is showed in equation 4.36:

$$P_V = K \cdot f^{\alpha} \cdot \hat{B}^{\beta} \left[\frac{W}{m^3}\right] \tag{4.36}$$

As the constants for that formula are hard to find, we will use a datasheet obtained from [9] to measure our core losses with a regression graph in Figure 38.

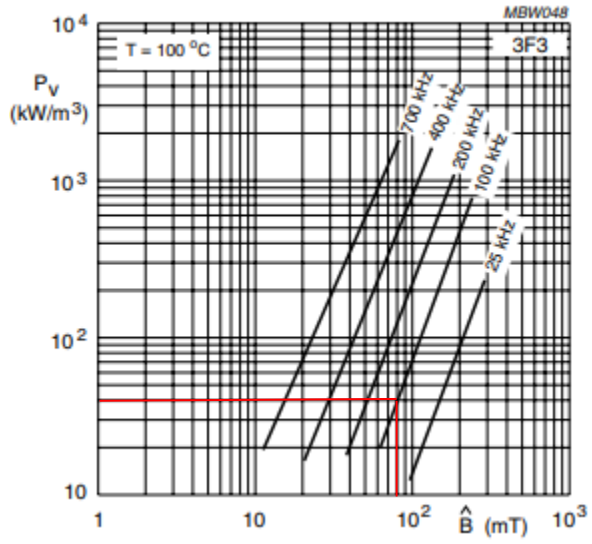

Fig. 37. Regression curve for the core losses [9].

With a peak magnetic field in our core of around 82 mT, and a switching frequency of 100 kHz we obtain a power loss of 40 $\frac{kW}{m^3}$, then our net losses are:

$$P_{core} = P_V \cdot V_e = 40 \cdot 10700 \cdot 10^{-9} = 428\, mW \tag{4.37}$$

With the resources available and the operating switching frequency, this was the best option for our transformer design despite the high core losses in comparison to the input power. However, this core does not have huge loses and will be suitable to be used in our converter.

5. Conduction losses

The last point to take into account in our transformer is the power loss due to the internal resistance of the wires. Our wires are made of copper as usual and with their resistivity, length, cross-sectional area and current flowing we can compute the power loss in that copper:

$$\rho_{Cu} = 1.71 \cdot 10^{-8}\, \Omega \cdot m \rightarrow At\ 25°C$$

$$A_{pri} = 0.3255\ mm^2; A_{sec} = 0.0810\ mm^2$$

$$l_{pri} = N_1 \cdot 2\pi \mathrm{R} = 6 \cdot 2\pi \cdot \frac{16.5}{2 \cdot 1000} = 0.311\ m$$

$$l_{sec} = N_2 \cdot 2\pi R = 120 \cdot 2\pi \cdot \frac{16.5}{2 \cdot 1000} = 6.22\ m$$

$$I_{pri} = I_m = 4.6;\ I_{sec} = I_D = 0.115$$

Then the calculated losses are:

$$P_{pri} = 4.6^2 \frac{1.71 \cdot 10^{-8} \cdot 0.311}{0.3255 \cdot 10^{-6}} = \ 345\ mW \tag{4.38}$$

$$P_{sec} = 0.115^2 \cdot \frac{1.71 \cdot 10^{-8} \cdot 6.22}{0.0810 \cdot 10^{-6}} = 17.36\ mW \tag{4.39}$$

$$P_{cond} = P_{pri} + P_{sec} = \ 362.36\ mW$$

We obtain a notable power loss in the copper due to the high current flowing through the primary windings.

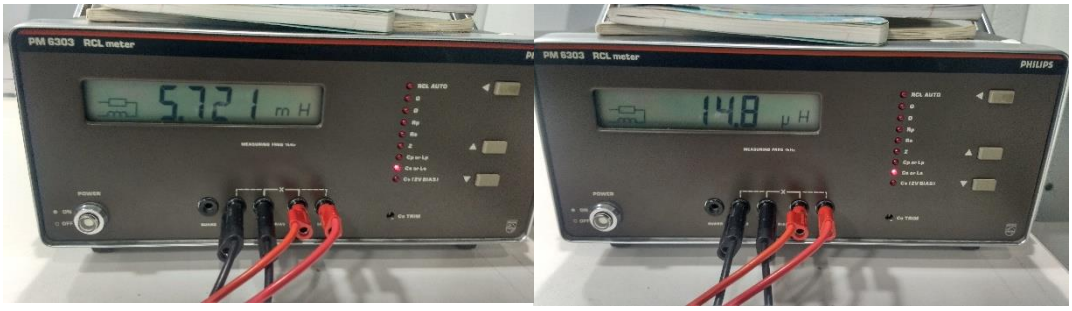

Fig. 38. Measurements of the inductances of the transformer.

The transformer built was tested to ensure that it satisfy our needs for the converter, and these are the readings of the measurement devices shown in Figure 39.

These inductance readings for the primary and secondary side of the transformer (lower value corresponds to the primary side), can show us if the turns ratio is the one desired of if we winded the transformer incorrectly.

$$\frac{L_{sec}}{L_{pri}} = N^2 \rightarrow N = \sqrt{\frac{5.721}{14.8 \cdot 10^{-3}}} = 19.66 \tag{4.40}$$

The expected value for the turns ratio is 1:20 so this transformer is suitable for building our design. To check the behavior of the core with the transformer, we did another test with sinusoidal waves. This is shown in figure 40.

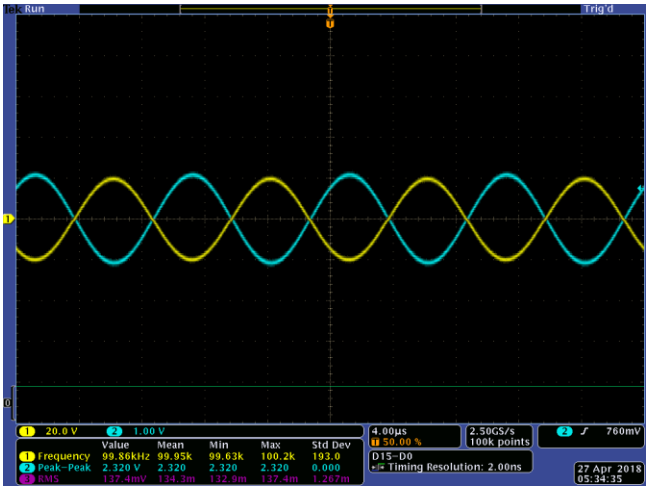

Fig. 40. Transformer input and output sinusoidal waveforms.

With the scales chosen (20 V/div and 1 V/div) for each side of the transformer and the size of the waveforms we check that one sine is twenty times bigger than the other one, which is satisfactory.

4.11. Efficiency analysis

Here, we are going to make a first estimation of the quantity of our losses due to component dissipation. We have calculated some of them, but others are missing yet. First, we will deal with the diodes conduction losses.

We know that the characteristic losses of the diodes come from its forward voltage times the current that flows through them. From our datasheets and points of operation we get those values. On average, both diodes have an induced forward voltage of 1 V.

$$P_{diodes} = V_{fw} \cdot I_{clamp} + V_{fw} \cdot I_D \approx V_{fw} \cdot I_D \tag{4.41}$$

We can ignore the losses in the clamping diode as the current flowing there is almost a pulse in a small period of time, making the average current almost negligible.

$$P_{diodes} = 1 \cdot \frac{190}{1652} = 115\ mW$$

The last missing element dissipating power in our converter is the MOSFET, not only due to conduction issues, but because the switching frequency.

$$P_{cond} = I_{SW}^2 \cdot D \cdot R_{Dd_{on}} = 2.3^2 \cdot 0.5 \cdot 0.27 = 714\ mW \tag{4.42}$$

For the case of the switching losses we have the following equation:

$$P_{sw} = \frac{1}{2} \cdot V_{sw} \cdot I_{sw} \cdot \left(t_f + t_r\right) \cdot f_{sw} \tag{4.43}$$

According to our datasheets we have a t_r of 30 nanoseconds and a t_f of 20 nanoseconds. In addition, with the other parameters we obtain:

$$P_{sw} = \frac{1}{2} \cdot 19 \cdot 2.3 \cdot (30 + 20) \cdot 10^{-9} \cdot 100 \cdot 10^3 = 109\ mW$$

The sum of conduction and switching losses is lower than the maximum dissipated power that can withstand the MOSFET of 60 Watts, this means that it will not overheat, and it is safe to operate with it.

The total losses in our circuit will be:

$$P_{loss} = P_{core_{transformer}} + P_{Cu_{transformer}} + P_{cond_{diode}} + P_{sw} + P_{cond_{sw}} + P_{clamp} \qquad (4.44)$$

$$P_{loss} = 428 + 362.36 + 115 + 109 + 714 + 82 = 1.81\ Watts$$

The efficiency of our converter in the maximum load operation will be:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{loss}}{P_{in}} = \frac{21.85 - 1.81}{21.85} = 0.917 \rightarrow \eta = 91.7\%$$

This gives a reasonable value meaning that our converter is feasible to be constructed and implemented. We have to take into consideration that this efficiency is given at a maximum load point and if we operate at a lower current condition those losses percentage will increase.

5. Simulation

For this section, we decided to write the code and design the simulation model with Matlab and more specifically, one of its extensions called Simulink. This model is shown in Figure 41.

The left part of the model represents the PV panel, and has the functionality of calculating the equivalent resistance, and with that, produce the current and voltage expected. The voltage will be read by the Simscape blocks (Matlab circuitry library) and will simulate the rest of the parameters. Continuing with the analysis of the circuit, we can notice there are several scopes that will show us the behaviors of our components and another special thing is the blocks in the top right that are used to measure power in the output of our converter. They receive the voltage and current data in arrays and multiply them to obtain the power vector, then in our Matlab code, we calculate the median of that vector to know the power drained by the load.

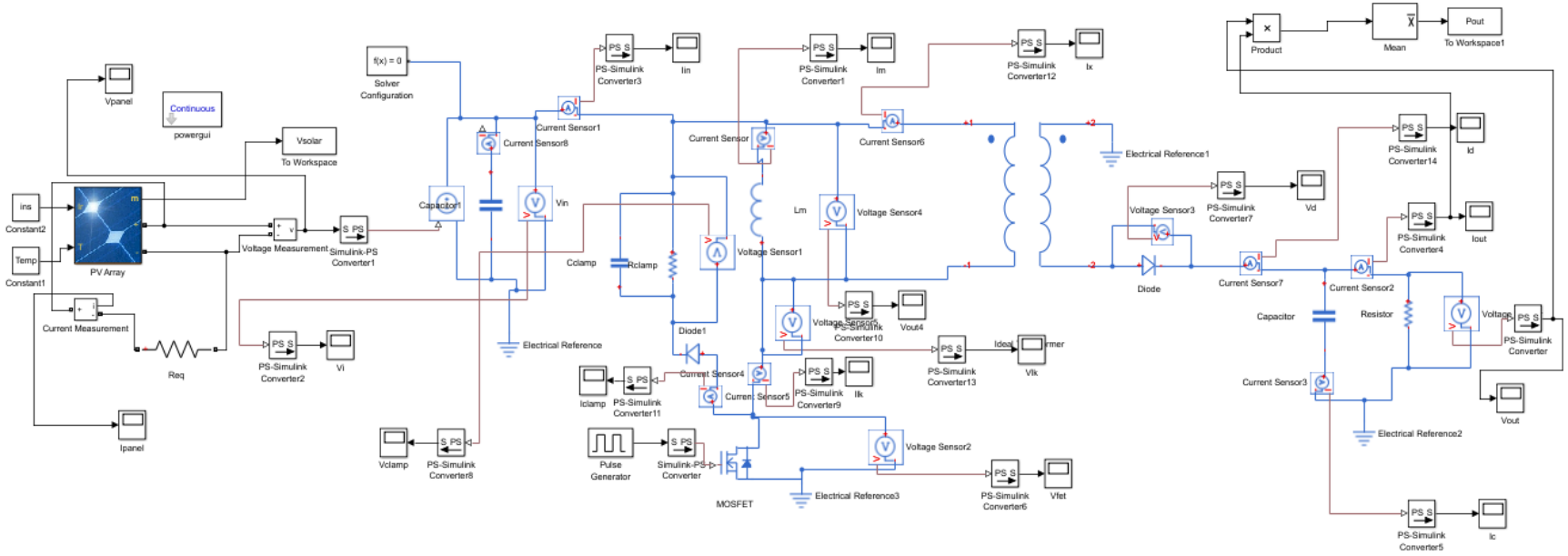

Fig. 41. Simulation model in Simulink.

The PV array block placed on the left of the model runs the simulation imitating the characteristics of the panel that will be used to test the real converter. Those characteristics are also shown in the graphs used to calculate the components' parameters are:

$$V_{oc} = 12\ V\ ; I_{sc} = 2.5\ A$$

$$V_{MPP} = 9.5\ V\ ; I_{MPP} = 2.3\ A \rightarrow P_{MPP} = 21.85\ W$$

Now, addressing the simulation of our converter, we have to take into account that it will be under Standard Test Conditions which means we will assume that the solar panel would be receiving an irradiation of 1 kW/m^2 and with a panel temperature of 25℃. This forces the panel to operate at the MPP at 9.5 Volts and around 2.3 Amps. The graphs representing those parameters are showed in Figure 42.

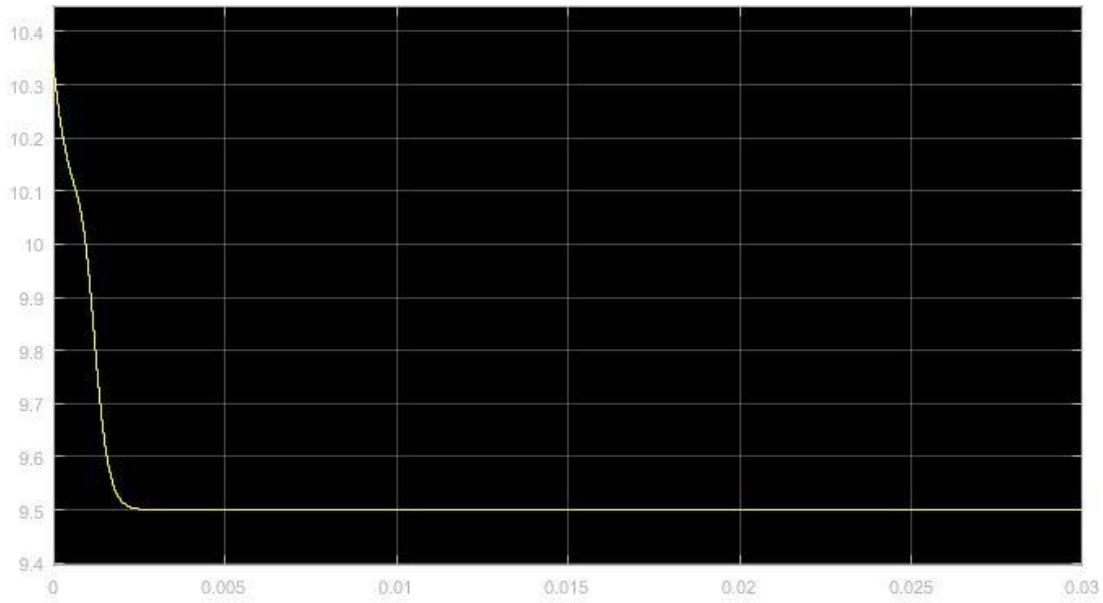

Fig. 42. Input voltage in the simulation.

Figure 43 showing the current flowing towards the transformer is not as smooth as the input voltage, but more detail will be given to notice its waveform.

It has the waveform expected showed in figure 33 with the name of i_1. We can extract the average value with the help of cursors that are showed in Figure 43. This is achieved by calculating the area of one half-wave and dividing it by the switching period.

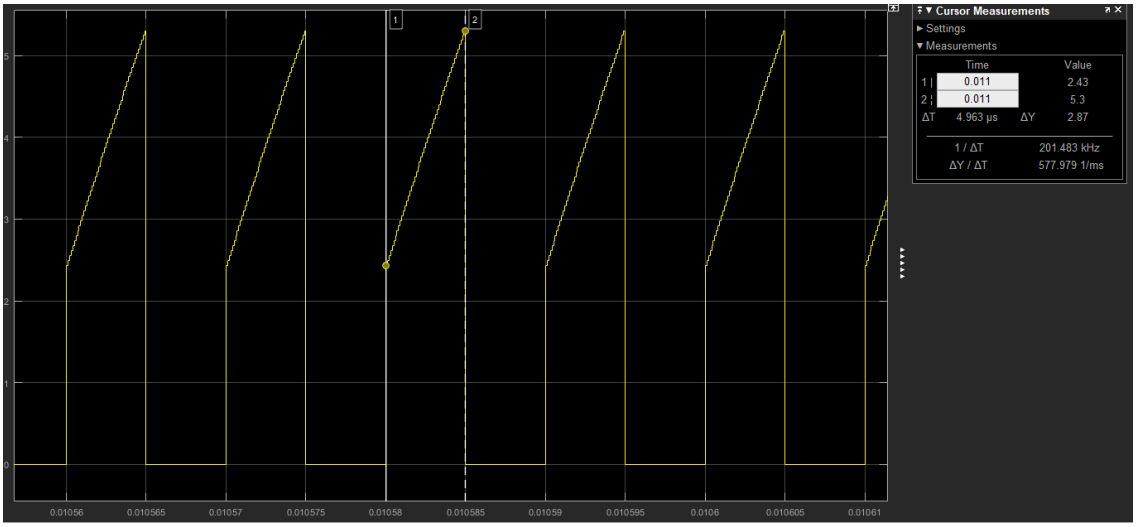

Fig. 43. Input current in the simulation.

With the values obtained with the cursors, we can deduce the average value of the current shown. That value should be near the input current of the solar panel of 2.3 A.

$$I_1 = \frac{4.963 \cdot 2.43 + 0.5 \cdot 4.963 \cdot 2.87}{10} = 1.92\ A \tag{5.1}$$

As we see, that value is very close to the 2.3 A expected, but not an exact value due to a commutation period (showed in the pulse width different from 5 µs) that will be explained when analyzing the leakage inductor current, and in addition, the dissipation losses occurred in the diodes and the transistor as they are included in the simulation.

Now let us take a look at the magnetizing current as one of the core parameters driving our converter in Figure 44.

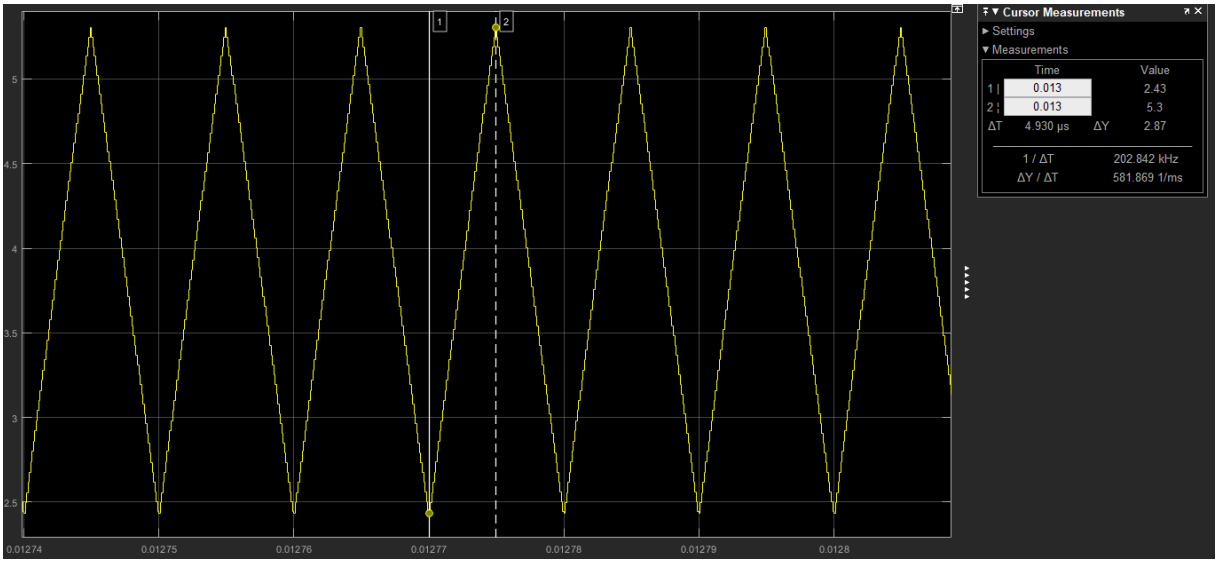

Fig. 44. Ripple current in the magnetizing inductor.

It follows the scheme deducted when calculating the magnetizing inductance but with different values because as now we have real parameters instead of ideal conditions we should not expect to receive the values desired. Calculating the average value and the percentage of ripple is an example of that.

Using the values showed with the cursors of figure 44:

$$I_m = 5.3 - \frac{2.87}{2} = 3.865\ A \tag{5.2}$$

$$\%_{ripple} = \frac{5.3 - 3.865}{3.865} = 0.371 \rightarrow 37.1\% \tag{5.3}$$

Both I_m and the percentage of ripple are going to be lower than expected, the average magnetizing current is normal to be reduced because all currents will decrease due to power losses in our components. In the case of the percentage of ripple, it is smaller because of the slight drop in the duty ratio due to commutation times and the increase of the magnetizing inductance because after building the transformer we obtained a higher value as showed in its section. Even though they are not our expected

values, the percentage of ripple is favorable to be lower being beneficial to our output voltage ripple as it will decrease because of that.

Now taking a look at the leakage current, we can understand anomalies in our simulation with respect to the ideal conditions. Our expected leakage current in comparison with the magnetizing one is as represented in Figure 45:

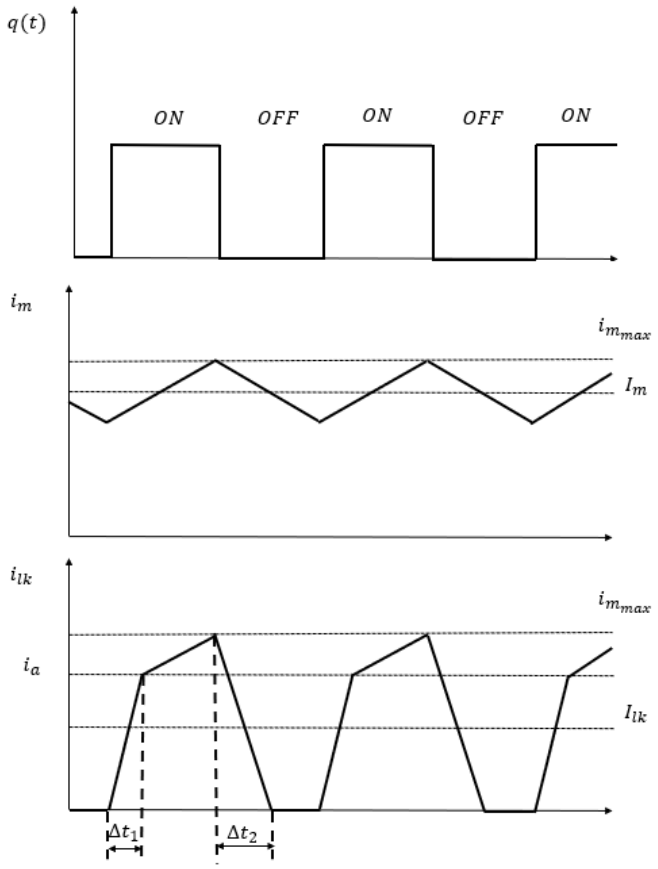

Fig. 45. Theoretical leakage current compared to the magnetizing current and the duty ratio.

As shown, the leakage inductor needs to charge and discharge when the FET changes its state. The increasing ramp happens when the transistor turns on and the leakage current increases until it reaches the value of i_m, at this point both inductors share the same current. When the FET turns off, the leakage current is discharged with the clamping circuit until it reaches zero, and the current in the secondary windings of the transformer reaches its normal value. The value of the charging and discharging times is

calculated with the voltage seen by the leakage inductor at every moment, and the maximum current that the ramps will produce:

$$\Delta t_1 = \frac{L_{lk} \cdot i_a}{\left(\frac{V_2}{n} + V_1\right)} \tag{5.4}$$

$$\Delta t_2 = \frac{L_{lk} \cdot i_{m_{max}}}{\left(V_{clamp} - \frac{V_2}{n}\right)} \tag{5.5}$$

The commutation time in which both the rectifying diode and the FET are turned on is Δt_1 because the leakage inductor does not let the current increase to reach the value of the magnetizing current instantaneously making the diode in the secondary conduct until it charges completely. In the case of Δt_2, The FET turns off as we decide to do so, and the current goes to the clamping circuit, not presenting a commutation period. That commutation time makes the effective duty ratio decrease as the rectifying diode blocks the output voltage less time increasing the period in which the magnetizing inductor sees that output voltage. This pulse reduction will affect our output as this converter is very sensible to small changes in the duty ratio. Figures 46 and 47 show the analysis of this event.

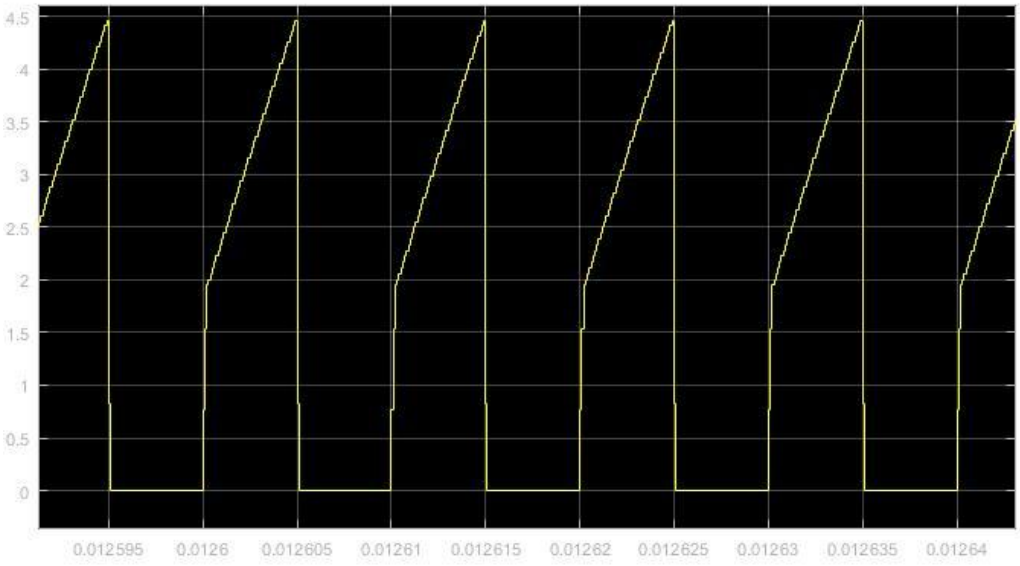

Fig. 46. Simulated current through the leakage inductance.

A slight slope in the beginning and ending of the waveform can be seen. The times are very small, and the maximum step applied for the simulation is small, but we would need a smaller one to see that slope correctly. However, this would result in very high simulation times and the important thing is to notice that ramp.

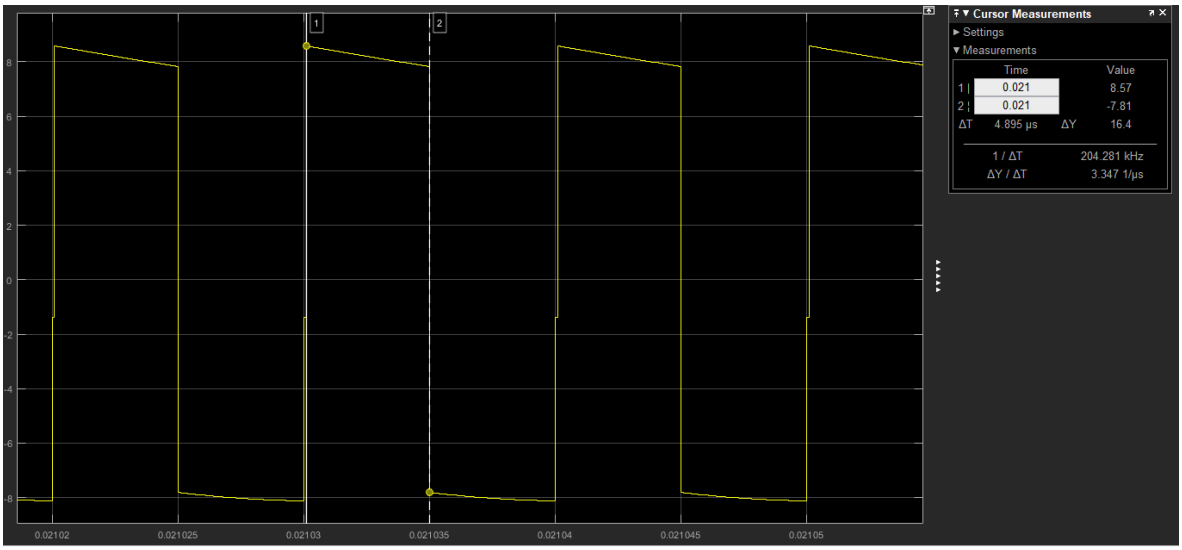

Fig. 47. Simulated voltage across the magnetizing inductance.

In Figure 47 we see how the pulse is reduced to a duty ratio of 0.4895 instead of 0.5, this could appear to be negligible but in practice that makes the output voltage change a lot. In addition, we will consider the effect of the leakage inductor in the transfer function to derive which is the expected output voltage without the losses taken into account.

$$\frac{V_{out}}{V_{in}} = \frac{n \cdot D}{1 - D} \cdot \frac{L_m}{L_m + L_{lk}} \rightarrow Derived\ in\ section\ 3$$

With our parameters:

$$\frac{V_{out}}{V_{in}} = \frac{n \cdot D}{1 - D} \cdot \frac{L_m}{L_m + 0.03 \cdot L_m} = \frac{n \cdot D}{1 - D} \cdot \frac{1}{1.03}$$

$$V_{out} = 9.5 \cdot \frac{20 \cdot 0.4895}{1 - 0.4895} \cdot \frac{1}{1.03} = 176.88\,V$$

Ideally, we expect to have 190 Volt in the output of our converter, so this makes a big difference in terms of voltage drop. Our simulated converter output with losses is depicted in Figure 48.

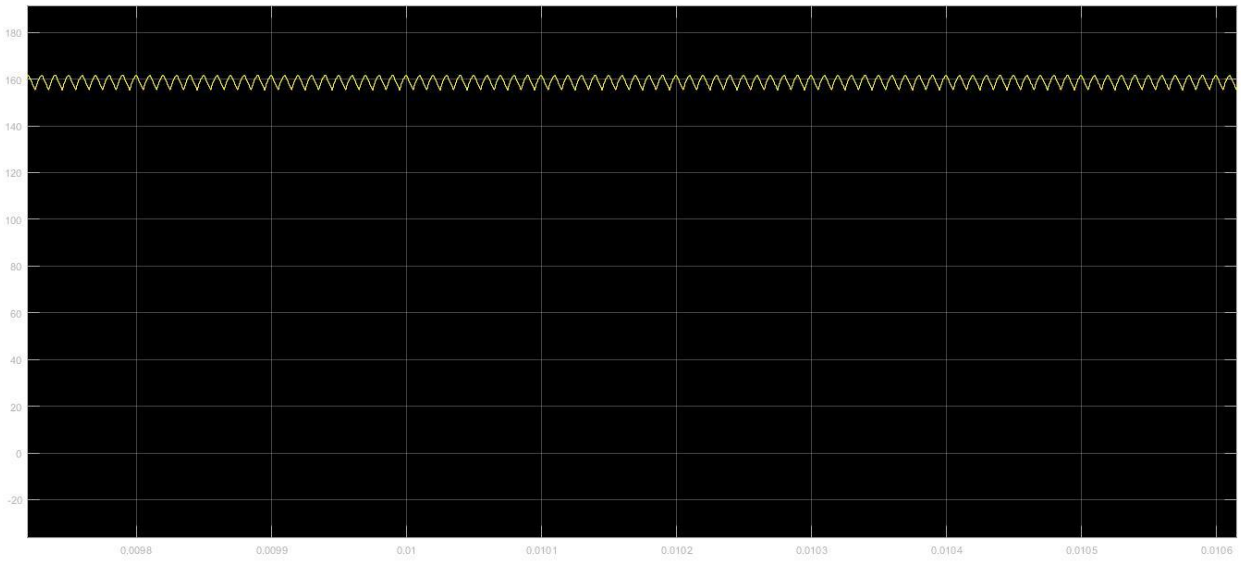

Fig. 48. Simulated output voltage.

We obtain a value of around 160 Volts which means a voltage drop of 30 Volts with respect the ideal conditions. Addressing the voltage ripple, we take a look to that waveform with more detail. The decrease from the 177 Volts to the 160 Volts is mainly caused by the dissipation losses in the components.

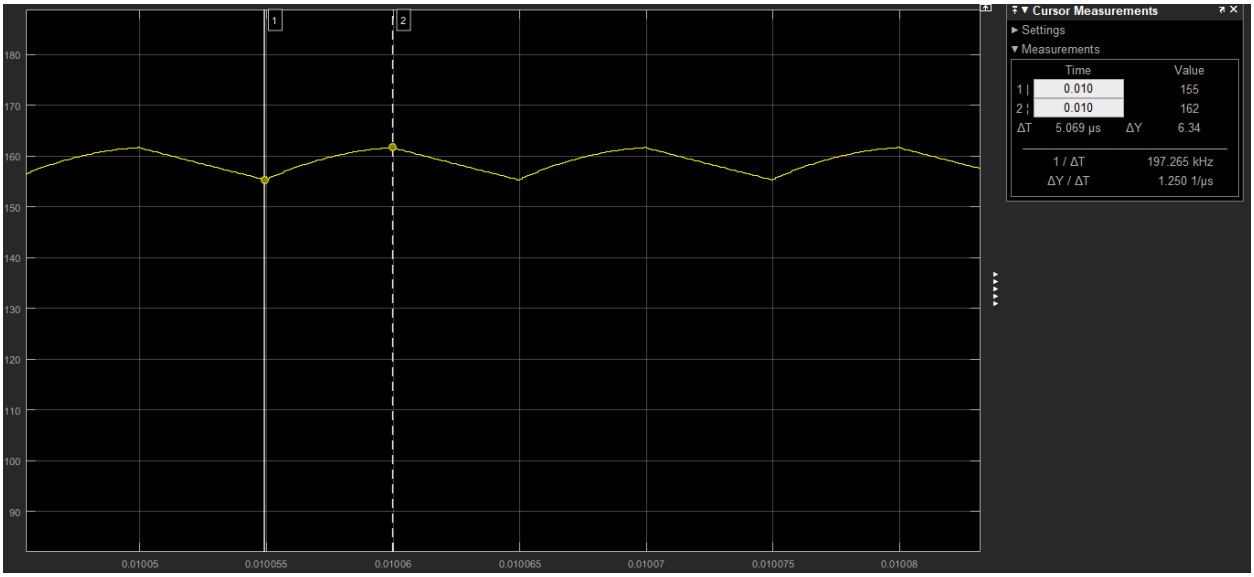

Fig. 49. Simulated output voltage ripple in more detail.

$$\%_{ripple} = \frac{\frac{6.34}{2}}{160} = 0.0198 = 1.98\% \tag{5.6}$$

We designed it to be a 2%, the change in the output voltage making it smaller would negatively affect the ripple but together with the decrease in the magnetizing ripple current we have improved the percentage of output voltage ripple.

That waveform follows two tendencies, when the capacitor charges it is parabolic and when it discharges it is a ramp. This is caused because in the time when the capacitor charges, the current entering the output node comes from the inductor and it has a ramp, and as the capacitor voltage is ruled with the derivative of that signal, it creates a parabolic waveform. On the other hand, when the capacitor discharges, the rectifying diode is turned off and the capacitor discharges with an approximate constant current.

Another waveform to consider is the clamping voltage as the safety of our MOSFET depends on it, shown in Figure 50.

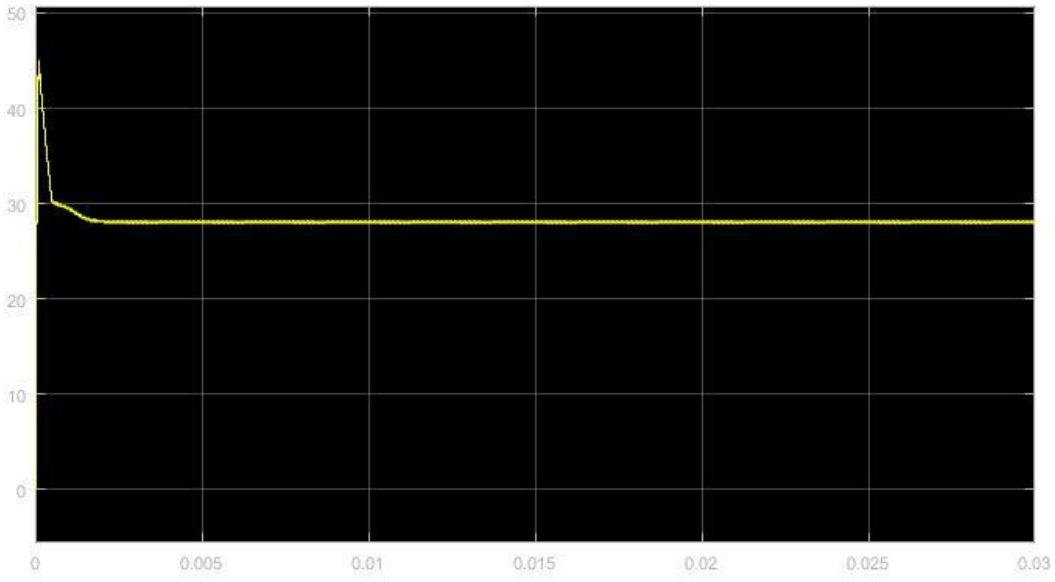

Fig. 50. Simulated clamping voltage.

We obtain the expected value of around 28 V with low ripple as designed in section 4. This means that the voltages peaks in the MOSFET will be as calculated and it will work properly.

If we take our converter as ideal without leakage inductance and without power losses in the components, we obtain the desired values as showed in Figure 51.

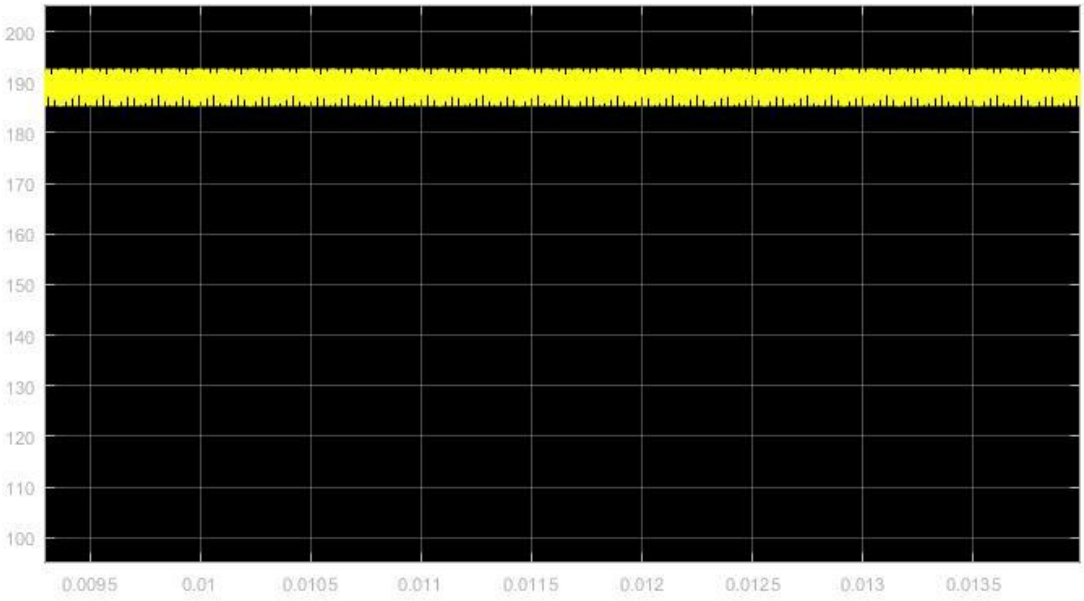

Fig. 51. Simulated output voltage with ideal components.

In Figure 51 is shown that the output voltage would be the 190 Volts expected so this means our simulation is running correctly. The problem with the drop in the output voltage due to real components could be solved by increasing the duty ratio, meaning that the effective value of it reaches the required value reestablishing the equivalent resistance value with the maximum power extracted.

6. Results.

We made the simulations at a low load condition to maintain a level of safety and avoid failures in the components. We tried to pack the whole circuit in order to reduce losses and parasitic inductances in it. The clamp circuit is placed as close as possible to the MOSFET to try to avoid parasitic inductances in the clamp circuit, which would be very bad for the functioning of the transistor and the converter. The connection of the circuit is the one showed in figure 52:

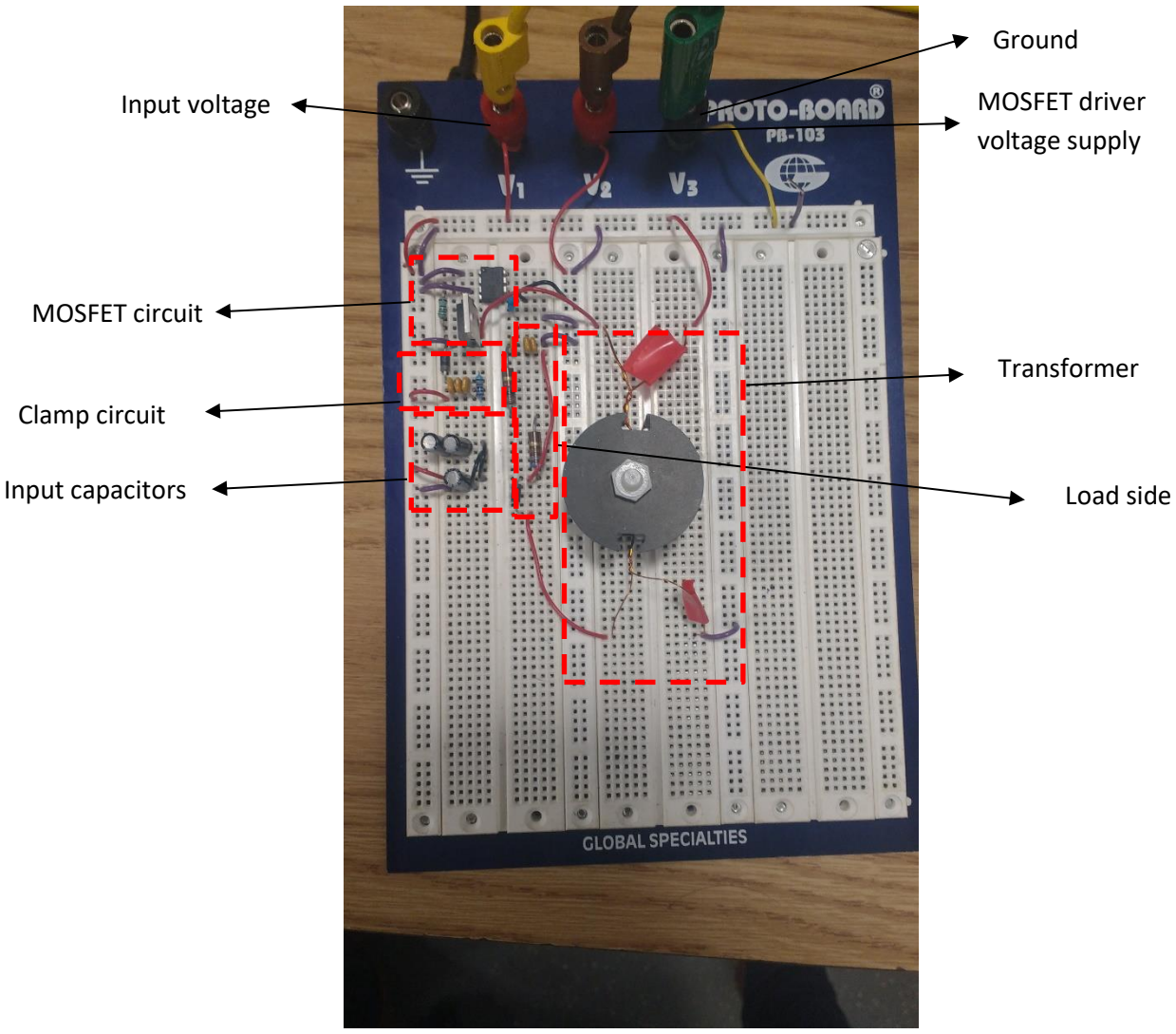

Fig. 52. Circuit design with each part described.

We did a test with 1.5 Volts in the input and a duty ratio of 0.5, this would lead to 30 Volts in the output theoretically, but in our case the output voltage obtained is the following represented in Figure 53.

Fig. 53. Output voltage obtained in the test.

We obtained 20 Volts in the output and we have to consider another thing. It seems that the voltage discharges when the FET is on because the blue signal shows the input signal of the gate driver, this would be contrary to what we deduced before in this project. The reality is that the MOSFET driver that we chose has the input signal negated so when the blue signal is up, the driver would be down. This makes our output voltage make sense.

Despite the fact that our converter gives a reasonable output voltage, the operation is not as good as it seems (despite having 10 Volts less than expected). If we analyze the other parameters in the circuit, we notice that the MOSFET is not operating as it should. This is the most important component of the converter with the transformer. If the transistor cannot block the voltage completely, we would have a voltage drop in the magnetizing inductance reducing our output voltage.

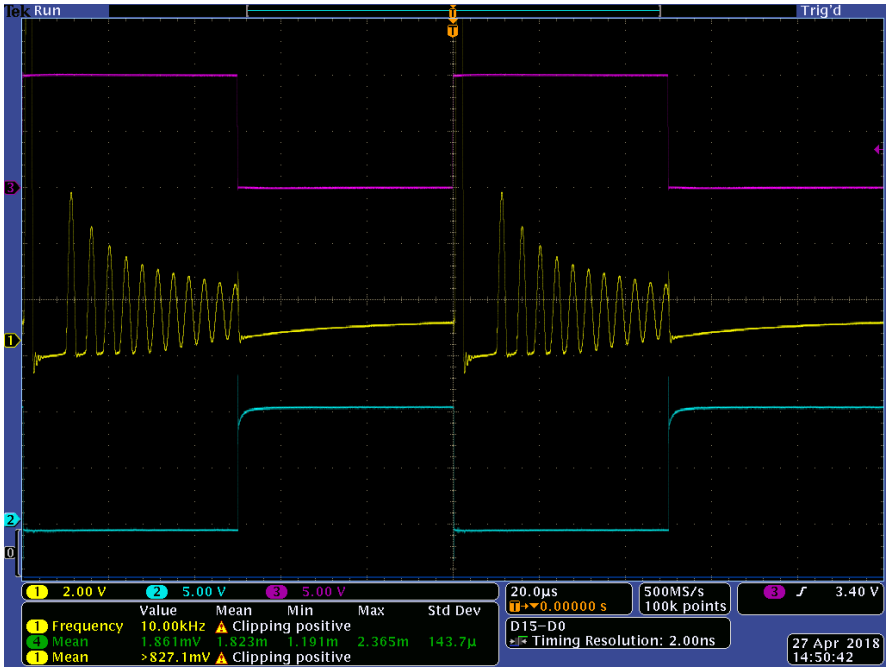

Fig. 54. Showed in purple the input signal of the drive, in blue the gate driver output signal and in yellow the voltage across the FET.

It is depicted in Figure 54 what is mentioned above, the input signal of the gate driver is the complementary of the output signal of that component. Now looking at the voltage across the FET, we realize that it is not blocking the current and voltage properly and at every moment it has some kind of voltage drop less than the input voltage of the circuit. Another strange operation of the driver-MOSFET pair is that when we increase the logic supply, the gate voltage increases until a point in which it seems to saturate.

This phenomenon changes a little when modifying some parameters of the driver such as the gate resistor or the load in some cases but overall that voltage limit in which it saturates does not vary so much. We tried to change the driver to others and even to ones designed for low level switches, but we did not manage to solve the problem. As shown in the driver's datasheet, this device can work with a logic supply of 20 Volts and a logic input voltage of 5 Volts. Applying the values recommended for the logic input supply but only around 15 Volts in the logic supply we obtained the waveforms shown in figure 55.

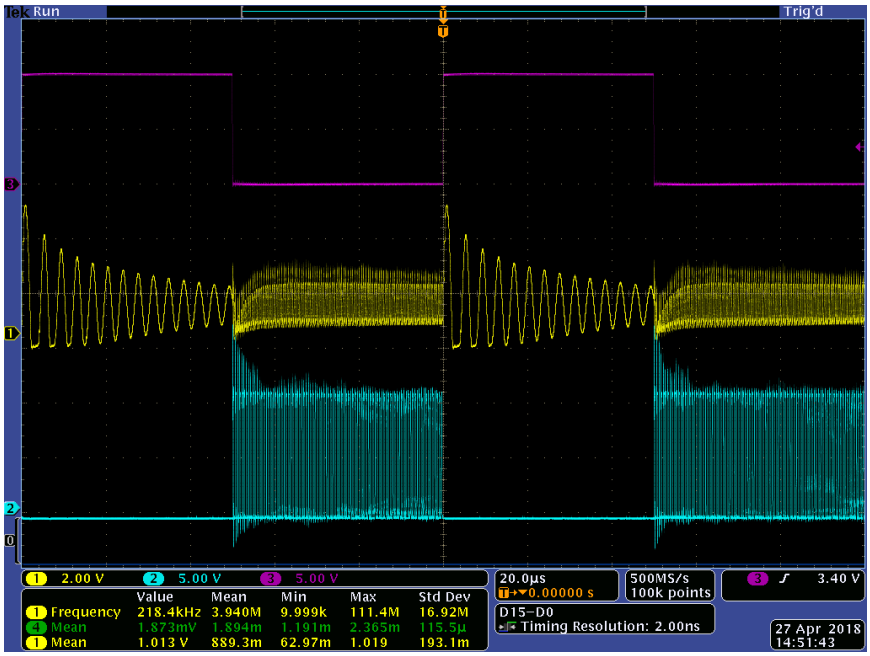

Fig. 55. Loss of pulse issue when the logic supply surpasses a voltage level despite being below its maximum value.

We tried to drive the FET alone with a resistor, but the same issue happens, it seems to fail when trying to open the gate and close. As the gate voltage follows a reasonable waveform to open and close the gate the problem should be the connection of the MOSFET proposed. The passives of our converter work properly as tested and shown in the transformer operation for example. When fixing the FET problem, the converter is expected to work properly. More work in this component will be done to drive it correctly permitting the voltage pulses in the transformer windings. The tight deadlines did not allow the problem to be solved but it will be addressed despite not being included in this thesis.

7. Conclusion.

Throughout the project, we have seen the benefits of using these types of converters to increase efficiency in solar panels. Nowadays, with the great increase in renewable generation and the solar PV potential, it is crucial to find new ways to improve our energy systems to compete with conventional energy resources such as coal, that are polluting at dangerous levels. Despite not managing to drive our converter properly in the tests, this converter proved to operate well as we use it in domestic electronic devices every day, but it would need more work to be fully developed to be used in other fields.

Next steps in this project are vital to making it feasible to be implemented in PV solar systems. They would include:

- Error fixing regarding the MOSFET drive to make the converter transfer energy properly in order to transform voltage in the desired levels.
- Study which type of control improves response times in this converter and would perform better in real applications.
- Development of the control of the Flyback converter.
- Development of the subsystems' interconnection control that would drive the system as a whole. Knowing the points of operation of each converter at every time, and their components, fixing parameters would improve even more efficiency.
- More in-depth research to reduce losses in our device. This would be done with an optimal component selection such as the transformer whose core had limited availability for us.
- Build a higher power Flyback converter to be attached to utility-level PV modules.
- Test the converter with a real PV panel at different points of operation to fix errors and prepare it for its real implementation.

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Appendix A. Recommended abbreviations.

Symbol or Abbreviation	Unit or Term
MPPT	Maximum Power Point Tracking
MPP	Maximum Power Point
V	Volt
A	Amp
Ω	Ohm
F	Farads
H	Henry
Wb	Webber
T	Tesla
AWG	American Wire Gauge
I_m	Average magnetizing current
i_m	Instantaneous magnetizing current
I_{lk}	Average leakage current
i_{lk}	Instantaneous leakage current
I_{in}	Average input current
i_{in}	Instantaneous input current
I_{out}	Average output current
i_{out}	Instantaneous output current

Symbol or Abbreviation	Unit or Term
V_{out}	Average output voltage
V_{clamp}	Average voltage in the clamp
Φ	Magnetic flux
B	Magnetic field density
R_c	Reluctance of the core
R_g	Reluctance of the gap
D	Duty ratio
I_D	Average current in the rectifying diode
i_D	Instantaneous current in the rectifying diode
I_c	Average current in the output capacitor
i_c	Instantaneous current in the output capacitor
V_{in}	Average input voltage

Appendix B. Datasheets.

In this appendix we will attach the datasheets of the components used in this project for the converter's design.

Surface Mount Multilayer Ceramic Chip Capacitors (SMD MLCCs)

X5R Dielectric, 4 – 50 VDC (Commercial Grade)

Electronic Components
KEMET
CHARGED.

Overview

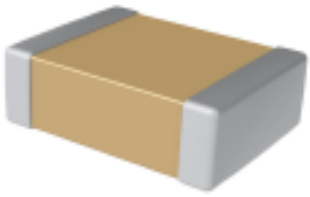
KEMET's X5R dielectric features an 85°C maximum operating temperature and is considered "semi-stable." The Electronics Components, Assemblies & Materials Association (EIA) characterizes X5R dielectric as a Class II material. Components of this classification are fixed, ceramic dielectric capacitors suited for bypass and decoupling applications or for frequency discriminating circuits where Q and stability of capacitance characteristics are not critical. X5R exhibits a predictable change in capacitance with respect to time and voltage and boasts a minimal change in capacitance with reference to ambient temperature. Capacitance change is limited to ±15% from −55°C to +85°C.

Benefits

- −55°C to +85°C operating temperature range
- Lead (Pb)-free, RoHS and REACH compliant
- Temperature stable dielectric
- EIA 0201, 0402, 0603, 0805, 1206, 1210, and 1812 case sizes
- DC voltage ratings of 4 V, 6.3 V, 10 V, 16 V, 25 V, 35 V, and 50 V
- Capacitance offerings ranging from 0.01 µF to 100 µF
- Available capacitance tolerances of ±10% and ±20%
- Non-polar device, minimizing installation concerns
- 100% pure matte tin-plated termination finish allowing for excellent solderability

Applications

Typical applications include decoupling, bypass, and filtering.



Click image above for interactive 3D content

Open PDF in Adobe Reader for full functionality

Ordering Information

C	1206	C	107	M	9	P	A	C	TU
Ceramic	Case Size (L" x W")	Specification/ Series	Capacitance Code (pF)	Capacitance Tolerance	Rated Voltage (VDC)	Dielectric	Failure Rate/ Design	Termination Finish[1]	Packaging/Grade (C-Spec)
	0201 0402 0603 0805 1206 1210	C = Standard	Two significant digits and number of zeros.	K = ±10% M = ±20%	7 = 4 9 = 6.3 8 = 10 4 = 16 3 = 25 6 = 35 5 = 50	P = X5R	A = N/A	C = 100% Matte Sn	See "Packaging C-Spec Ordering Options Table" below

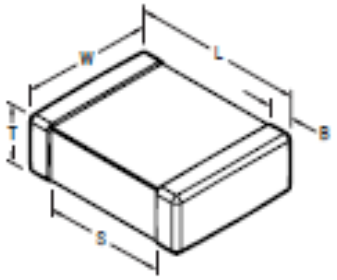
[1] *Additional termination finish options may be available. Contact KEMET for details.*

Packaging C-Spec Ordering Options Table

Packaging Type[1]	Packaging/Grade Ordering Code (C-Spec)
Bulk Bag/Unmarked	Not required (Blank)
7" Reel/Unmarked	TU
13" Reel/Unmarked	7411 (EIA 0603 and smaller case sizes) 7210 (EIA 0805 and larger case sizes)
7" Reel/Marked	TM
13" Reel/Marked	7040 (EIA 0603 and smaller case sizes) 7215 (EIA 0805 and larger case sizes)
7" Reel/Unmarked/2mm pitch[2]	7081
13" Reel/Unmarked/2mm pitch[2]	7082

[1] *Default packaging is "Bulk Bag". An ordering code C-Spec is not required for "Bulk Bag" packaging.*
[2] *The terms "Marked" and "Unmarked" pertain to laser marking option of capacitors. All packaging options labeled as "Unmarked" will contain capacitors that have not been laser marked. Please contact KEMET if you require a laser marked option. For more information see "Capacitor Marking".*
[3] *The 2 mm pitch option allows for double the packaging quantity of capacitors on a given reel size. This option is limited to EIA 0603 (1608 metric) case size devices. For more information regarding 2 mm pitch option see "Tape & Reel Packaging Information".*

Dimensions – Millimeters (Inches)



EIA Size Code	Metric Size Code	L Length	W Width	T Thickness	B Bandwidth	S Separation Minimum	Mounting Technique
0201	0603	0.60 (0.024) ±0.03 (0.001)	0.30 (0.012) ±0.03 (0.001)	See Table 2 for Thickness	0.15 (0.006) ±0.05 (0.002)	N/A	Solder Reflow Only
0402[1]	1005	1.00 (0.040) ±0.05 (0.002)	0.50 (0.020) ±0.05 (0.002)		0.30 (0.012) ±0.10 (0.004)	0.30 (0.012)	
0603	1608	1.60 (0.063) ±0.15 (0.006)	0.80 (0.032) ±0.15 (0.006)		0.35 (0.014) ±0.15 (0.006)	0.70 (0.028)	Solder Wave or Solder Reflow
0805	2012	2.00 (0.079) ±0.20 (0.008)	1.25 (0.049) ±0.20 (0.008)		0.50 (0.02) ±0.25 (0.010)	0.75 (0.030)	
1206[2]	3216	3.20 (0.126) ±0.20 (0.008)	1.60 (0.063) ±0.20 (0.008)		0.50 (0.02) ±0.25 (0.010)	N/A	
1210[3]	3225	3.20 (0.126) ±0.20 (0.008)	2.50 (0.098) ±0.20 (0.008)		0.50 (0.02) ±0.25 (0.010)		Solder Reflow Only

[1] *For capacitance values ≥ 4.7 µF add 0.15 (0.006) to the width and length tolerance dimensions.*
[2] *For capacitance values ≥ 22 µF add 0.10 (0.004) to the positive bandwidth tolerance dimension.*
[3] *For capacitance values ≥ 22 µF add 0.10 (0.004) to the length and width tolerance dimension and add 0.15 (0.006) to the positive bandwidth tolerance dimension.*

Qualification/Certification

Commercial Grade products are subject to internal qualification. Details regarding test methods and conditions are referenced in Table 4, Performance & Reliability.

Environmental Compliance

Lead (Pb)-free, RoHS, and REACH compliant without exemptions.

Electrical Parameters/Characteristics

Item	Parameters/Characteristics
Operating Temperature Range	-55°C to +85°C
Capacitance Change with Reference to +25°C and 0 Vdc Applied (TCC)	±15%
[1]Aging Rate (Maximum % Capacitance Loss/Decade Hour)	5.0%
[2]Dielectric Withstanding Voltage (DWV)	250% of rated voltage (5±1 seconds and charge/discharge not exceeding 50mA)
[3]Dissipation Factor (DF) Maximum Limit at 25°C	See Dissipation Factor Limit Table
[4]Insulation Resistance (IR) Minimum Limit at 25°C	See Insulation Resistance Limit Table (Rated voltage applied for 120±5 seconds at 25°C)

[1]Regarding Aging Rate: Capacitance measurements (including tolerance) are indexed to a referee time of 48 or 1,000 hours. Please refer to a part number specific datasheet for referee time details.

[2]DWV is the voltage a capacitor can withstand (survive) for a short period of time. It exceeds the nominal and continuous working voltage of the capacitor.

[3]Capacitance and dissipation factor (DF) measured under the following conditions:

1 kHz ±50 Hz and 1.0 ±0.2 Vrms if capacitance ≤ 10 µF

120 Hz ±10 Hz and 0.5 ±0.1 Vrms if capacitance > 10 µF

[4]To obtain IR limit, divide MΩ-µF value by the capacitance and compare to GΩ limit. Select the lower of the two limits.

Note: When measuring capacitance it is important to ensure the set voltage level is held constant. The HP4284 and Agilent E4980 have a feature known as Automatic Level Control (ALC). The ALC feature should be switched to "ON."

Post Environmental Limits

High Temperature Life, Biased Humidity, Moisture Resistance					
Dielectric	Rated DC Voltage	Capacitance Value	Dissipation Factor (Maximum %)	Capacitance Shift	Insulation Resistance
X5R	> 25	< 1.0 µF	7.5	±20%	10% of Initial Limit
		≥ 1.0 µF	20.0		
	25	< 2.2 µF	7.5		
		≥ 2.2 µF	20.0		
	< 25	< 0.56 µF	7.5		
		≥ 0.56 µF	20.0		

Dissipation Factor Limit Table

Rated DC Voltage	Capacitance	Dissipation Factor (Maximum %)
> 25	< 1.0 µF	5.0
	≥ 1.0 µF	10.0
25	< 2.2 µF	5.0
	≥ 2.2 µF	10.0
< 25	< 0.56 µF	5.0
	≥ 0.56 µF	10.0

Insulation Resistance Limit Table

EIA Case Size	1,000 Megohm Microfarads or 100 GΩ	500 Megohm Microfarads or 10 GΩ	100 Megohm Microfarads
0201	N/A	ALL	N/A
0402	< .012 µF	≥ .012 µF < 1.0 µF	≥ 1.0 µF
0603	< .047 µF	≥ .047 µf < 1.0 µF	≥ 1.0 µF
0805	< 0.15 µF	≥ 0.15 µF < 1.0 µF	≥ 1.0 µF
1206	< 0.47 µF	≥ 0.47 µF < 1.0 µF	≥ 1.0 µF
1210	< 0.39 µF	≥ 0.39 µF < 1.0 µF	≥ 1.0 µF
1812	< 2.2 µF	≥ 2.2 µF	N/A

Table 1 – Capacitance Range/Selection Waterfall (0201 – 0805 Case Sizes)

Capacitance	Capacitance Code	Case Size/ Series		C0201C				C0402C						C0603C						C0805C					
		Voltage Code		7	9	8	4	7	9	8	4	3	5	7	9	8	4	3	5	7	9	8	4	3	5
		Rated Voltage (VDC)		4	6.3	10	16	4	6.3	10	16	25	50	4	6.3	10	16	25	50	4	6.3	10	16	25	50
		Capacitance Tolerance		Product Availability and Chip Thickness Codes – See Table 2 for Chip Thickness Dimensions																					
10,000 pF	103	K	M	A3	A3	A3	A3	BB	BB	BB	BB														
12,000 pF	123	K	M					BB	BB	BB	BB														
15,000 pF	153	K	M					BB	BB	BB	BB														
18,000 pF	183	K	M					BB	BB	BB	BB														
22,000 pF	223	K	M					BB	BB	BB	BB														
27,000 pF	273	K	M					BB	BB	BB	BB														
33,000 pF	333	K	M					BB	BB	BB	BB														
39,000 pF	393	K	M					BB	BB	BB	BB														
47,000 pF	473	K	M					BB	BB	BB	BB														
56,000 pF	563	K	M					BB	BB	BB	BB														
68,000 pF	683	K	M					BB	BB	BB	BB														
82,000 pF	823	K	M					BB	BB	BB	BB														
0.10 µF	104	K	M	A3	A3			BB	BB	BB	BB	BB		CG	CG	CG	CG	CG							
0.12 µF	124	K	M																						
0.15 µF	154	K	M																						
0.18 µF	184	K	M																						
0.22 µF	224	K	M					BB	BB					CG	CG	CG	CG								
0.27 µF	274	K	M											CG	CG	CG	CG								
0.33 µF	334	K	M											CG	CG	CG	CG								
0.39 µF	394	K	M											CG	CG	CG	CG								
0.47 µF	474	K	M					BB	BB					CG	CG	CG	CG	CG		DG	DG	DG	DG	DG	
0.56 µF	564	K	M											CG	CG	CG	CG			DP	DP	DP	DP	DP	
0.68 µF	684	K	M											CG	CG	CG	CG			DP	DP	DP	DP	DE	
0.82 µF	824	K	M											CG	CG	CG	CG			DF	DF	DF	DF	DF	
1.0 µF	105	K	M					BB	BB	BB	BB			CG	CG	CG	CG	CJ		DP	DP	DP	DP	DG	DG
1.2 µF	125	K	M																	DN	DN	DN	DN		
1.5 µF	155	K	M																	DN	DN	DN	DN		
1.8 µF	185	K	M																	DP	DP	DP	DP		
2.2 µF	225	K	M					BB	BB	BB[1]				CG	CG	CG	CG			DG	DG	DG	DG	DG	
2.7 µF	275	K	M																	DL	DL	DL	DL		
3.3 µF	335	K	M					BB[1]						CG	CG					DL	DL	DL	DG		
3.9 µF	395	K	M																	DG	DG	DG	DG		
4.7 µF	475	K	M					BE[1]	BE[1]					CG	CG	CG				DG	DG	DG	DG	DG	
5.6 µF	565	K	M																	DG	DG	DG			
6.8 µF	685	K	M																	DG	DG	DG			
8.2 µF	825	K	M																						
10 pF	106	K	M					BF[1]	BF[1]					CG[1]	CG[1]	CK[1]				DG	DG	DG	DG	DH	
12 pF	126	K	M																						
15 pF	156	K	M																						
18 pF	186	K	M																						
22 pF	226	K	M																	DG	DG	DH[1]			
47 pF	476	K	M																	DH[1]	DH[1]				
Capacitance	Capacitance Code	Rated Voltage (VDC)		4	6.3	10	16	4	6.3	10	16	25	50	4	6.3	10	16	25	50	4	6.3	10	16	25	50
		Voltage Code		7	9	8	4	7	9	8	3	5	4	7	9	8	4	3	5	7	9	8	4	3	5
		Case Size/Series		C0201C				C0402C						C0603C						C0805C					

xx[1] Available only in M tolerance.

Radial Leaded Multilayer Ceramic Capacitors for General Purpose Class 1, Class 2 and Class 3, 50 V_{DC}, 100 V_{DC}, 200 V_{DC}, 500 V_{DC}

FEATURES

- High capacitance with small size
- High reliability
- Crimp and straight leadstyles
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

APPLICATIONS

- Temperature compensation
- Coupling and decoupling

QUICK REFERENCE DATA										
DESCRIPTION	VALUE									
Ceramic Class	1				2				3	
Ceramic Dielectric	C0G				X7R				Y5V	
Voltage (V_{DC})	50	100	200	500	50	100	200	500	50	100
Min. Capacitance (pF)	10	10	33	33	100	100	100	100	10 000	10 000
Max. Capacitance (pF)	10 000	5600	3900	1800	1 000 000	560 000	220 000	47 000	1 000 000	220 000
Mounting	Radial									

MARKING

Marking indicates capacitance value and tolerance in accordance with "EIA 198" and voltage marks.

OPERATING TEMPERATURE RANGE

C0G, X7R: - 55 °C to + 125 °C

Y5V: - 30 °C to + 85 °C

TEMPERATURE CHARACTERISTICS

Class 1: C0G

Class 2: X7R

Class 3: Y5V

SECTIONAL SPECIFICATIONS

Climatic category (acc. to EN 60068-1)

Class 1 and 2: 55/125/21

Class 3: 30/85/21

APPROVALS

EIA 198

IEC 60384-9

DESIGN

- The capacitors consist of a general purpose MLCC
- The lead wires are 0.5 mm and are made of 100 % tinned copper clad steel wire
- The capacitors may be supplied with straight or kinked leads having a lead spacing of 2.5 mm and 5.0 mm
- Coating is made of yellow colored flame retardant epoxy resin in accordance with UL 94 V-0

CAPACITANCE RANGE

10 pF to 1 µF

TOLERANCE ON CAPACITANCE

± 5 %, ± 10 %, ± 20 %, + 80 %/- 20 %

RATED VOLTAGE

50 V_{DC}, 100 V_{DC}, 200 V_{DC}, 500 V_{DC}

TEST VOLTAGE

- 50 V_{DC} and 100 V_{DC}: 250 % of rated voltage
- 200 V_{DC}: 150 % of rated voltage + 100 V_{DC}
- 500 V_{DC}: 130 % of rated voltage + 100 V_{DC}

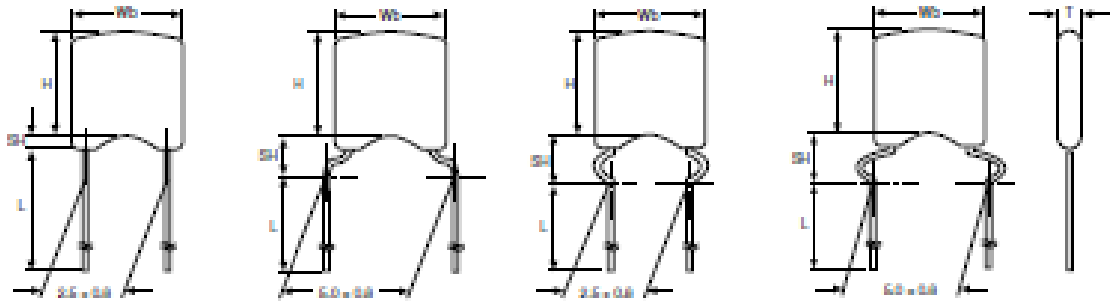
INSULATION RESISTANCE AT 500 V_{DC}

- 50 V_{DC} and 100 V_{DC}: 100 GΩ or 1000 ΩF whichever is less at rated voltage within 2 min of charging
- 200 V_{DC} and 500 V_{DC}: 10 GΩ or 100 ΩF whichever is less at rated voltage within 2 min of charging

DISSIPATION FACTOR

Class 1	0.1 % max. when C ≥ 30 pF (at 1 MHz; 1 V where C ≤ 1000 pF, and at 1 kHz; 1 V where C > 1000 pF) For C < 30 pF: DF = 100/(400 + 20 x C) DF = Dissipation factor in %; C = Capacitance value in pF
Class 2	2.5 % max. (at 1 kHz; 1 V)
Class 3	5 % max. (at 1 kHz; 1 V)

LEAD CONFIGURATION AND DIMENSIONS (in millimeters)



L2
Component outline for lead spacing 2.5 mm ± 0.8 mm (straight leads)

H5
Component outline for lead spacing 5.0 mm ± 0.8 mm (flat bent leads)

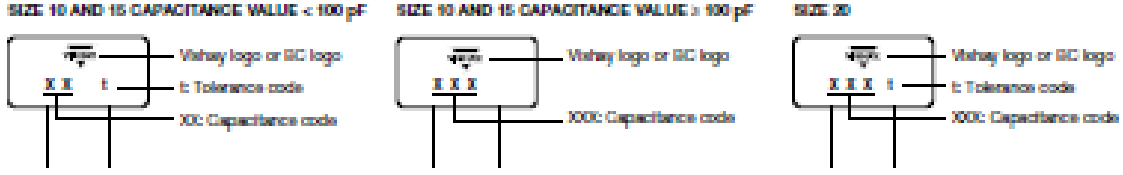
K2
Component outline for lead spacing 2.5 mm ± 0.8 mm (outside kink)

K5
Component outline for lead spacing 5.0 mm ± 0.8 mm (outside kink)

SIZE CODE	$Wb_{MAX.}$	$H_{MAX.}$	$T_{MAX.}$	MAXIMUM SEATING HEIGHT (SH)			
				L2	H5	K2	K5
10	3.6	3.6	2.3	1.6	2.6	3.5	-
15	4.0	4.0	2.6	1.6	2.6	3.5	3.5
20	5.0	5.0	3.2	1.6	2.6	3.5	3.5

Notes
- Bulk packed types have a standard lead length L = 30 mm ± 5 mm.
- The K5 lead style is not available for size 10.
- L2 and H5 are preferred styles.

MARKING



Notes
- The capacitance code indicates actual capacitance in pF when capacitance value < 100 pF.
- Two significant digits followed by one digit for the multiplier as given following: 1 = " 10, 2 = " 100, 3 = " 1000, 4 = " 10 000, 5 = " 100 000.
- The tolerance codes are J = 5 %, K = 10 %, M = 20 % and Z = + 80 %/- 20 %.

ORDERING CODE INFORMATION

K	104	K	15	X7R	F	5	3	H	5
1	2 3 4	5	6 7	8 9 10	11	12	13	14	15
Product Type	Capacitance (pF)	Capacitance Tolerance	Size Code	T.C. Code	Rated Voltage	Lead Diameter	Packaging/ Lead Length	Lead Style	Lead Spacing
K = Radial leaded MLCC	The first two digits are the significant figures of capacitance and the last digit is a multiplier as follows: 0 = " 1 1 = " 10 2 = " 100 3 = " 1000 4 = " 10 000 5 = " 100 000	J = ± 5 % K = ± 10 % M = ± 20 % Z = + 80 %/ - 20 %	Please refer to relevant datasheet	Please refer to relevant datasheet	F = 50 V_{DC} H = 100 V_{DC} K = 200 V_{DC} L = 500 V_{DC}	5 = 0.50 mm ± 0.05 mm	3 = Bulk T = Tape and reel U = Ammo	H = Flat crimp L = Straight K = Outside crimp	2 = 2.5 mm 5 = 5.0 mm

DATA SHEET

3F3
Material specification

Supersedes data of September 2004 2008 Sep 01

Material specification 3F3

3F3 SPECIFICATIONS

A medium frequency power material for use in power and general purpose transformers at frequencies of 0.2 - 0.5 MHz.

SYMBOL	CONDITIONS	VALUE	UNIT
μ_i	25 °C; ≤10 kHz; 0.25 mT	2000 ±20%	
μ_a	100 °C; 25 kHz; 200 mT	≈ 4000	
B	25 °C; 10 kHz; 1200 A/m	≈ 440	mT
	100 °C; 10 kHz; 1200 A/m	≈ 370	
P_V	100 °C; 100 kHz; 100 mT	≤80	kW/m³
	100 °C; 400 kHz; 50 mT	≤150	
ρ	DC; 25 °C	≈ 2	Ωm
T_C		≥200	°C
density		≈ 4750	kg/m³

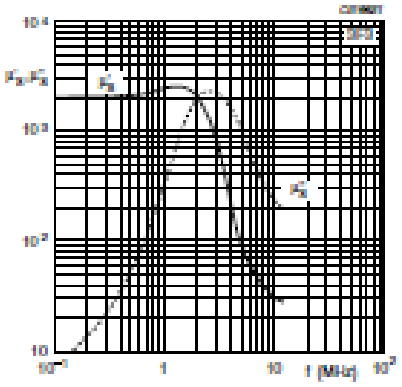


Fig.1 Complex permeability as a function of frequency.

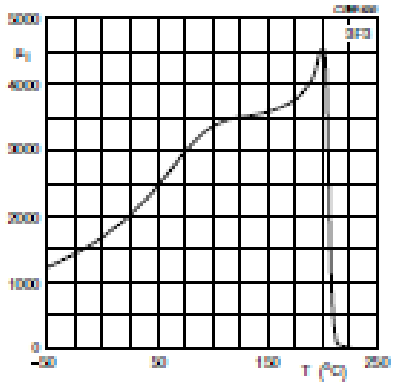


Fig.2 Initial permeability as a function of temperature.

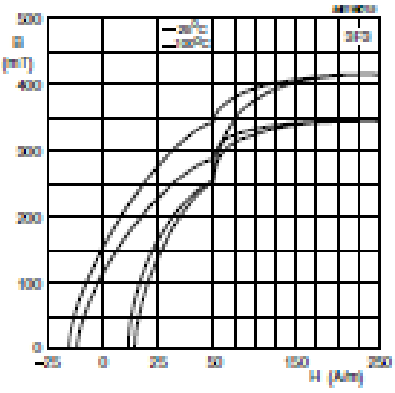


Fig.3 Typical B-H loops.

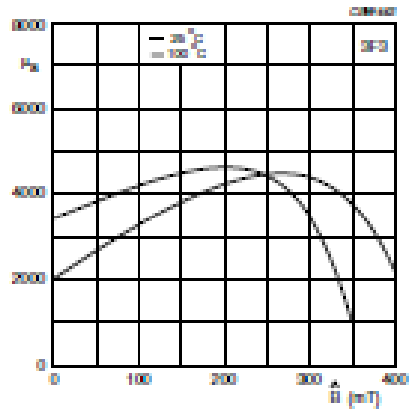


Fig.4 Amplitude permeability as function of peak flux density.

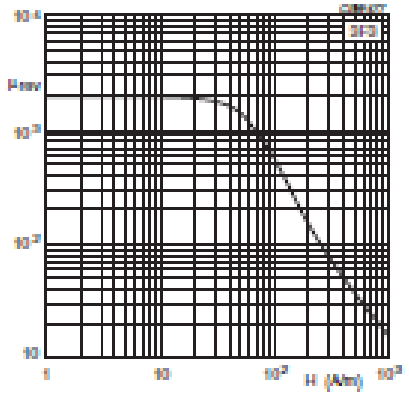


Fig.5 Reversible permeability as a function of magnetic field strength.

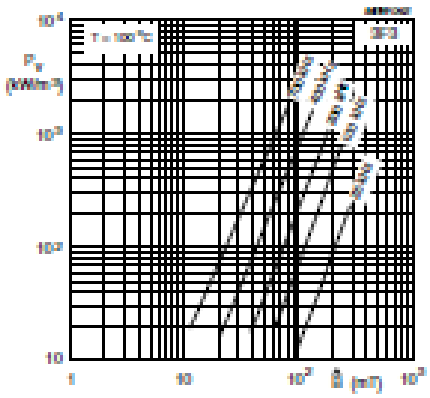


Fig.6 Specific power loss as a function of peak flux density with frequency as a parameter.

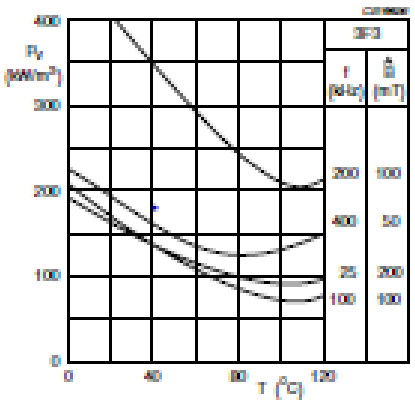


Fig.7 Specific power loss for several frequency/flux density combinations as a function of temperature.

Material specification 3F3

DATA SHEET STATUS DEFINITIONS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS
Preliminary specification	Development	This data sheet contains preliminary data. Ferroxcube reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Ferroxcube reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

DISCLAIMER

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Ferroxcube customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Ferroxcube for any damages resulting from such application.

PRODUCT STATUS DEFINITIONS

STATUS	INDICATION	DEFINITION
Prototype		These are products that have been made as development samples for the purposes of technical evaluation only. The data for these types is provisional and is subject to change.
Design-In		These products are recommended for new designs.
Preferred		These products are recommended for use in current designs and are available via our sales channels.
Support		These products are **not** recommended for new designs and may not be available through all of our sales channels. Customers are advised to check for availability.

MUR405, MUR410, MUR415, MUR420, MUR440, MUR460

SWITCHMODE Power Rectifiers

These state−of−the−art devices are a series designed for use in switching power supplies, inverters and as free wheeling diodes.

Features

- Ultrafast 25 ns, 50 ns and 75 ns Recovery Times
- 175°C Operating Junction Temperature
- Low Forward Voltage
- Low Leakage Current
- High Temperature Glass Passivated Junction
- Reverse Voltage to 600 V
- Shipped in Plastic Bags, 500 per Bag
- Available in Tape and Reel, 1500 per Reel, by Adding a "RLG" Suffix to the Part Number
- MUR460 available in Fan Fold Ammo Pak, 1000 per Box, by adding a "TFG" suffix to the part number
- These are Pb−Free Packages*

Mechanical Characteristics:

- Case: Epoxy, Molded
- Weight: 1.1 Gram (Approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead Temperature for Soldering Purposes: 260°C Max. for 10 Seconds
- Polarity: Cathode indicated by Polarity Band

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

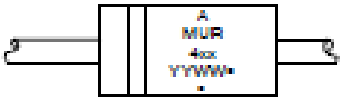
ON Semiconductor®

http://onsemi.com

ULTRAFAST RECTIFIERS
4.0 AMPERES, 50−600 VOLTS

AXIAL LEAD
CASE 267
STYLE 1

MARKING DIAGRAM



A = Assembly Location
MUR4xx = Device Number
x = 05, 10, 15, 20, 40, 60
YY = Year
WW = Work Week
* = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	MUR						Unit
		405	410	415	420	440	460	
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	150	200	400	600	V
Average Rectified Forward Current (Square Wave) (Mounting Method #3 Per Note 2)	$I_{F(AV)}$	4.0 @ T_A = 80°C				4.0 @ T_A = 40°C		A
Nonrepetitive Peak Surge Current (Surge applied at rated load conditions, half wave, single phase, 60 Hz)	I_{FSM}	125				110		A
Operating Junction Temperature & Storage Temperature	T_J, T_{stg}	−65 to +175						°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL CHARACTERISTICS

Rating	Symbol	MUR						Unit
		405	410	415	420	440	460	
Maximum Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	See Note 2						°C/W

ELECTRICAL CHARACTERISTICS

Rating	Symbol	MUR						Unit
		405	410	415	420	440	460	
Maximum Instantaneous Forward Voltage (Note 1) (i_F = 3.0 A, T_J = 150°C) (i_F = 3.0 A, T_J = 25°C) (i_F = 4.0 A, T_J = 25°C)	v_F		0.71 0.85 0.89				1.05 1.25 1.28	V
Maximum Instantaneous Reverse Current (Note 1) (Rated dc Voltage, T_J = 150°C) (Rated dc Voltage, T_J = 25°C)	i_R		150 5				250 10	μA
Maximum Reverse Recovery Time (I_F = 1.0 A, di/dt = 50 A/μs) (I_F = 0.5 A, i_R = 1.0 A, I_{REC} = 0.25 A)	t_{rr}		35 25				75 50	ns
Maximum Forward Recovery Time (I_F = 1.0 A, di/dt = 100 A/μs, Recovery to 1.0 V)	t_{fr}	25				50		ns
Controlled Avalanche Energy (Maximum)	W_{AVAL}				5			mJ
Typical Peak Reverse Recovery Current (I_F = 1.0 A, di/dt = 50 A/μs)	I_{RM}	0.5				1.7		A

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

MUR120 Series

SWITCHMODE Power Rectifiers

MUR105, MUR110, MUR115, MUR120, MUR130, MUR140, MUR160

The MUR120 series of SWITCHMODE power rectifiers are designed for use in switching power supplies, inverters and as free wheeling diodes.

Features

- Ultrafast 25, 50 and 75 Nanosecond Recovery Times
- 175°C Operating Junction Temperature
- Low Forward Voltage
- Low Leakage Current
- High Temperature Glass Passivated Junction
- Reverse Voltage to 600 V
- Shipped in Plastic Bags; 1,000 per Bag
- Available Tape and Reel; 5,000 per Reel, by adding a "RL" Suffix to the Part Number
- These are Pb−Free Devices*

Mechanical Characteristics:

- Case: Epoxy, Molded
- Weight: 0.4 Gram (Approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead Temperature for Soldering Purposes: 260°C Max. for 10 Seconds
- Polarity: Cathode Indicated by Polarity Band

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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http://onsemi.com

ULTRAFAST RECTIFIERS
1.0 AMPERE, 50 – 600 VOLTS

AXIAL LEAD
CASE 59
STYLE 1

MARKING DIAGRAM

A = Assembly Location
MUR1xx = Specific Device Code
Y = Year
WW = Work Week
* = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MAXIMUM RATINGS

Rating	Symbol	MUR							Unit
		105	110	115	120	130	140	160	
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	150	200	300	400	600	V
Average Rectified Forward Current (Square Wave Mounting Method #3 Per Note 2)	$I_{F(AV)}$	1.0 @ T_A = 130°C				1.0 @ T_A = 120°C			A
Nonrepetitive Peak Surge Current (Surge applied at rated load conditions, halfwave, single phase, 60 Hz)	I_{FSM}	35							A
Operating Junction Temperature and Storage Temperature	T_J, T_{stg}	−65 to +175							°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Maximum Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	Note 2	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Value		Unit
Maximum Instantaneous Forward Voltage (Note 1) (i_F = 1.0 Amp, T_J = 150°C) (i_F = 1.0 Amp, T_J = 25°C)	v_F	 0.710 0.875	 1.05 1.25	V
Maximum Instantaneous Reverse Current (Note 1) (Rated DC Voltage, T_J = 150°C) (Rated DC Voltage, T_J = 25°C)	i_R	 50 2.0	 150 5.0	μA
Maximum Reverse Recovery Time (I_F = 1.0 A, di/dt = 50 A/μs) (I_F = 0.5 A, I_R = 1.0 A, I_{REC} = 0.25 A)	t_{rr}	 35 25	 75 50	ns
Maximum Forward Recovery Time (I_F = 1.0 A, di/dt = 100 A/μs, I_{REC} to 1.0 V)	t_{fr}	25	50	ns
Typical Peak Reverse Recovery Current (I_F = 1.0 A, di/dt = 50 A/μs)	I_{RM}	0.55		A

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

International
IOR Rectifier

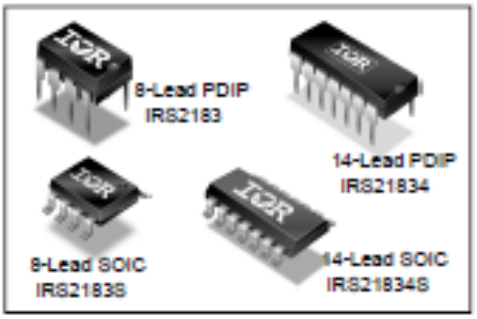
IRS2183/IRS21834(S)PbF

HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V and 5 V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5 V offset
- Lower di/dt gate driver for better noise immunity
- Output source/sink current capability 1.4 A/1.8 A
- RoHS compliant

Packages



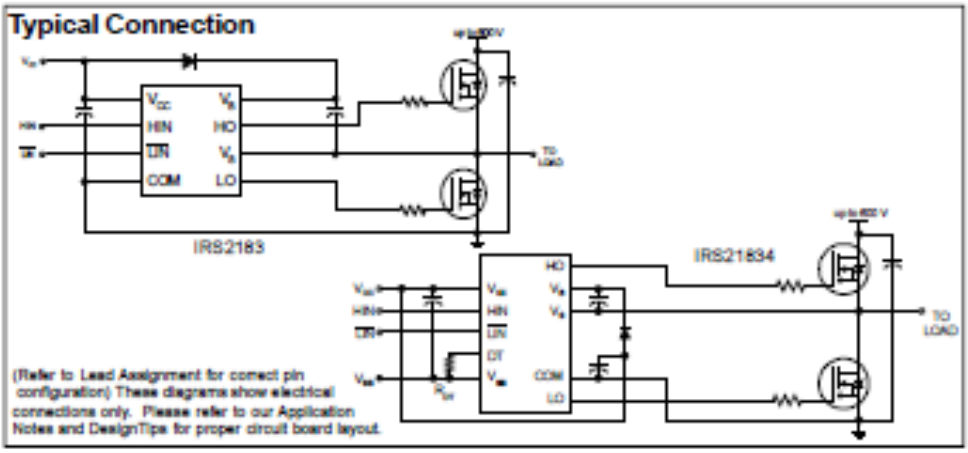
Description

The IRS2183/IRS21834 are high voltage, high speed power MOSFET and IGBT drivers with dependent high-side and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Deadtime (ns)	Ground Pins	t_{on}/t_{off} (ns)
2181	HIN/LIN	no	none	COM	180/220
21814				Vss/COM	
2183	HIN/$\overline{LIN}$	yes	Internal 400	COM	180/220
21834			Program 400-5000	Vss/COM	
2184	IN/$\overline{SD}$	yes	Internal 400	COM	680/270
21844			Program 400-5000	Vss/COM	

Typical Connection



(Refer to Lead Assignment for correct pin configuration) These diagrams show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating absolute voltage		-0.3	620 (Note 1)	V
V_S	High-side floating supply offset voltage		V_B - 20	V_B + 0.3	
V_{HO}	High-side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low-side and logic fixed supply voltage		-0.3	20 (Note 1)	
V_{LO}	Low-side output voltage		-0.3	V_{CC} + 0.3	
DT	Programmable deadtime pin voltage (IR21834 only)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & $\overline{LIN}$)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{SS}	Logic ground (IR21834 only)		V_{CC} - 20	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25$ °C	(8-lead PDIP)	—	1.0	W
		(8-lead SOIC)	—	0.625	
		(14-lead PDIP)	—	1.6	
		(14-lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8-lead PDIP)	—	125	°C/W
		(8-lead SOIC)	—	200	
		(14-lead PDIP)	—	75	
		(14-lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: All supplies are fully tested at 25 V and an internal 20 V clamp exists for each supply.

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15 V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High-side floating supply offset voltage	Note 2	600	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side and logic fixed supply voltage	10	20	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & $\overline{LIN}$)	V_{SS}	V_{CC}	
DT	Programmable deadtime pin voltage (IR21834 only)	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21834 only)	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 2: Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM, C_L = 1000 pF, T_A = 25 °C, DT = V_{SS} unless otherwise specified.

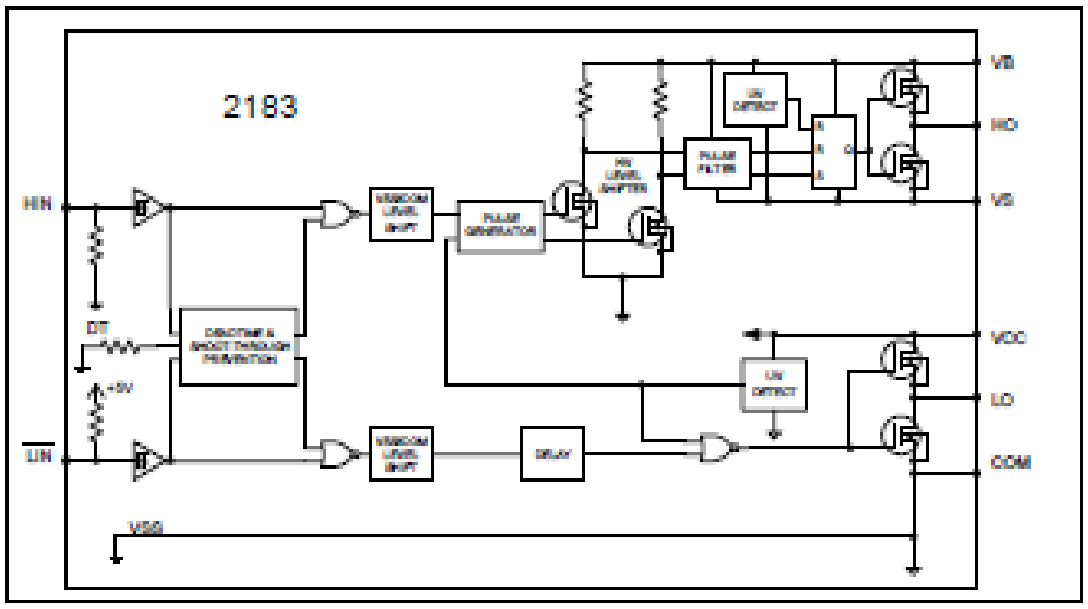
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	180	270	ns	V_S = 0V
t_{off}	Turn-off propagation delay	—	220	330		V_S = 0V or 600V
MT	Delay matching | t_{on} - t_{off} |	—	0	35		
t_r	Turn-on rise time	—	40	60		V_S = 0 V
t_f	Turn-off fall time	—	20	35		
DT	Deadtime: LO turn-off to HO turn-on(DT_{LO-HO}) &	280	400	520		R_{DT}= 0 Ω
	HO turn-off to LO turn-on (DT_{HO-LO})	4	5	6	µs	R_{DT} = 200 kΩ (IRS21834)
MDT	Deadtime matching = | DT_{LO-HO} - DT_{HO-LO} |	—	0	50	ns	R_{DT}=0 Ω
		—	0	600		R_{DT} = 200kΩ (IRS21834)

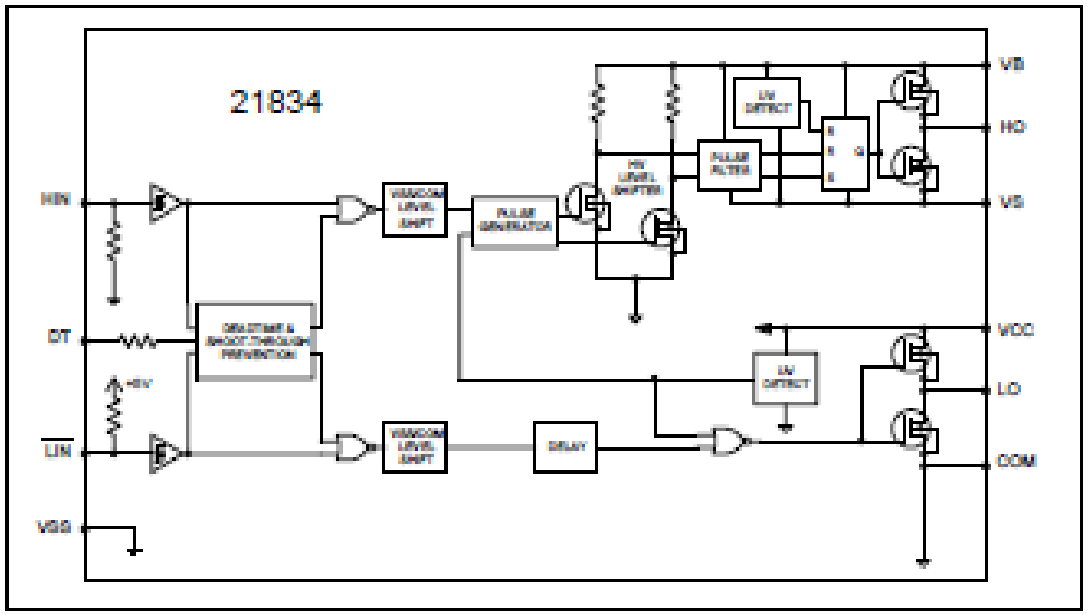
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM, DT= V_{SS} and T_A = 25 °C unless otherwise specified. The V_{IL}, V_{IH}, and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads: $\overline{HIN}$ and LIN. The V_O, I_O, and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage for HIN & logic "0" for $\overline{LIN}$	2.5	—	—	V	V_{CC} = 10 V to 20 V
V_{IL}	Logic "0" input voltage for HIN & logic "1" for $\overline{LIN}$	—	—	0.8		
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	1.4		I_O = 0 A
V_{OL}	Low level output voltage, V_O	—	—	0.2		I_O = 20 mA
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0 V or 5 V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.8	mA	
I_{IN+}	Logic "1" input bias current	—	25	60	µA	HIN = 5 V, $\overline{LIN}$ = 0 V
I_{IN-}	Logic "0" input bias current	—	—	5.0		HIN = 0 V, $\overline{LIN}$ = 5 V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	1.4	1.9	—	A	V_O = 0 V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	1.8	2.3	—		V_O = 15 V, PW ≤ 10 µs

Functional Block Diagrams

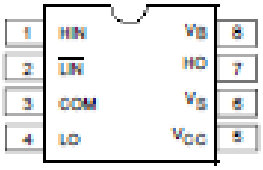




Lead Definitions

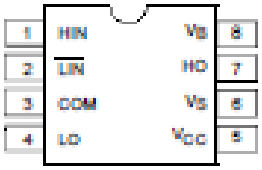
Symbol	Description
HIN	Logic input for high-side gate driver output (HO), in phase (referenced to COM for IRS2183 and VSS for IRS21834)
LIN	Logic input for low-side gate driver output (LO), out of phase (referenced to COM for IRS2183 and VSS for IRS21834)
DT	Programmable deadtime lead, referenced to VSS (IRS21834 only)
V_{SS}	Logic ground (IRS21834 only)
V_B	High-side floating supply
HO	High-side gate driver output
V_S	High-side floating supply return
V_{CC}	Low-side and logic fixed supply
LO	Low-side gate driver output
COM	Low-side return

Lead Assignments



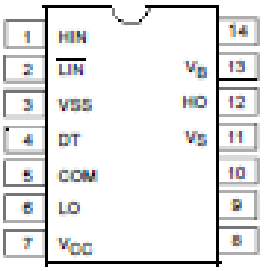
8-Lead PDIP

IRS2183PbF



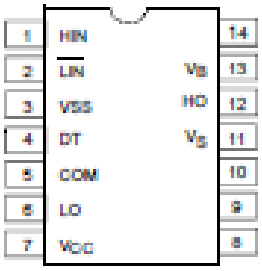
8-Lead SOIC

IRS2183SPbF



14-Lead PDIP

IRS21834PbF



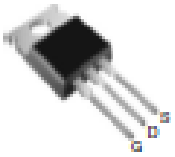
14-Lead SOIC

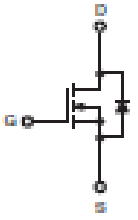
IRS21834SPbF

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	100	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.27
Q_g (Max.) (nC)	16	
Q_{gs} (nC)	4.4	
Q_{gd} (nC)	7.7	
Configuration	Single	

TO-220AB





N-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- 175 °C Operating Temperature
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

RoHS* COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRF520PbF
	SiHF520-E3
SnPb	IRF520
	SiHF520

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	100	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	9.2	A
		T_C = 100 °C		6.5	
Pulsed Drain Current[a]			I_{DM}	37	
Linear Derating Factor				0.40	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	200	mJ
Repetitive Avalanche Current[a]			I_{AR}	9.2	A
Repetitive Avalanche Energy[a]			E_{AR}	6.0	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	60	W
Peak Diode Recovery dV/dt[c]			dV/dt	5.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 25 V, starting T_J = 25 °C, L = 3.5 mH, R_g = 25 Ω, I_{AS} = 9.2 A (see fig. 12).
c. I_{SD} ≤ 9.2 A, dI/dt ≤ 110 A/µs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	2.5	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		100	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.13	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V		-	-	25	µA
		V_{DS} = 80 V, V_{GS} = 0 V, T_J = 150 °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 5.6 A[b]	-	-	0.27	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 5.6 A[b]		2.7	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	360	-	pF
Output Capacitance	C_{oss}			-	150	-	
Reverse Transfer Capacitance	C_{rss}			-	34	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 9.2 A, V_{DS} = 80 V, see fig. 6 and 13[b]	-	-	16	nC
Gate-Source Charge	Q_{gs}			-	-	4.4	
Gate-Drain Charge	Q_{gd}			-	-	7.7	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50 V, I_D = 9.2 A, R_g = 18 Ω, R_D = 5.2 Ω, see fig. 10[b]		-	8.8	-	ns
Rise Time	t_r			-	30	-	
Turn-Off Delay Time	$t_{d(off)}$			-	19	-	
Fall Time	t_f			-	20	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	9.2	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	37	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 9.2 A, V_{GS} = 0 V[b]		-	-	1.8	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 9.2 A, dI/dt = 100 A/µs[b]		-	110	260	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.53	1.3	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.