GRADO EN INGENIERÍA EN TECNOLOGÍAS DE TELECOMUNICACIÓN

TRABAJO FIN DE GRADO

CIRCUIT DESIGN FOR BIO-INSPIRED SAMPLING

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Circuit Design for Bio-inspired Sampling

(Diseño de Circuito para muestreo bio-inspirado)

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GRADO EN INGENIERÍA EN TECNOLOGÍAS DE TELECOMUNICACIÓN

TRABAJO FIN DE GRADO

Circuit Design for bio-inspired sampling

Autor: Gimena Segrelles Munarriz

Director: Karen Adan

Co-Director: Adrien Hoffet

Madrid

Agradecimientos

Quiero agradecer el poder haber hecho este trabajo tanto a ICAI como a EPFL. Concretamente, dar las gracias a mi mentora Karen Adam y a Adrien Hoffet por ayudarme a hacerlo posible.

CIRCUIT FOR BIO-INSPIRED SAMPLING

Autor: Segrelles Munárriz, Gimena.
Director: Adam, Karen.
Entidad Colaboradora: ICAI – Universidad Pontificia Comillas

RESUMEN DEL PROYECTO

Este proyecto consiste en diseñar un dispositivo que muestree señales imitando a como lo hacen las neuronas. En [1] se presentan una serie de proposiciones que han sido utilizadas en este proyecto para diseñar dicho dispositivo. Finalmente se han obtenido señales como los potenciales de acción, pero también otros resultados no previstos.

Palabras clave: TEM, potenciales de acción, codificación temporal, hardware, muestreo

1. Introducción

El muestro es un paso clave para convertir una señal del dominio analógico al dominio digital. Normalmente, este proceso de muestreo se realiza mediante la obtención de valores de la amplitud de una señal en ciertos instantes de tiempo. Sin embargo, en la naturaleza, concretamente en el cerebro, las neuronas muestrean de la siguiente manera: la neurona integra (suma y acumula) la señal de entrada que le llega o estímulo hasta que cierto umbral es alcanzado, lo cual desencadena en la emisión o disparo de una señal llamada potencial de acción. La información del estímulo recibido por la neurona está en el espacio temporal entre potencial de acción y potencial de acción. Es aquí donde encontramos el propósito de este proyecto que es tratar de imitar este comportamiento mediante una implementación hardware.

2. Definición del proyecto

El proyecto consiste en la realización de simulaciones y en el diseño e implementación de un circuito que trate de imitar la forma en la que las neuronas muestrean. Los desarrollos teóricos y el diseño del circuito están basados en un trabajo previo realizado por Aurel A. Lazar [1].

Descripción del modelo/sistema/herramienta

El circuito propuesto por [1] que se muestra en la *Figura 1* se compone de las siguientes partes: un integrador para simular el proceso de integración del estímulo, un disparador sin inversión para imitar la generación del potencial de acción una vez alcanzado el umbral, en este caso representado por la letra δ y una red de realimentación.

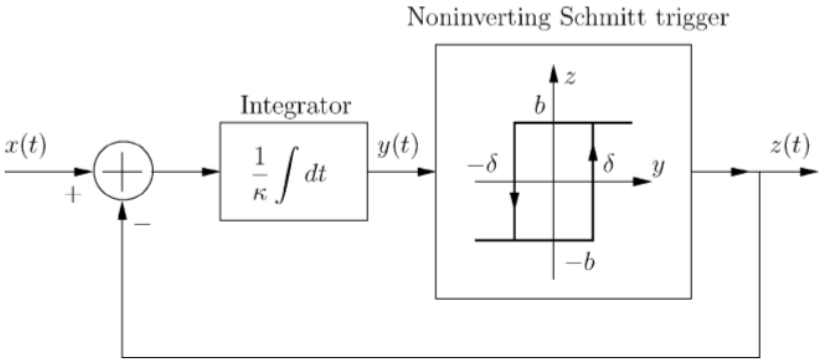

Figura 1. Diagrama de Bloques propuesto por [1]

El circuito propuesto por este proyecto difiere del previo del siguiente modo:

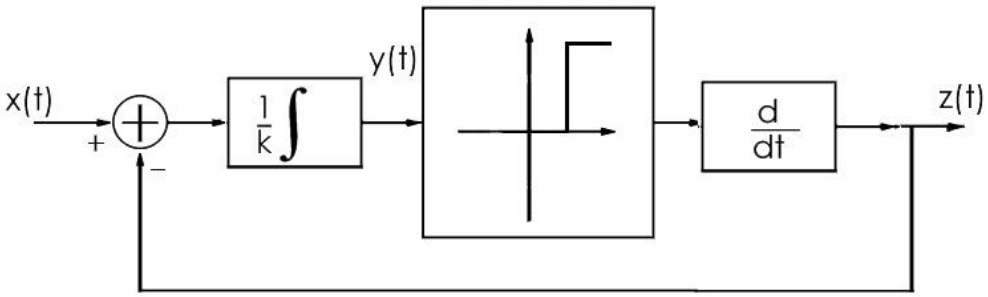

Figura 2 Diagrama de bloques del diseño

Lo único que mantenemos es el integrador y el circuito de realimentación ya que es importante para resetear el integrador. Sin embargo, en vez de utilizar un disparador de Schmitt con histéresis, hemos optado por un comparador simple con el fin de tener un solo valor para el umbral δ. A continuación, con el objetivo de obtener una señal lo más parecida en forma al potencial de acción, hemos añadido un circuito diferenciador cuyo cometido es "derivar" la señal cuadrada a la salida del comparador.

3. Resultados

Simulaciones: Llevadas a cabo con el programa Lspice de Analog Devices.

Ejemplo: Para un señal de entrada: $1.75\sin(2\pi 4\times 10^3)$ y δ = 3.5 V, la señal de salida es:

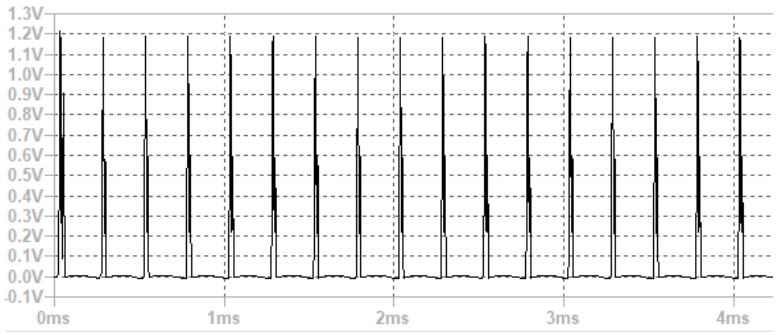

Figura 3 Resultado A. Señal de salida

Resultados empíricos: Para realizar los tests, en vez de utilizar un telescopio clásico, se utilizó un aparato llamado *Analog Discovery 2*.

En este test, dos señales fueron inyectadas en el circuito: primero, $2 \times \sin(2\pi 5000)$ y segundo, $2 \times \sin(2\pi 10000)$.

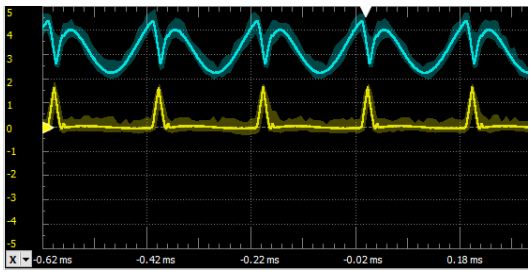

Figura 3 señal de entrada 2sin(2π5000)

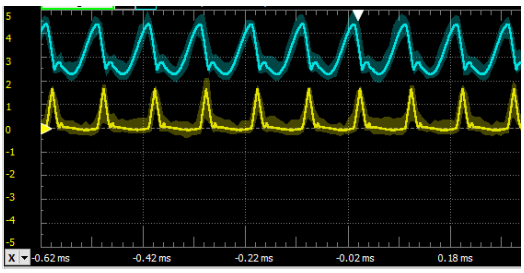

Figura 5 señal de entrada 2sin(2π10000)

En la *Figura 5* podemos ver la forma de sierra en la señal, así como el hecho de que la señal no baja hasta cero, es decir no es del todo reseteada. En la *Figura 4*, se pueden observar los efectos negativos de este comportamiento de forma más evidente. Puesto que la señal de 5kHz tiene un rizado más 'ancho', el potencial de acción que se resta no es lo suficientemente significativo, lo cual produce dos 'lóbulos' o dos máximos en vez de la señal de sierra. Esto impacta directamente en el valor de δ: si el valor es más pequeño que el valor de los dos máximos entonces habrá dos potenciales de acción disparados de forma muy seguida. Estas señales serán realimentadas en el circuito cada una de ellas creando otros dos 'lóbulos', lo cual desembocará en el disparo de más acciones potenciales. Este comportamiento del circuito es evidente un comportamiento no deseado por lo que ha de elegirse bien el valor δ o amplificar las acciones potenciales realimentados para que tengan un mayor impacto.

4. Conclusiones

A pesar de los problemas presentados en el apartado anterior relativos a la realimentación, en general, para otras frecuencias, el circuito funciona de forma deseable: obtenemos potenciales de acción coherentes y con la forma deseada.

5. Referencias

[1] Aurel A. Lazar, Fellow, IEEE, and László T. Tóth Perfect Recovery and Sensitivity Analysis of Time Encoded Bandlimited Signals

[2]Dale Purves, George J. Augustine , David Fitzpatrick, William C. Hall , Anthony-Samuel Lamantia Neuroscience 5th Edition. New York: Oxford University Press, 2018.

[3] Thomas C.Hayes, Paula Horowitz (1989) "Chapter 4 Feedback and Operational Ampfliers" Student Manual for the Art of Electronics. New York: Oxford University Press

[4]https://www.electronics-tutorials.ws/

[5] LTspice Guide

Images:

Figure 1 was obtained from [1]

CIRCUIT FOR BIO-INSPIRED SAMPLING

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Supervisor: Adam, Karen.
Collaborating ICAI – Universidad Pontificia Comillas

ABSTRACT

This project consists in the design of a device able to sample signals in the same way neurons do it. The design of the circuit is based on the propositions made in [1]. Finally, a PCB was designed and manufactured and the expected results were obtained that is the action potenicals, as well as some other unexpected ones.

Keywords: TEM, action potential, temporal encoding, hardware, sampling

1. Introduction

Sampling is a key step in converting any analogue signal to the digital world. Usually, it is done by recording the signal's amplitude at certain defined time points. In nature, concretely in the brain, sampling is done differently. A neuron integrates its input until a threshold is reached and then fires a spike or action potential. How the information is encoded in the signals is explained by two main different theories: rate coding which is based on how many spikes are triggered per unit of time and temporal coding which is the one on which this project is based. Temporal coding relies on the principle that the signal's information is contained not in how many spikes are triggered, but in the temporal space between spike and spike. The main purpose of this project is to mimic with hardware the way in which neurons encode signal information.

2. Project Definition

The project consists in the realization of simulations and the design and implementation of a circuit that will try to mimic neurons' way of sampling. The theoretical ideas and constraints of the circuit as well as its high level design are based on an article [1] by Aurel A. Lazar and László T. Tóth concretely called "Perfect Recovery and Sensitivity Analysis of Time Encoded Bandlimited Signals".

3. System Description

In [1] they propose a high level schema of the main parts the circuit should have which is reminiscent to the integrate and fire model. The proposed circuit by [1] shown in figure 1 is composed by the following blocks: an integrator so as to simulate the integration (sum and accumulation) done by the neuron, a non-inverting Schmitt trigger so as to generate the action potential signal once a certain threshold (represented by δ) is surpasseed and finally a feedback net with the function of resetting the circuit.

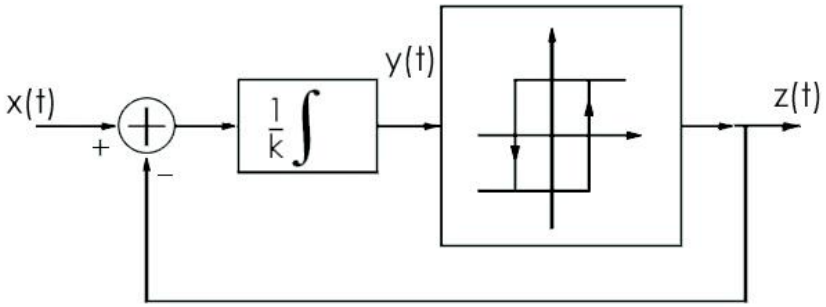

Figure 1. Block Diagram by [1]

However, the circuit proposed in this project is different from the one described in [1] in the following way:

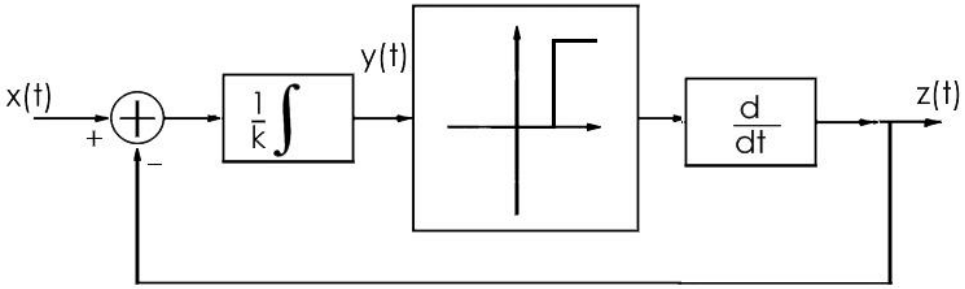

Figure 2. Block diagram proposed for the project

The only aspects that do not vary with respect to the design in [1] are the integrator and the feedback net. However, instead of implementing a non-inverting Schmitt trigger with hysteresis we have chosen a simple comparator with the purpose of having just one value for the threshold δ. In addition, with the aim of obtaining a signal as similar as possible to the real spikes, we have added a differentiator which will "derivate the square signal that comes out of the comparator".

4. Results

Simulations: They were performed with Ltspice tool by Analog Devices.

Example: For an input signal: $1.75\sin(2\pi 4 \times 10^3)$ and δ = 3.5 V, the obtained output is:

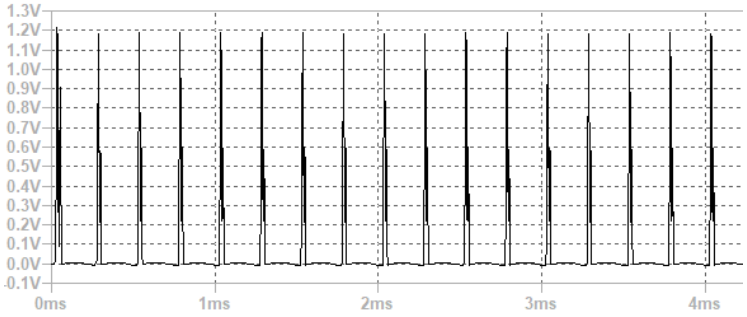

Figure 3. Output signal

Empirical results: For the testing setup, an analog discovery 2 was used instead of a classical oscilloscope.

The following figures are the result of feeding circuit with : to the left, a $2 \times \sin(2\pi 5000)$ and to the right, a $2 \times \sin(2\pi 10000)$.

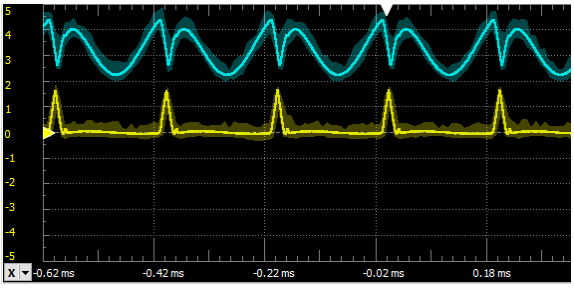

Figure 4Result when input is a 10kHz sine

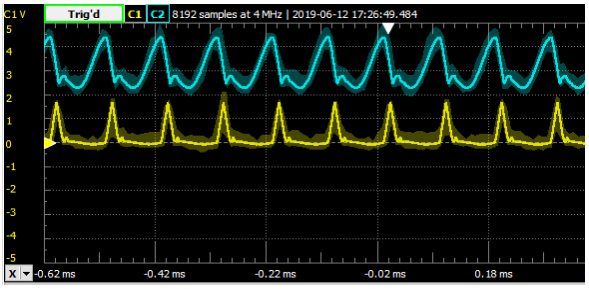

Figure 5. Result when input is a 10kHz sine

In *Figure 5* one can see the saw-like shape but also that the reset does not go fully to zero. The fact that the spike needs to be amplified in the feedback loop is more visible in *Figure 4* because the ripple due to the 5kHz signal is wider (slower) than that of the 10kHz. The spike which is not precisely wide, is not large or significant enough to really discharge the capacitor. This has a direct consequence on the threshold δ value. If a too low value is chosen there is the possibility that two spikes are fired consecutively due to the two lobes. Consequently, the two spikes would be fed back to the circuit and since they would be practically no time between both of them, at the output of the integrator would have three of these lobes instead of two. Again, if the threshold is too low, the amount of fired spikes would grow and grow as well as the number of lobes and this is an incorrect behavior of the circuit.

5. Conclusions

Despite the issues presented in the previous section regarding feedback, in general the circuit has the desired behavior for most frequencies: we obtain coherent action potentials and they have the desired shape.

6. References

[1] Aurel A. Lazar, Fellow, IEEE, and László T. Tóth Perfect Recovery and Sensitivity Analysis of Time Encoded Bandlimited Signals

[2]Dale Purves, George J. Augustine , David Fitzpatrick, William C. Hall , Anthony-Samuel Lamantia Neuroscience 5th Edition. New York: Oxford University Press, 2018.

[3] Thomas C.Hayes, Paula Horowitz (1989) "Chapter 4 Feedback and Operational Ampfliers" Student Manual for the Art of Electronics. New York: Oxford University Press

[4]https://www.electronics-tutorials.ws/

[5] LTspice Guide

Images:

Figure 1 was obtained from [1]

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Chapter 1 INTRODUCTION

Sampling is a key step in converting any analogue signal to the digital world. Usually, it is done by recording the signal's amplitude at certain defined time points. In nature, concretely in the brain, sampling is done differently. A neuron integrates its input until a threshold is reached and then it fires a spike. The interesting characteristic of these spikes is that they all have the same amplitude regardless of the strength of the stimulus, which means that the information of the signal is not contained in the amplitude like it is for classical sampling. How the information is encoded in the signals is explained by two main different theories: rate coding which is based on how many spikes are triggered per unit of time and temporal coding which is the one on which this project is based. Temporal coding relies on the principle that the signal's information is contained not in how many spikes are triggered, but in the temporal space between spike and spike. The main purpose of this project is to mimic with hardware the way in which neurons encode signal information.

PROJECT MOTIVATION

As mentioned before this project aims to reproduce how the brain encodes signals. The brain is good at managing various stimuli as well as doing seemingly complex and multiple tasks with certain ease, which could be translated as having a "multichannel" device in signal processing. Therefore, the motivation for this project is to design the basic element of what will be a multichannel system by developing an electronic neuron. The main advantage between current multi-channel sampling and multi-channel time encoding is that the second has a more straightforward inverse problem than classical sampling. This means that when sampling a signal with multiple similar time encoding machines we know how to reconstruct the signal more easily than when doing so with regular samplers. Another important advantage is quantization: Quantization in time is more accurate than quantization in amplitude, because it is easier (with today's hardware) to sample at a higher rate than it is to

quantize at higher resolution, so time encoding might provide more accurate encodings of the data.

Moreover, a notable advantage is power consumption. The difference between state of the art multichannel devices and the one we want to design here is that, the bio-inspired one is meant to be much more power efficient, in the sense that it consumes less power for doing the same function as other circuits. The main argument behind this reasoning is that even though there are computations and operations for which computers, microprocessors or simple electronic devices are much more efficient and faster than the brain, there are also some other tasks like image recognition where the brain takes the lead in speed and efficiency. Depending on the task, the brain can be from 10 times to 100,000 times more energy efficient than current state of the art machines. This possible advantage is important because power consumption is a major issue in electronics due to heat radiation and limited power supply.

Generally, neuromorphic engineering is aimed for developing neurons or neural circuits that behave as much as possible as their biological versions with the purpose of creating learning machines. This project is different in that way; its purpose is different and this fact has an impact on the parameters we will be focusing on. This neuron is not designed for learning, but for encoding and more importantly for accurate signal reconstruction. Therefore, a parameter like noise which might even be desired in general neuro-morphology as it adds randomness to the system and thus a more brain-like behavior, in this project will be a parameter we will characterize and strive to keep low.

A final reason to start this project is that this way of sampling is the way in which nature samples. It has survived millennia of evolutionary pressure and at the same time is common to most animals that have a nervous system of certain complexity.

Chapter 2 TECHNOLOGY DESCRIPTION

The following chapter is dedicated to describe important terms that may not be known by the reader, with the aim of making the main concepts easier to understand. It is noted that some terms are basic but due to the project involving the signal processing field as well as the neuromorphic field it is important for a reader of either fields to be able to follow the paper, regardless of his or her background.

- Time encoding machine (TEM): system that can map/encode amplitude information into a time sequence [1].
- Time decoding machine (TDM): system which can recover the amplitude information of a signal by receiving as input its time sequence [1].
- Action potential or spike: electrical signal produced by a neuron when it receives a stimulus strong enough [3].
- Refractory period: minimum time that must pass between the firing of a spike and the next [3].

Chapter 3 STATE OF THE ART

The aim of this project is to find a solution to a problem in the signal processing field. However, given the nature of the solution, one could say that the project is a combination of two fields: signal processing and neuro-engineering. Therefore, so as to understand why the combination of these two fields might bring innovation, a brief introduction and explanation of them will be made in the following paragraphs.

Signal processing is a field of mathematics and engineering oriented to the analysis, management and modification of signals, so as to store them, send them or extract useful information from them. In order to deal with these signals more easily, sampling is made, which consists on taking just the necessary information of a signal from which we will later be able to infer the rest of information or reconstruct it again. This is especially important when working with computers as analog signals belong to the continuous time domain, while computers work in the discrete domain. The sampling theorem was first conceived by Nyquist around the year 1928, but it was not until the 1940s -1950s with Shannon, Whittaker and Kotel'nikov that its potential was understood and developed [2]. The basic idea behind the theorem is to take values of the signal's amplitude at certain time intervals (or instants if we are talking about ideal sampling) like is shown in *Figure 1*.

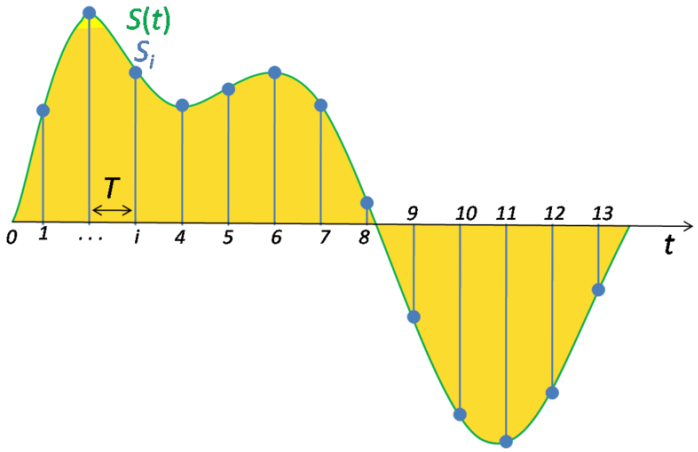

Figure 1. Sampling Theorem [8]

However, the recovery of the original signal is only possible under two conditions: (a) the frequency at which we may take samples must be at least two times the bandwidth of the signal and (b) the signal must be bandlimited so (a) can be fulfilled. Otherwise we will come across a phenomenon called aliasing due to which we will be unable to recover the original signal as it is shown in the following figure:

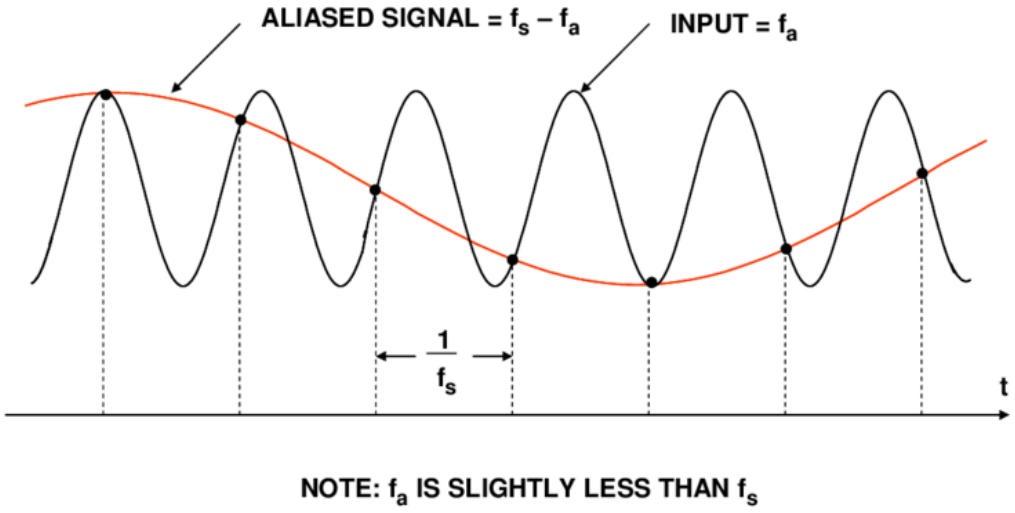

Figure 2. Effect of Aliasing [7]

The final step to this sampling process would be quantization in which values (represented with bits) are assigned to the different samples of the signal's amplitude according to a quantization step.

Nevertheless, in the real world modifications and transformations have consequences and therefore, we will never be able to recover the exact original signal. This is due to: noise, quantization error, jitter or other causes like the limitations of hardware and their behavior with high frequencies. As a consequence, since the development of the Sampling Theorem many sampling methods have been developed each of them trying to solve one or more of the aforementioned issues, sometimes at the cost of higher SW or HW complexity.

A solution for precision is irregular or non-uniform sampling in which the sampling frequency is not constant. The aim is to get more samples of the parts of the signal we are more interested in, which is possible as long as the average Nyquist frequency is twice the signal's bandwidth [10]. However, if we don't know the signal's bandwidth *a priori* it may be useful to use random sampling, so long one doesn't care at which times the samples are taken [11]. If what we want is to sample accurately high frequency signals, we might consider time interleaved sampling which consists on using multiple uniform sampling devices to sample a signal at different times and then join the results of each sampler.

Another option to sample high frequency signals might be to use a flash converter because of their speed and simplicity. However, the setback of this converter is that it requires many comparators which in turn require a high power consumption compared to the rest. Concretely, the number of comparators needed is $2^n - 1$ where n is the number of bits used in the quantization process, which means that high resolution comes at a high cost [15]. From here it is derived that to obtain more resolution a larger converter (in terms of area) would be needed which is not the case for the proposed project.

Another technique for sampling more similar to the one proposed in [1] is called delta sigma modulation. In fact, [1] compares its model and recovery algorithm with delta sigma modulation and in [12] they mention delta sigma modulation as though it were a time encoding machine. This is because delta sigma modulation uses an integrator and a

comparator, but with a different approach as the one proposed in [1]. To clarify this, I will dedicate the following paragraph to explain delta sigma modulation.

The process starts with a parameter δ (hence the name and with a different meaning from the one in [1]) which has a certain value. This value is compared to that of the analog signal at a certain time, if δ is smaller than the value of the original signal, δ will be increased by one step and fed back to the comparator for the next iteration and so on. However, in the output we will only have a pulse whose amplitude will be represented by a single bit. In order to recover the original signal just an RC circuit is needed to sum up the values.

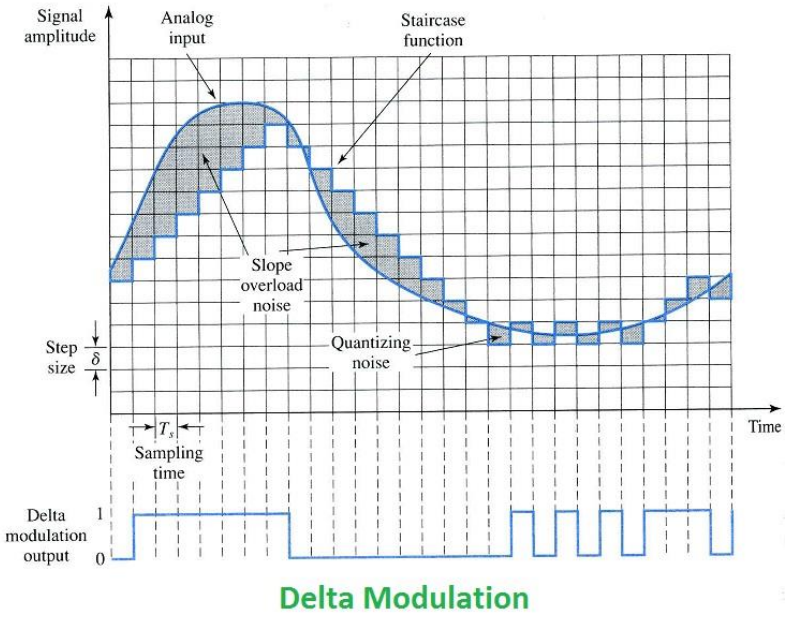

Figure 3. Delta sigma modulation [13]

The figure shows what was explained above: the comparison with the original signal and thus the summing of δ and below the one-bit output signal. In their comparison [1] points out how delta sigma modulation offered a low accuracy recovery given its linear demodulator structure.

[12] expands what was developed in [1] by expanding the types of signals to be fed into the system as well as freeing the system of knowing the signal's bandwidth beforehand.

Now that we have introduced the background of how sampling is made we can proceed into introducing how the solution proposed in this project based on [1] is different from the state of the art methods and how is neuro-engineering involved.

Neuro-engineering or more specifically neuromorphic hardware is a branch of engineering aimed to mimic the way in which biological neurons work. Most of the research done in neuromorphic engineering aims to reproduce as truthfully as possible the chemical reactions that occur in neurons when producing the action potential signal. Other approaches focus more on how neurons communicate between them and thus try to mimic synapses. In this case, as it has previously been exposed, the interest lies on how neurons encode stimuli information in the action potentials they fire. In other words, the way in which neurons sample stimuli. Regarding this, there are some typical models used: Hodgkin-Huxley Model, Axon Hillock model and integrate-fire model. The first model mentioned aims to represent as realistically as possible the ionic exchange that occurs in cell membranes and that ultimately leads to an action potential. On the other hand, the Axon Hillock model is less realistic as it aims to capture the essence of the process that leads to an action potential. In the figure below we can see a block diagram of such model made by [14]. In this model the input current is integrated by the capacitance C_{mem} while its voltage increases until the threshold of amplifiers in block A is reached as explained in [14]. There is a sub-model within the Axon Hillock model which in addition allows to control the spiking threshold, but the circuit becomes more complex as it can be seen in [14].

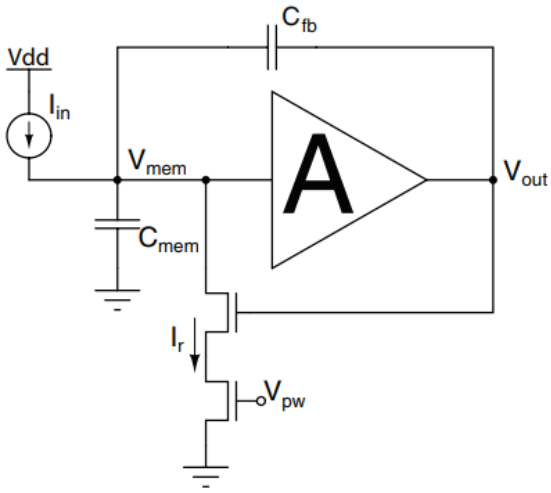

Figure 4. Axon Hillock Model [14]

All the aforementioned models are usually used in the neuroscience and computational fields. It is A. Lazar *et al* who have thought of applying the integrate and fire model in the signal processing domain and created the term TEM, Time Encoding Machine.

In their article [1] a certain implementation is proposed as well as a theoretical analysis which ensures the possibility of recovering the signal with a TDM. Even though, we have followed these theoretical constraints when designing the circuit, we have developed our own implementation which aims for obtaining a more spike-like shape signal. In order to achieve this, some changes will be applied to the circuit proposed by [1]: not using a Schmitt trigger and adding a differentiator.

FOR THE READER

The aim of the following paragraphs is to clear a possible question that might be arising in the reader's mind. A TEM is a sampler, not an A/D converter, in order words the output signal is not a digital signal, but it is still analog. Consequently, in order to proof that the original circuit can be recovered, we would need to sample and convert it into the digital domain. This might lead to another question, why use a sampler that needs another sampler? There are two main answers for this:

1. The final purpose of this project is to ideally use it to feed a neuromorphic chip and thus this issue would no longer be a problem because neuromorphic chips are designed to process data from analog signals.
2. Not looking into the future however, the use of this sampler can still be justified. On the one hand, having another sampler and A/D is a temporal solution necessary for the research and development phase of these kinds of sampler. On the other hand, the A/D converter to be added would not be dealing with a different set of amplitude values at a certain time, but instead at 'yes' spike or 'no' spike values which still saves energy and time.

Chapter 4 PROJECT DEFINITION

JUSTIFICATION

In the previous section we have seen various sampling techniques which have their own advantages as well as flaws and complexities. Based on the results by [1] we believe that it is worth trying to implement a hardware version of what it is proposed in the paper though with a few changes, due to all the advantages that such sampler could have with respect to the rest. Most of the reasons why this project is interesting were described in the motivation. In a few words, there are chances of getting less error with respect to the original signal as well as a higher resolution and at the same time have a more or less simple circuit design. Another reason why this project might be interesting is that TEM are meant to be asynchronous, thus the system would be free of using a clock and thus will be free of jitter. In addition, as it was mentioned the circuitry is simpler and is composed of silicon components which may allow speed as well as lower power consumption. Economically speaking, it is yet to see of this method would be cheaper than the ones currently dominating the market.

Now to answer the question of why we have modified the design proposed in [1]. Concretely with our design, we want to get rid of parts of the signal output seen in [1] that have no relevant information of the signal and that are originated due to the Schmitt trigger with hysteresis.

OBJETIVES

Most of the research papers just focus on the theoretical part of developing a time encoding machine, this project however, is more focused on the practical implementation of theory. One of the objectives of the project is to make a real implementation of an integrator-fire model of a neuron so as to characterize it: noise, power, costs and more importantly its

actual behavior. The limitations of the encoding and the quality of the decoding are also main concerns of the future of this project as the final aim is to infer if this kind of hardware implementation and TEM are a good option for improving signal processing sampling techniques and if they add actual value with respect to the state of the art. It must be noted that this project will only be focusing on building the TEM and not the TDM as the decoding will be made using software.

As a final remark, this project is aimed to be used for sampling audio signals and as it was previously mentioned another main goal is to get an output signal as similar as possible in shape as that of the real action potentials to add precision to the time sequence.

METHODOLOGY

In the following lines, the way in which this project was carried out will be described. The first task was to do research and read articles like [1] so as to understand the nature of the problem that needed to be solved and how. This was followed by the design and research phase so as to carry out different solutions from the ones proposed. In this phase simulation tools were used, concretely LTSpice XVII. When the desired results were reached with the simulations the prototyping phase started. The prototyping phase involved the design and manufacturing of a PCB with the aid of KiCad. Once the PCB is manufactured(externally) and soldered (by the author) more exhaustive tests will be done. Ideally, if there are no complications during these phases, the project would expand and try to work for more than one channel. In addition, there were weekly meetings with the mentor so as to check the correct progress of the work.

PLANNING AND ECONOMIC ESTIMATES

Temporal Planning

The following timeline is a guide of the evolution of the project, however, it is subject to delays and changes as the project advances and different problems are found and confronted.

Week of	**Planned Work**
18/02	- Read paper, understand functioning of TEM - Come up with list of simulation software - Pick one, with advantages, disadvantages - First simulation of original circuit (in Lazar and Tòth 2004)
25/02	- Propose schemes for integrate-and-fire model - Implement them using simulator
Project description and planning is due on Friday the 1st of March.	
04/03	- Testing using simulations - Try different frequencies and voltages
11/03	- Implementation of feedback loop and offset
18/03	- Design of actual hardware: choose components taking into account costs - PCB design
25/03	- PCB design (+ ordering hardware)
01/04	- PCB Edit, check (+ ordering hardware) - Prepare Midterm Presentation
Midterm presentation.	
08/04	- Waiting for the PCB to be manufactured - Interface hardware/software (*Setup of Analog discovery 2* and *waveform*)

15/04	- Soldering of components
22/04	- Preliminary hardware setup and testing
29/04	- Hardware testing
06/05	- Hardware testing (with different comparator)
13/05	- Hardware testing (with different comparator)
20/05	- MATLAB coding for analyzing power consumption
07/06/19	Final report submitted to lab.
Final presentation.	
21/06/19	Final grade is due at register.
05/07/2019	- Additional Testing
12/07/19	Final report for Spain

Table 1. Timeline

The only aspect to be commented regarding the timeline is that the testing took longer than expected due to delays and problems with the component supplier. The first issue was that the comparator was not in stock so the first tests were carried out with an OP777 instead of the one used in the simulations. The second tests were finally carried out with a more suited component though still not the desired one (Because of this some simulations had to be redone)

Economical costs:

Assets	*Price (CHF)*
Electrical components.	47.3 [1]
Comparator(was ordered separately)	3.25
Manufacture of the PCB (x2)	95.02
Total	145.57

[1] Out of this amount 36.02 CHF are costs coming from the converter(x2), which might be able to be surpassed in future design improvements.

Chapter 5 DEVELOPED SYSTEM

SYSTEM ANALYSIS

In order to understand the essence of the project, in the following section, the way in which neurons produce action potentials will be briefly explained. In addition, the difference between the design chosen and the one proposed in [1] will be presented by first explaining the circuit proposed by [1] as well as the parameters used to characterize it and secondly introducing the circuit proposed in this project.

ACTION POTENTIAL

Neurons have differences in the concentration of ions at both sides (in and out) of their membranes which in turn produce a difference of potential between the inside and the outside of such membranes called resting potential. In addition, these membranes are permeable to specific types of ions which means that they can open and let pass ions from the inside to outside and vice versa, consequently changing the voltage difference between both sides of their membranes. Hyperpolarization occurs when the resting potential which is usually negative, becomes even smaller. The opposite process is called depolarization and it's the one in which we are interested in this project. During depolarization the change of ion concentration due to a stimulus produces the resting potential to rise until it reaches a threshold value. At that moment, the neuron fires the spike or the action potential whose shape can be seen in the figure below:

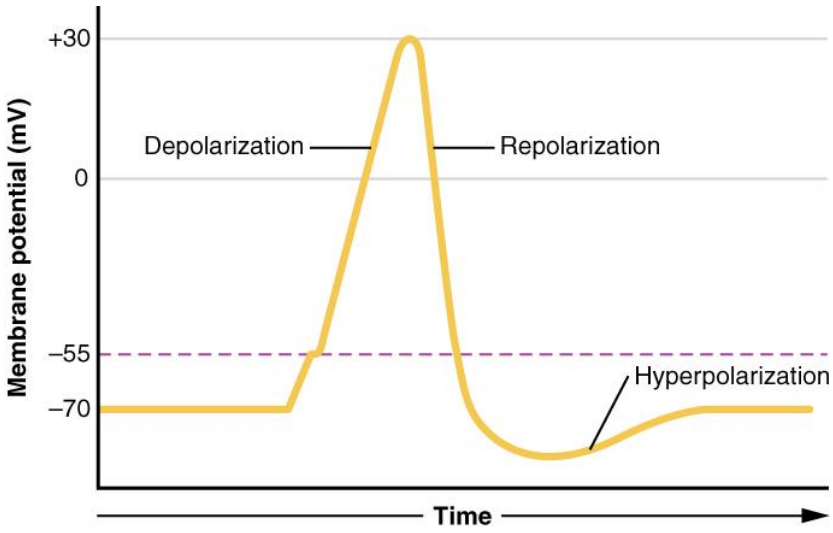

Figure 5. Action Potential [16]

There are two more relevant concepts regarding the project that happen with the firing of the action potential. The first one is that there is a period called the refractory period during which the neuron is not able to fire a second spike. The analogy with what happens in the design of the sampler is that there must be a minimum period between spike and spike given by the Nyquist theorem if the original signal is to be recovered. The second concept is that all spikes have the same amplitude regardless of the strength of the stimulus received. The conclusion to this fact is that there is no information coded in the spike's amplitude. In fact, strong stimulus fire multiple spikes and this is why it is believed by neuroscientists that the information is coded in the frequency of these spikes. In the introduction, it was mentioned that there are two main theories, this project follows the theory that defends Temporal coding, that is, that the information remains in the time sequence composed by the different spikes.

For more detailed information, the reader is directed to [3].

CIRCUIT BY A. LAZAR *ET AL* [1]

The circuit functions in the following way: first the input signal, the one that is to be sampled is summed with what is obtained at the output through the feedback loop. This signal which is a constant has values b or –b and it is used to bias in order to guarantee that the signal that enters the integrator is a positive increasing function of time (for b) or a negative decreasing function of time (for –b). If we are in the state in which we have –b, we will move from –δ to δ. When the integration reaches δ we will obtain an output that will go from –b to b.

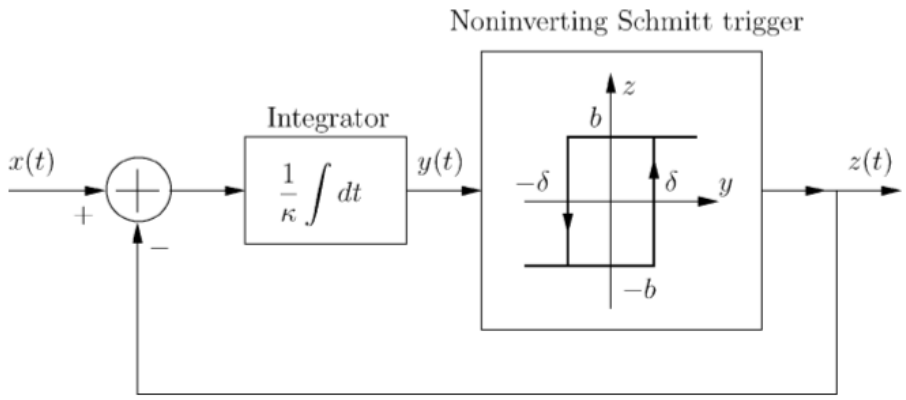

Figure 6. Block Diagram by A. Lazar

When observing the output signal of each block in *Figure 7* the effect of the added bias b can be observed in the slopes of the saw-like signal $y(t)$. When b is summed the integration will be faster and so the slope steeper, while the opposite happens when we subtract b. The peak in which the slope changes represents the moment in which the threshold δ has been reached, making the square signal $z(t)$ to have a positive value, in the case of the figure this value is equal to one. Thus, these squares represent the spikes produced by neurons. In [1] it is also mentioned a few constraints for the parameters δ and b.

- $|x(t)| < b$
- $|y(t)| \leq \delta$ to ensure stability.
- "To achieve perfect reconstruction the distance between two consecutive trigger times has to be in average smaller than the distance between the uniformly spaced

samples in the classical sampling theorem" [1]. In other words, there is a maximum distance between spike and spike if the signal is to be recovered correctly.

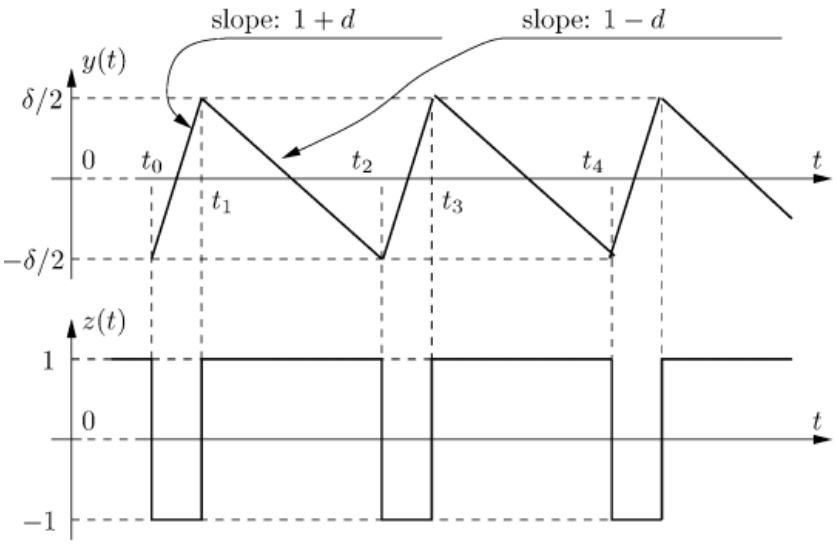

Figure 7. Outputs of integrator and trigger [1]

CIRCUIT PROPOSED BY THE PROJECT

The implementation proposed in this project differs from the one in [1] mainly due to changing the Schmitt trigger with a comparator and adding a differentiator. This is done in order to avoid the slow transition seen in $y(t)$ of *figure 32*. Instead of biasing the signal with two different values of b, the aim is to subtract this b so as to reset the integrator.

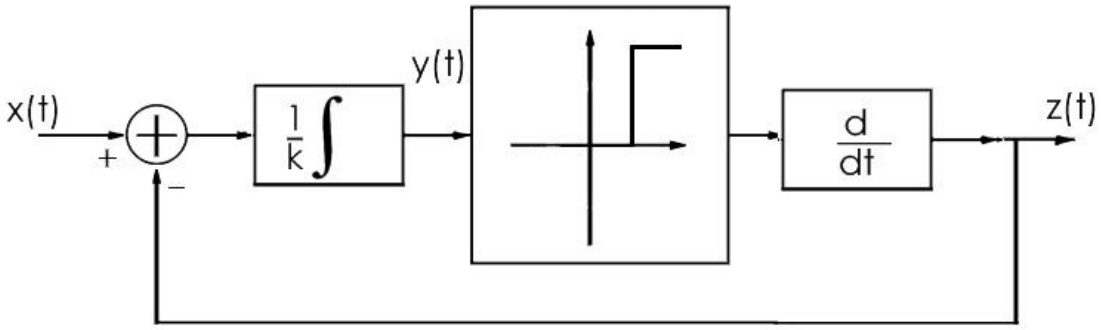

Figure 8. Diagram proposed by the project

In the following figure, the explanation above might be seen more clearly:

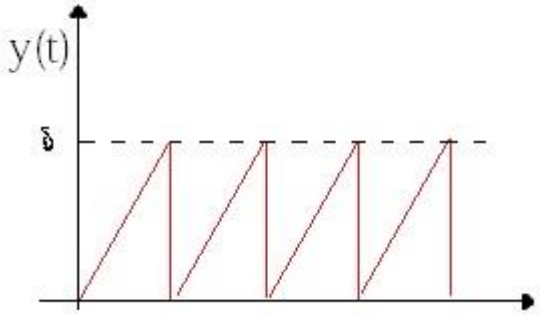

Figure 9. Desired integrator output

The constraints mentioned in section **CIRCUIT BY LAZAR *ET AL*** still apply if an accurate recovery is meant to be done.

The purpose of the following images is to show with images obtained from simulations how the output signals at each of the circuit stages should look like.

Input signal:

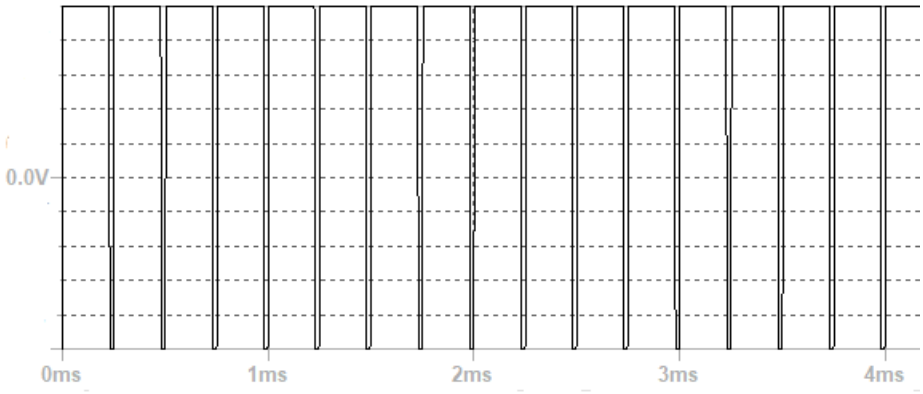

Figure 10. Simulation Input Signal

Integrator Output multiplied by -1

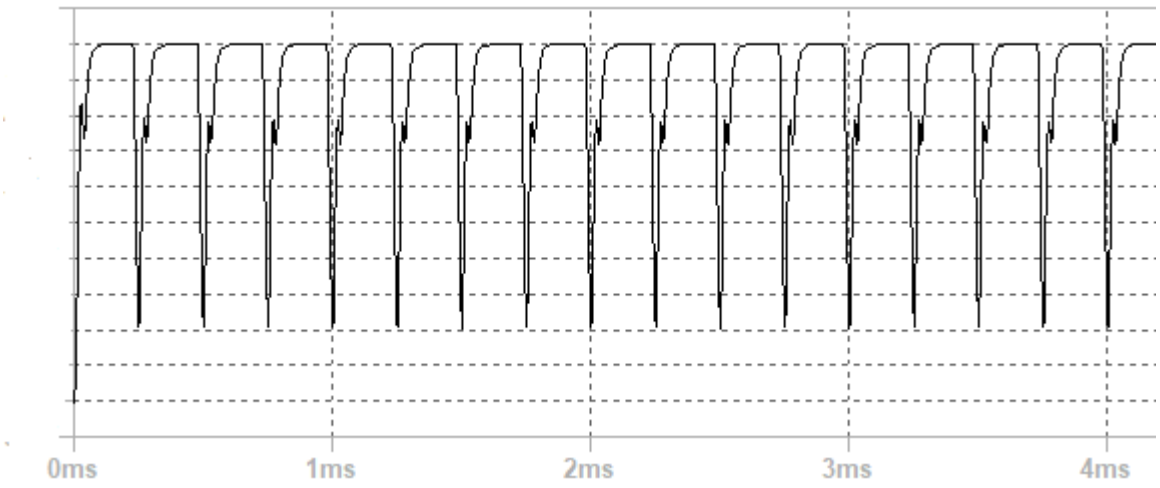

Figure 11. Simulation: Input to the Comparator

Differentiator output:

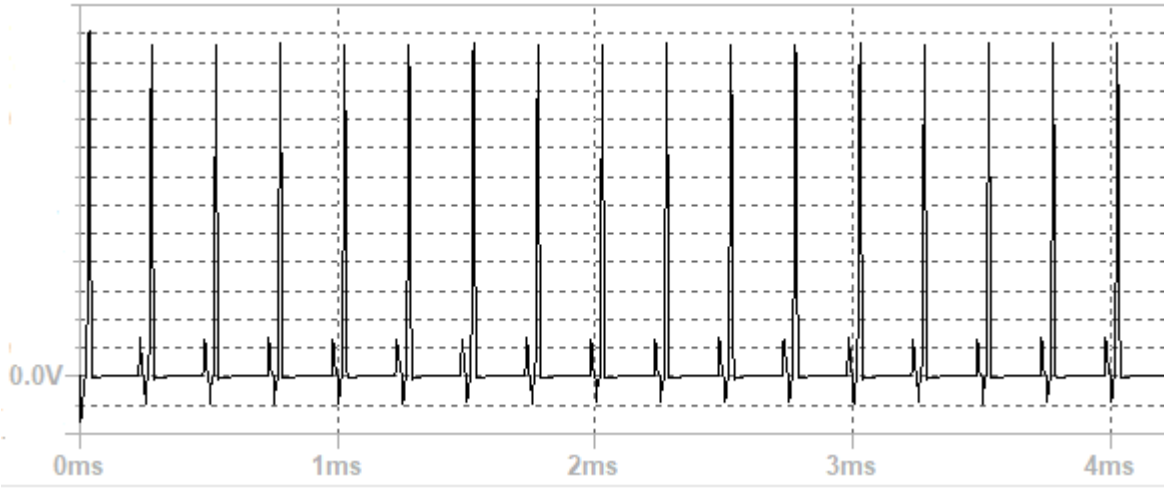

Figure 12. Simulation: Output Signal

DESIGN

INTEGRATOR BLOCK

Integrators are well known structures in electronics and are composed by an operational amplifier and a feedback loop composed of a capacitor and a resistance in parallel. As it can be seen in *Figure 14* this integrator is also used as a summer. It concretely sums three different signals.

- *V1* aims to represent the input signal that is to be sampled. The input signal will be audio signals of bandwidth $\Omega = 4kHz$ and of an amplitude between -2.5V and 2.5V which is the limit of the microphones that will be used in the tests.

- *V_out* represents the output signals of the circuits i. e the spikes or action potentials which are fed back to the circuit and summed up to the input signal with the purposed of serving as a reset. The spikes already have a negative sign at the output of the differentiator and this is why these signals are summed instead of subtracted as it appears in the block diagram. The purpose

of the reset is to discharge capacitor *C1* which is the one in charge of making the integration.

- Finally, on the top left corner of the image we can see a voltage divisor. The purpose of this third input signal is to create an offset of 2.5V so as to move *V1* into a positive range to guarantee that the signal to be integrated is always positive and thus the output is a positive increasing function of time. This has been done this way because the ultimate objective is to use this circuit with a microphone that outputs 5V peak-to-peak.

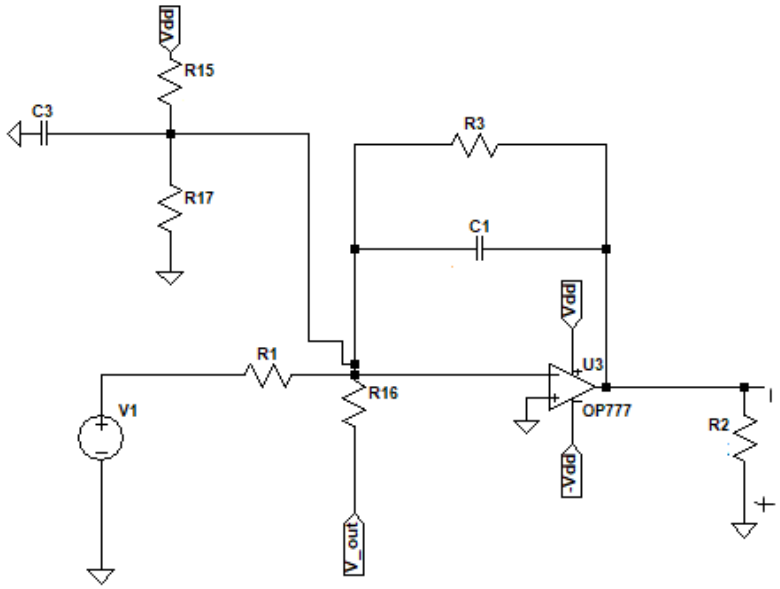

Figure 13. Integrator block

CHOOSING C1

So as to decide the correct value or range of values for capacitor C1 we must take into account that integrators work also as low pass filters. This is important because since the objective is to work with audio signals, we are expecting to sample signals that have

frequencies between 20 Hz and 40kHz. Therefore, our first constraint is met with the cut frequency of filters:

$$f_c = \frac{1}{2\pi RC}$$

$$C = \frac{1}{2\pi R f_c}$$

Finally, the capacitor chosen was of the order of nF as smaller orders of magnitude didn't provide the desired range and larger orders (pF) didn't give the desired circuit behavior, especially with the lower frequency signals.

In the following figures we can see the output of the integrator for different capacitor C1 values. In *Figure 14*, it is shown the output of the signal for the integrator when a 15kHz sine is fed to the circuit. The fact that the ripple goes than faster than the normal behavior is due to the spikes resetting. In *Figure 16*, the output of the integrator shown is the result of changing C1 from 10nF to 1µF. In this case the signal obtained is a more similar to the classical signal used to represent the charge of a capacitor. Again, the effect of the spikes can be seen marked by the red circle.

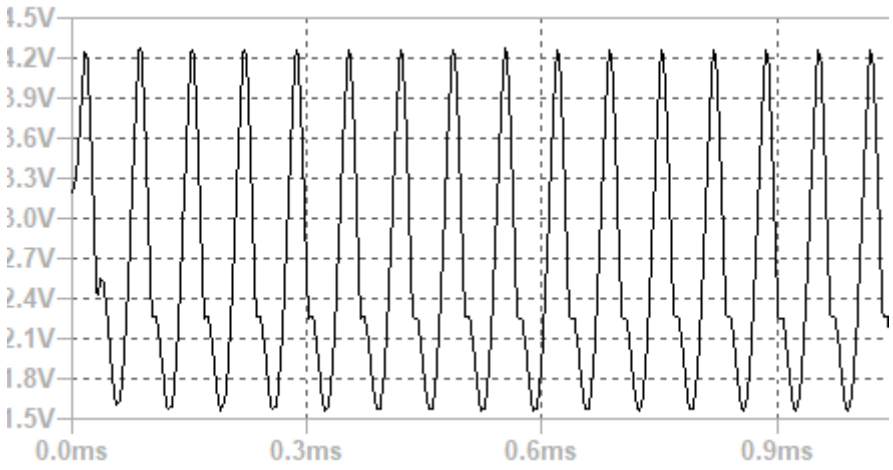

Figure 14. Integrator Output with C1 = 10nF

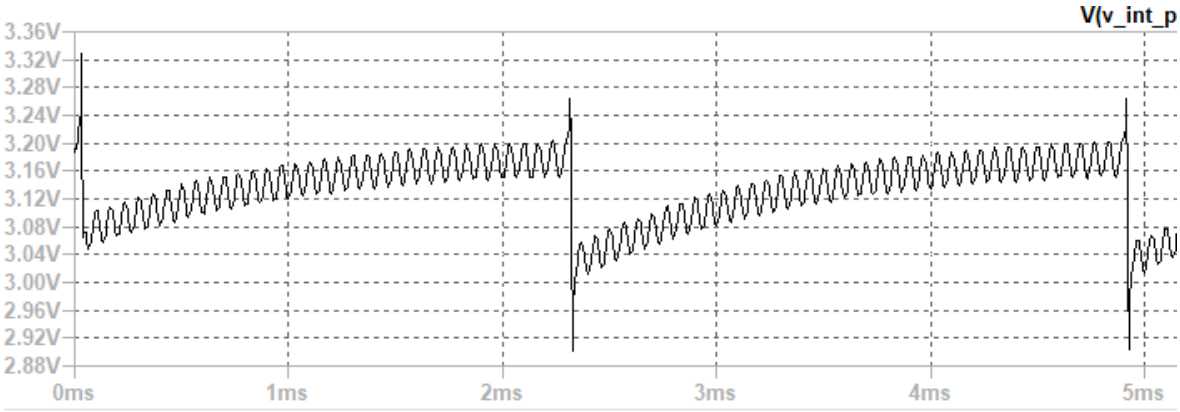

Figure 15. Integrator Output with C1 = 1uF

The act of changing the capacitor to a bigger value means that the circuit, concretely the integrator will have a slower response and thus ultimately less spikes. The different in the number of spikes fired can be seen when comparing *Figure 16* and *Figure 17*. For this first prototype a faster response was chosen, which doesn't mean that a slower one would be incorrect or not useful to recover the signal.

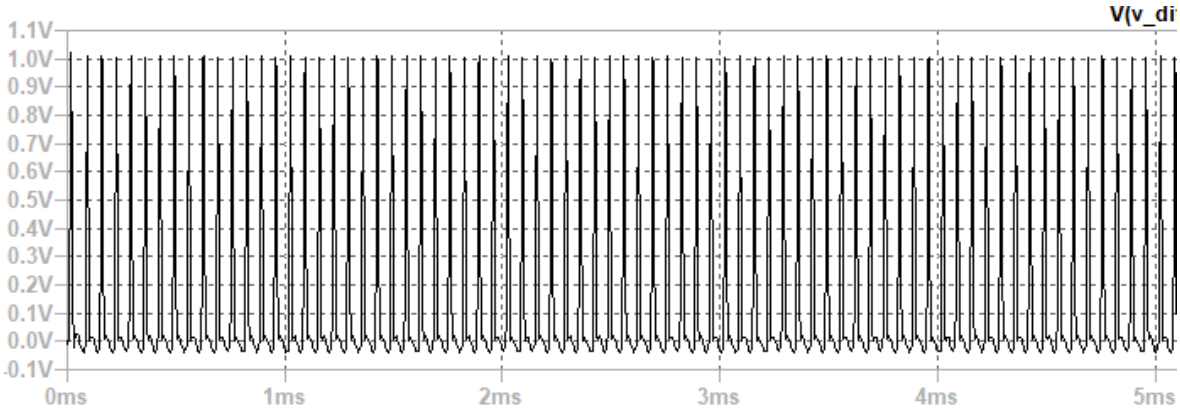

Figure 16. Circuit Output with C1 = 10nF

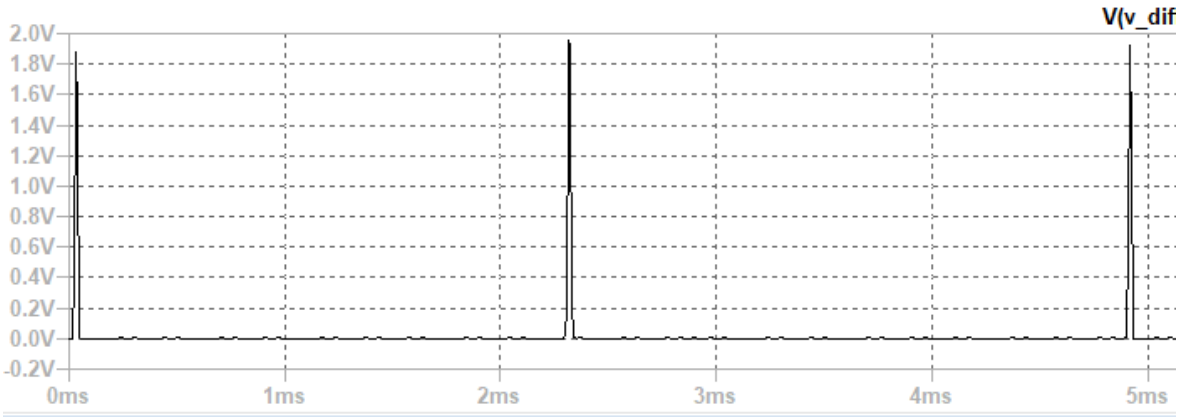

Figure 17. Circuit Output with C1 = 1uF

COMPARATOR BLOCK

The comparator mimics the function of firing the action potential once the threshold is reached and it has two sub-blocks: the first block corresponds to a multiplier and the second block is the comparator itself.

The first block multiplies the output signal of the integrator by a factor of -1. This is because the integrator inverts the signal making the output of the integrator negative. Since when doing a real implementation is easier to work with positive voltages (also easier to produce them) I decided to add this extra block for the comparator.

The second block is a common comparator whose negative input pin is connected to *V4*. *V4* is the δ parameter mentioned in section 5.1.2, in other words the threshold which if surpassed will trigger the action potential. In this case, what happens is that the result of the integration of the integrator block is compared to the threshold and if it is larger, the operational will be saturated positively. If it is lower, the operational will be saturated negatively if we are working with dual supply or cero if we are working with single supply.

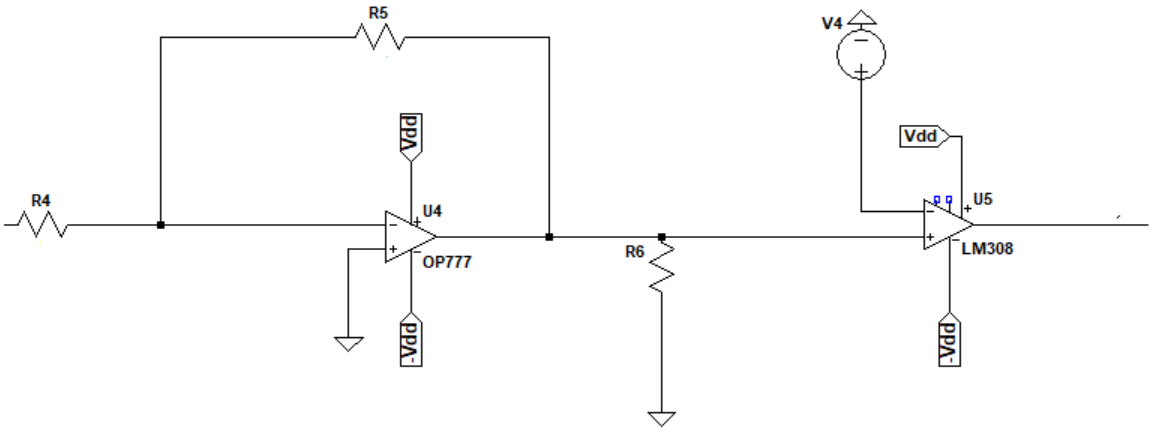

Figure 18. Comparator block

V4 which in this paragraph will be referred to with δ for practical reasons, was said in previous sections to be used to ensure that the time between spikes was respected. However, in the results made through the simulations one can observe that δ is restricted to some values. In *Figure 15* the traces of the subtraction of the spikes to the input signals can be seen circled in red. This is caused because the spikes are subtracted to the input signal with certain delay.

If the threshold is placed too high, too close to this area we will obtain undesirable results as two spikes will be fired. Indeed, the threshold will be surpassed twice, which we want to avoid. It is yet to be seen if this phenomenon seen in the simulations will actually have an impact on the real implementation.

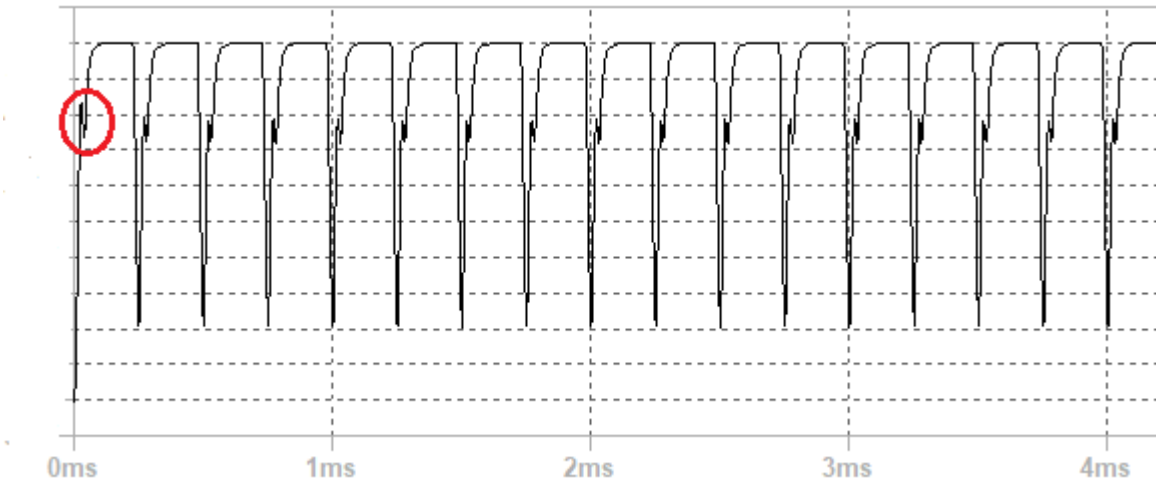

Figure 19. Comparator Input

When the δ parameter is chosen wisely, this is what it is obtained at the output of the comparator.

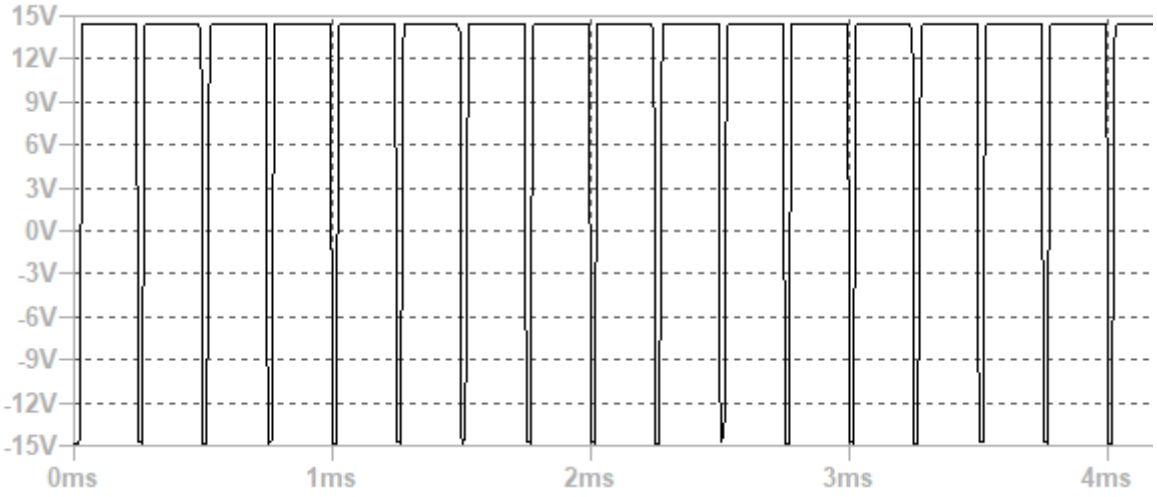

Figure 20. Comparator Output

Note: It can be noted from the voltage values in the y axis that the selected supply for the operational amplifiers in the simulations is a dual supply.

DIFFERENTIATOR BLOCK

The differentiator is meant to derivate the output seen in *Figure 16.* However, it must be taken into account that we are only interested in the positive saturation values of the comparator as only these ones will come from actual threshold surpassing. As a consequence, we must look carefully at the output signal produced by the differentiator and compare it to the one of the comparator:

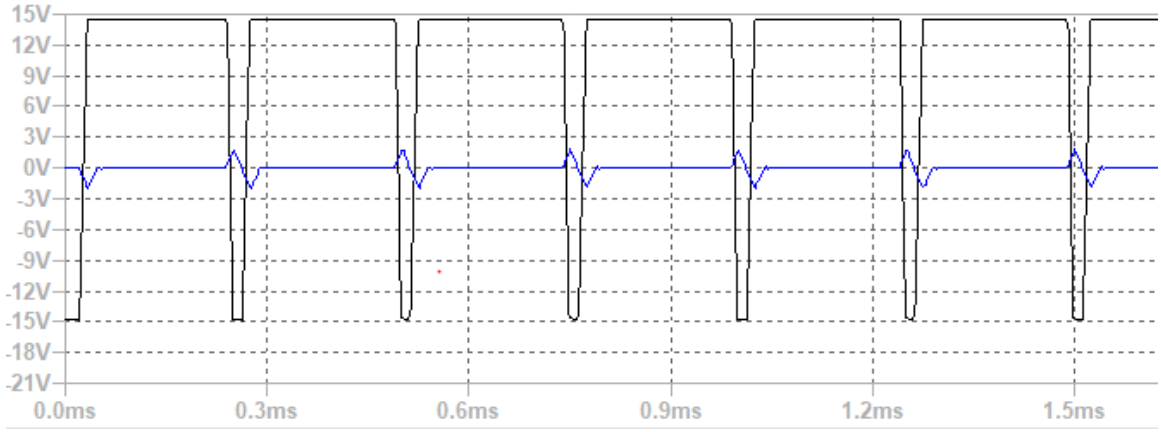

Figure 21. Comparator Output vs Differentiator Output

One may think that the positive spike comes from differentiating the positive value of the square signal and that the negative comes from differentiating the negative value, however, we must recall that the differentiator as well as the integrator circuit multiplies the circuit by a negative factor. As a result, the spikes that correspond to the correct firing are the ones with a negative value which is the reason why a diode has been placed at the output of the block:

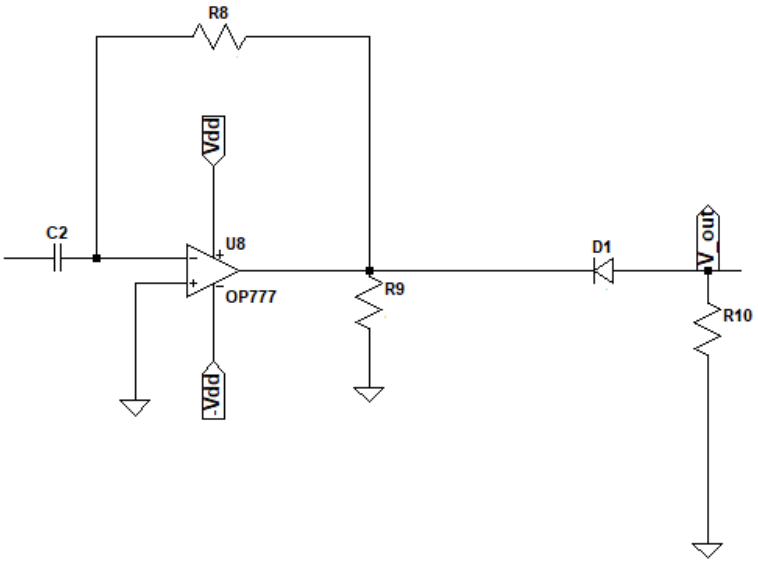

Figure 22. Differentiator Block

Another detail that can be observed from *Figure 17* is the loss of signal gain after differentiating it. This is explained with the formula that describes the gains of differentiators:

$$G = \frac{R_8}{X_{c2}}$$

$$G = \frac{R_8}{\frac{1}{\omega C_2}}$$

The differentiator works as a high pass filter meaning that the capacitor used in this case will be of the order of pF which as it can be inferred from the formulas above reduces the gain considerably. Consequently, a very large resistance is needed (of the order of 100kΩ) and even so, the loss is of approximately ten times that of the original voltage. Adding higher resistances does not help as much as it could be thought since it has been observed during the implementation that this part of the circuit is no longer linear i.e, having 300kΩ instead of 100kΩ doesn't result in 3 times more gain.

The criterion to choose the value of the capacitance was made once again with the cut off frequency. As it was mentioned, the difference is that in this case the differentiator performs as a high pass filter, this is why it can be used to derivate the signal, in this case the constant value(f=0) at the operational saturation point. Since the resistance seen by the capacitor is very large (that of the input resistance of the operational), the capacitance must be very small. The simulations have shown that with a range of pico-farads the objective is achieved.

The figure below shows the total output of the circuit. The only aspect to remark is that the differentiator output has been multiplied by a factor of -1.

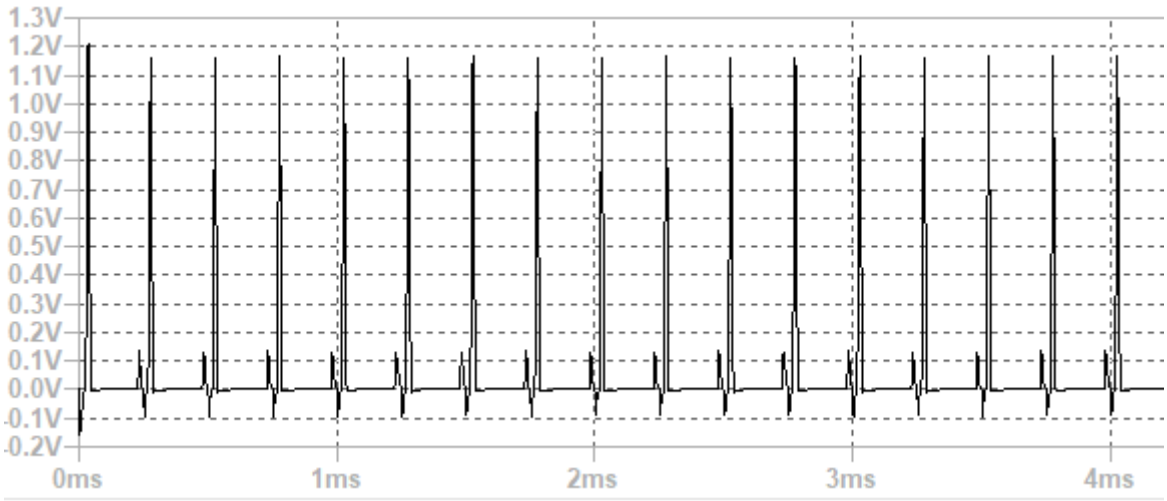

Figure 23. Output Signal

IMPLEMENTATION

This section will describe the PCB design and final real PCB obtained. For the design of the PCB KiCad was the choosen tool which is an open source, free program. It was developed by Jean-Pierre Charras and it allows the direct translation from the schematic design to the PCB design. It also allows to create, edit and add footprints and the generation of gerber files which are the ones needed to manufacture the PCB. The link to download the software is the following: **http://kicad-pcb.org/download/**

Image of Schematics

In the schema of the circuit seen in *Figure 20* the aforementioned blocks can be seen as well as two extra components: connectors and a converter. The converter is used to achieve the positive and negative voltage needed to feed the operational amplifiers.

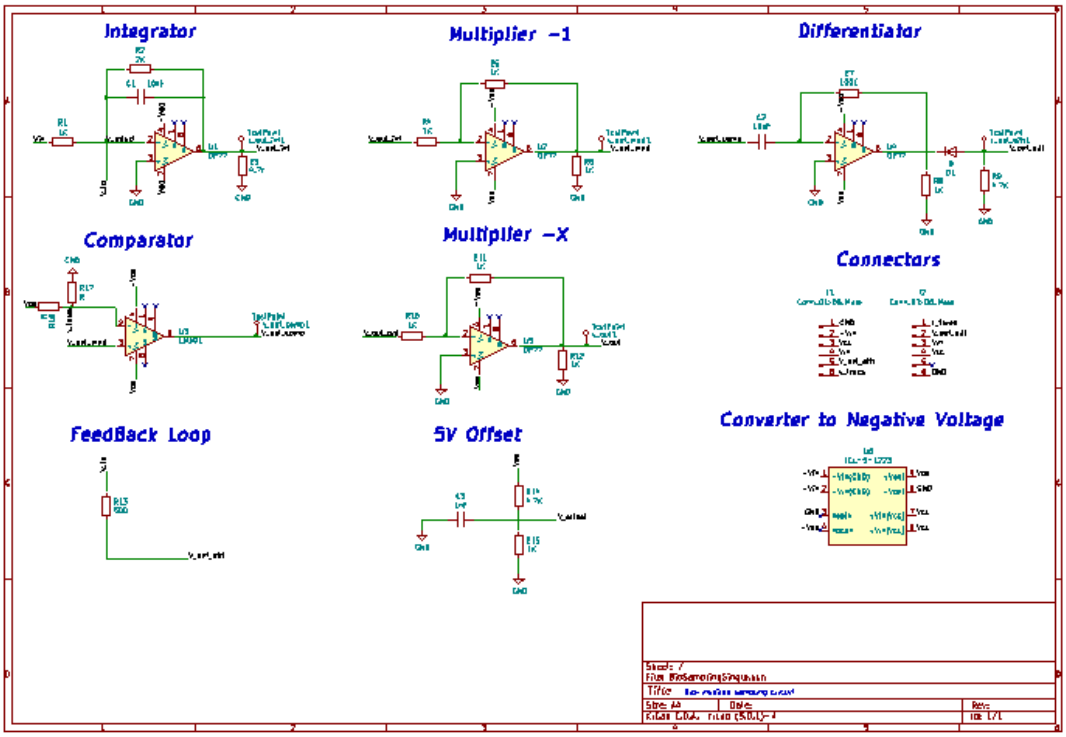

Figure 24. PCB Schematics

Image of PCB layout and 3D vision

The following figures show the PCB layout and the 3D vision provided by KiCad.

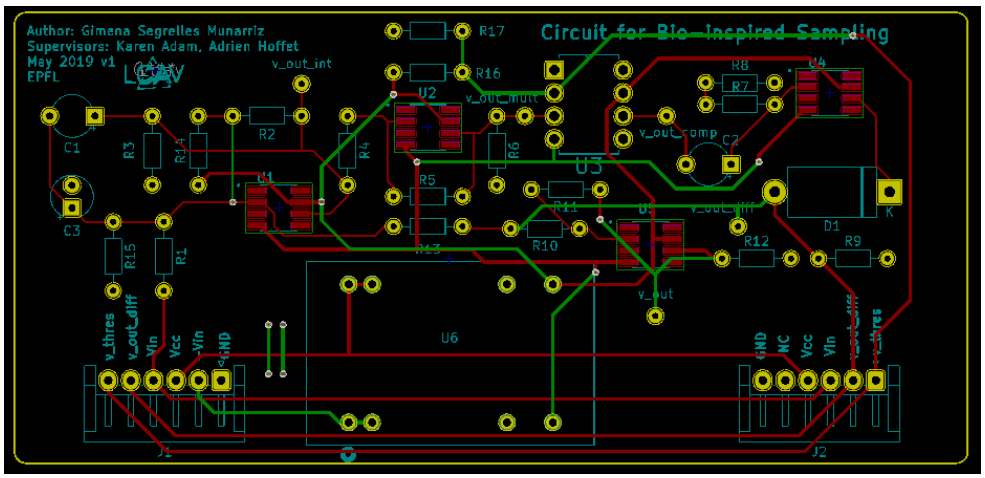

Figure 25. PCB Layout

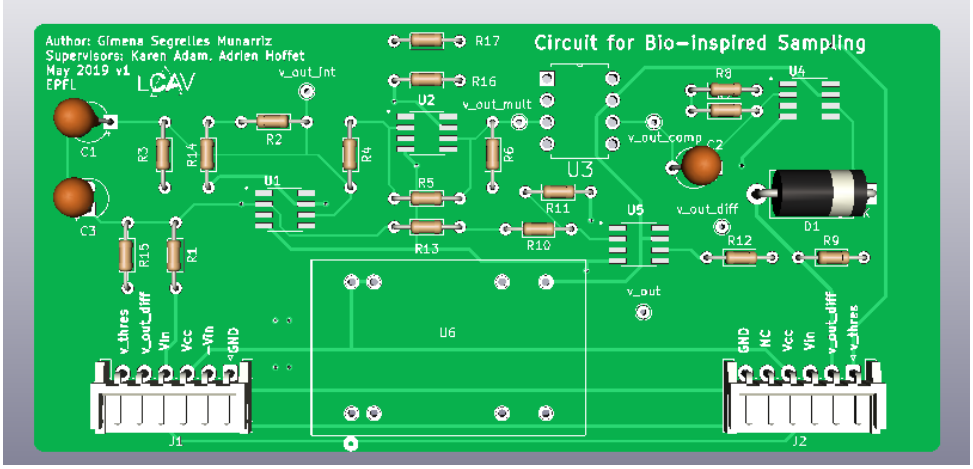

Figure 26. PCB 3D Vision

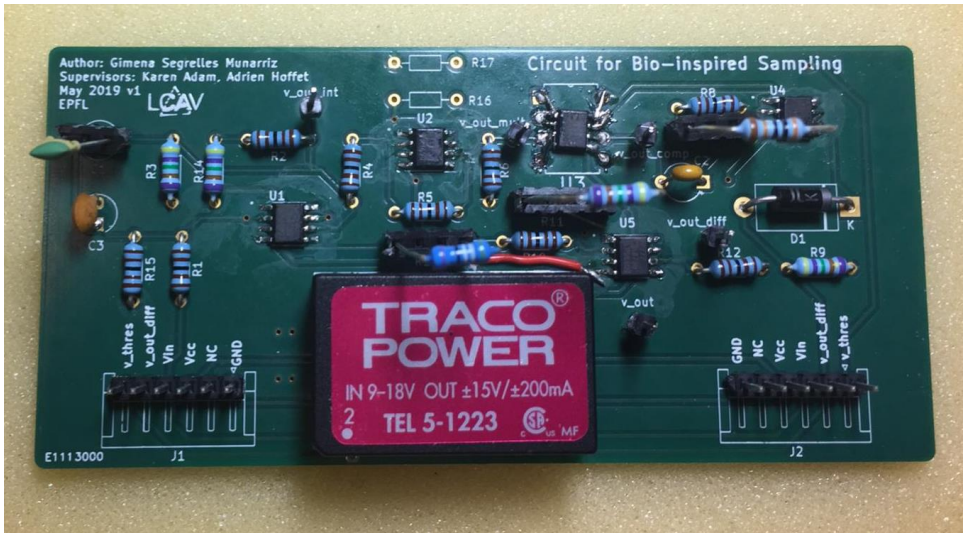

Figure 27. Real PCB Image

Table of component values

The following table contains the final chosen values for the different components of the circuit. R_{16} and R_{17} are auxiliary resistances for when a fixed value of δ is decided and thus avoiding the need of an external supply.

Components	*Values*
C1	10nF
C2	18pF
C3	1nF
D1	-
J1, J2	Conn_01x06_Male
R1 - R15	1K
R2	2K

R3	4.7K
R7	100K (subject to changes)
R9, R14	4.7K
R13	500
R16, R17	No value
U1 - U5	OP777
U3	LM301
U6	TEL-5-1223

Table 2. Components

Chapter 6 RESULT ANALYSIS

In order to test the circuit, each stage or block was built and tested one after another. Once the whole circuit was built the correct functioning of the circuit was assessed with sinusoids of various frequencies. One important note is that due to logistic issues from the company providing the electronic components, the first tests were carried out without the selected comparator (LM308) and operational OP777 was used instead. Because this operational is not fast enough the tests realized were limited to low frequencies as OP777 performs like a filter for frequencies higher than 2kHz. This inconvenience will be depicted in the empirical measurement outputs obtained for each stage. A second set of test were made when the correct component was finally provided, however, the results of firsts tests (setup 1) have been added even if the only information useful provided by them is the impact of not choosing the right component can have. Therefore, setup 1 corresponds to the circuit in which OP777 was used as a comparator and setup 2 corresponds to the one using the correct comparator.

For the testing of both setups, an *Analog Discovery 2* was used instead of a classical oscilloscope as it has multiple advantageous features. It allows to generate custom signals by either using the user's interface it provides or scripting them manually as well as measuring signals and save them in image format directly in the computer. For the 15V supply required for the amplifiers an external voltage generator was used.

SETUP 1

The following images correspond to the signals measured in different points of the circuit for an input signal $\sin(2\pi \times 2000t)$ and $\delta = 3.5\,V$.

Integrator output:

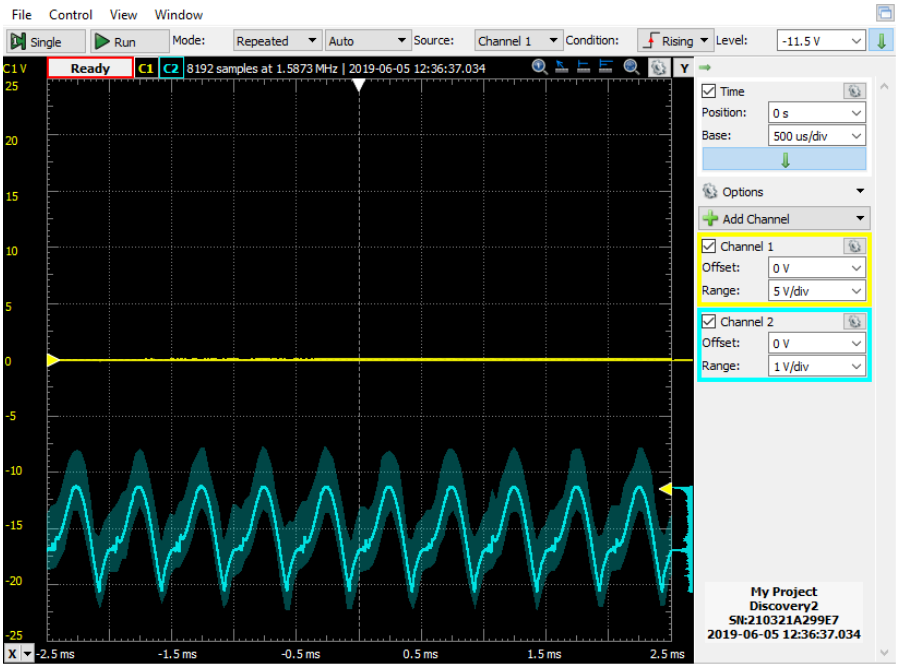

Figure 28. Integrator output with Feedback applied

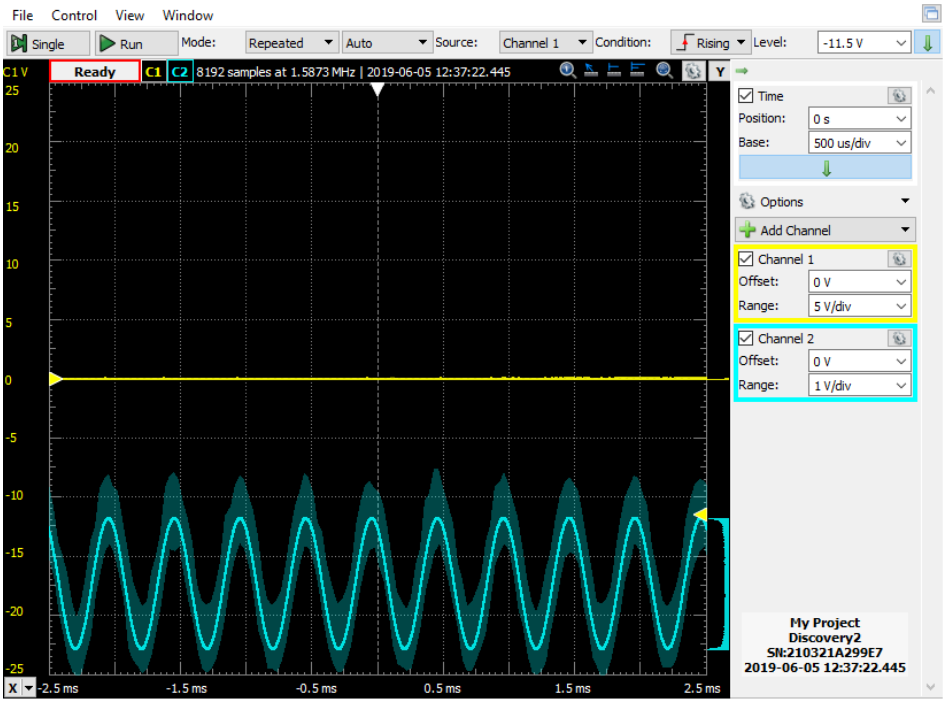

Figure 29. Integrator output with no Feedback applied

When comparing *Figure 24* and *25*, the effect of the reset due to the spikes can be seen. The falling slope is much faster in *Figure 24* than *25*.

Comparator output:

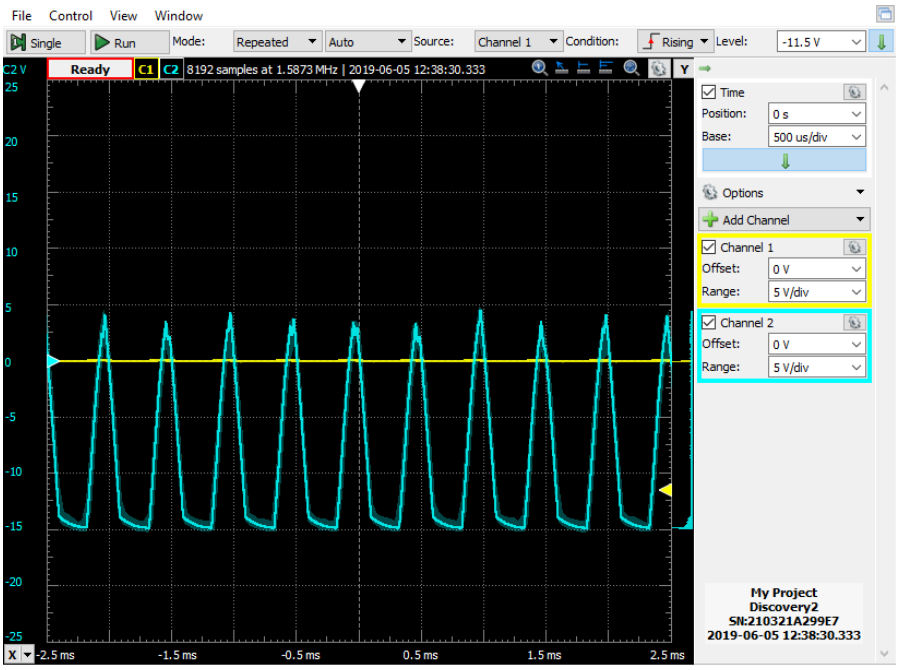

Figure 30. Comparator output

In Figure 26 is it visible what was previously described regarding the operational OP777 used as a comparator. It can be seen that the signal is too fast and that it cannot reach both saturation levels. The signal starts in $-15\,V$ when the integrator output is below the threshold, when it is above, the signal starts growing towards $15\,V$ but this value is never reached.

Differentiator output after the diode

Figure 27 and *28* show the output signal of the differentiator right after the diode. The difference between *Figure 27* and *28* is that the first one had a C1 capacitor value of $47nF$ while the second had $10nF$. As it was mentioned in **INTEGRATOR BLOCK** the integrator circuit behaves as a low pass filter and so the bigger the value of the capacitor the

lower the cut frequency will be. Spikes are high frequency signals, so they will be better filtered with larger capacitors.

It can also be observed in *Figure 27* that the shape of the signal is not exactly that of a spike. This is due to the fact that the comparator output behaves strangely and does not have a perfect square shape.

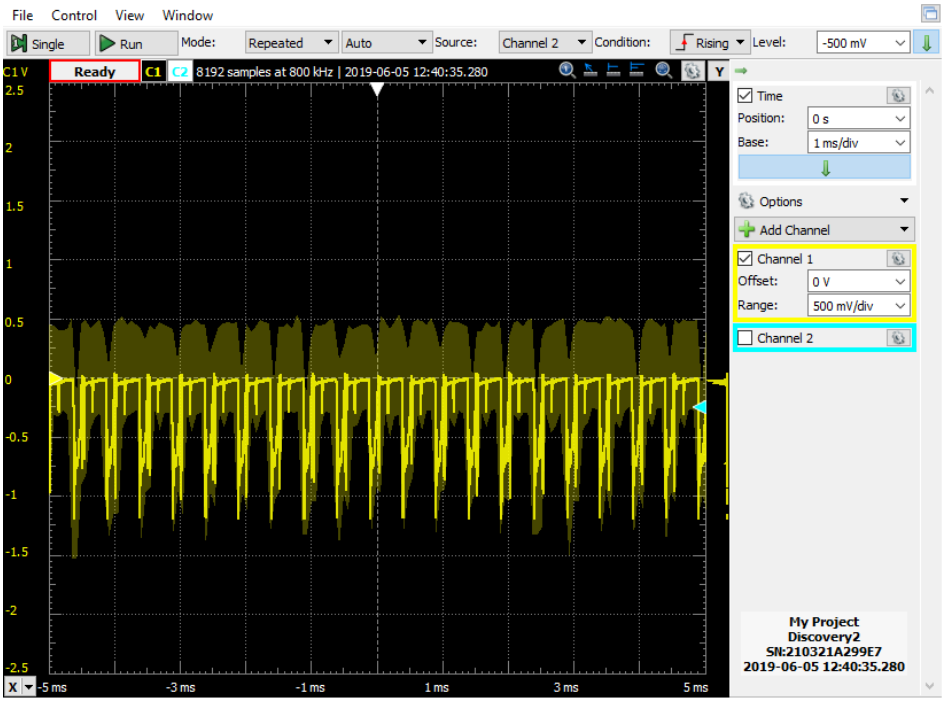

Figure 31. Output Signal after diode 47nF

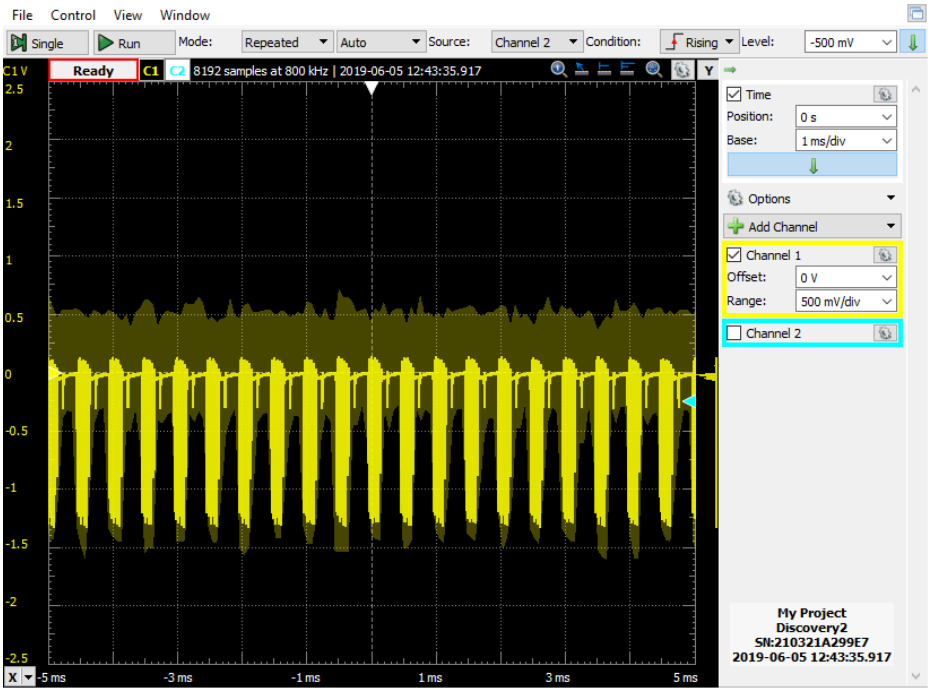

Figure 32. Output Signal after diode 10nF

Final output

Figure 29 shows the final output of the circuit inverted and amplified, this signal will be the one used for the recovery of the original signal.

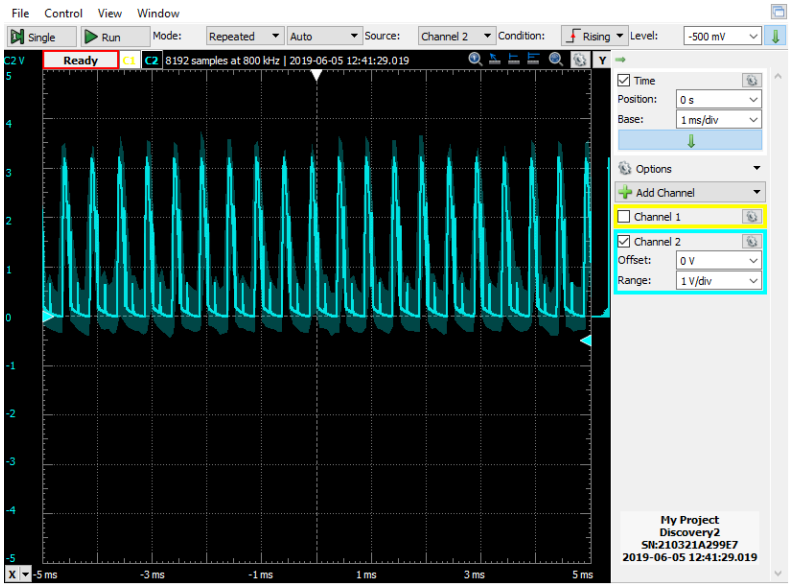

Figure 33. Circuit total output

Trigger and Spike

The first thing to clear about this image is that they are being represented at different scales. In reality the yellow signal i. e the spikes are approximately 15 times smaller than the blue signal. What is interesting about this image is to see that when the comparator is triggered and saturates, we obtained the desired spike.

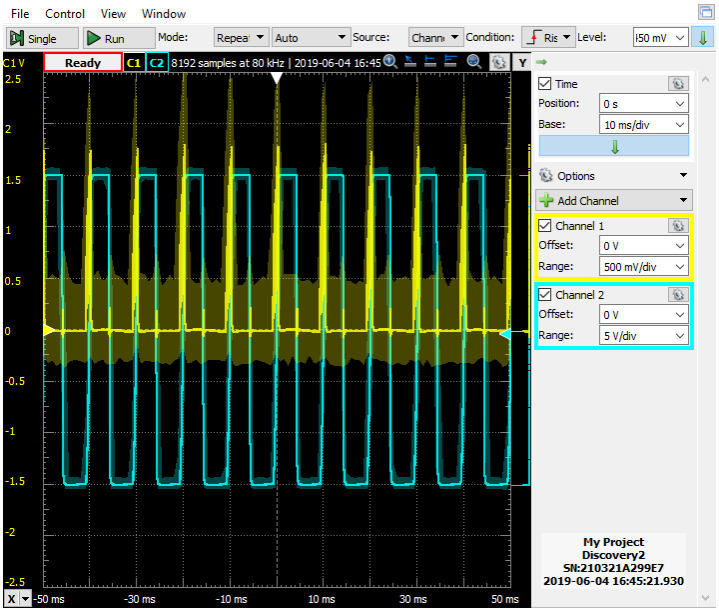

Figure 34. Comparator vs Differentiatior Output

SETUP 2

With this setup a wider range of frequencies was tested being the maximum one 10kHz which is still not the highest one tested in the simulations.

TEST A

In this test the signal fed to the circuit is a simple 2V DC signal, like the one proposed on the paper and used to describe the desired behavior of the circuit. If we recall what was described in Chapter 5. System Analysis section 3, the reason why the design from [1] was changed was that one of the aims of the circuit was to obtain a saw-like signal at the output of the integrator with no other purpose than resetting C1.

In *Figure 31*, when observing the blue colored signal, one can see this saw-like signal shape. Here the effect of the reset is clearly shown for if there was no reset, the integrator's capacitor would be charged only once and we would see a DC voltage at the integrator's output instead of this oscillating signal. As a consequence, we would not obtain the train of

spikes seen in the yellow signal of the figure. Moreover, there is a second detail to be mentioned and that is that indeed C1 is reset but not completely. When observing more thoroughly the blue signal in *Figure 31* it can be seen that it does not go down to zero and this is due to the fact that the spikes that are being fed back to the circuit need to be amplified. Even though for this simple signal this effect might not be too consequential it might for some more complex signals as it will be shown in following tests.

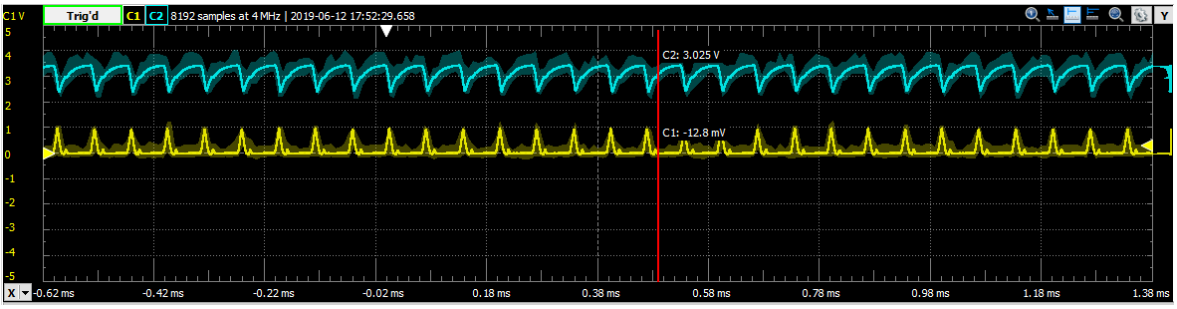

Figure 35. Test A comparator and circuit output

TEST B & C

For these tests two signals were fed to the circuit: firstly, a $2 \times \sin(2\pi 5000)$ and secondly, a $2 \times \sin(2\pi 10000)$.

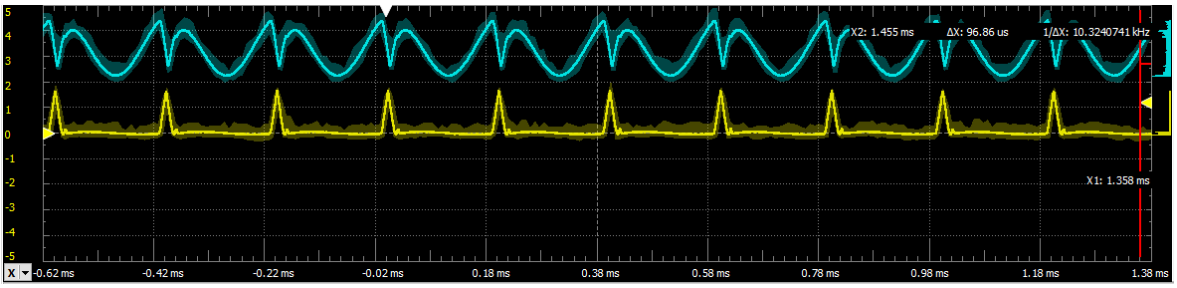

Figure 36. Test B 5kHz sine input

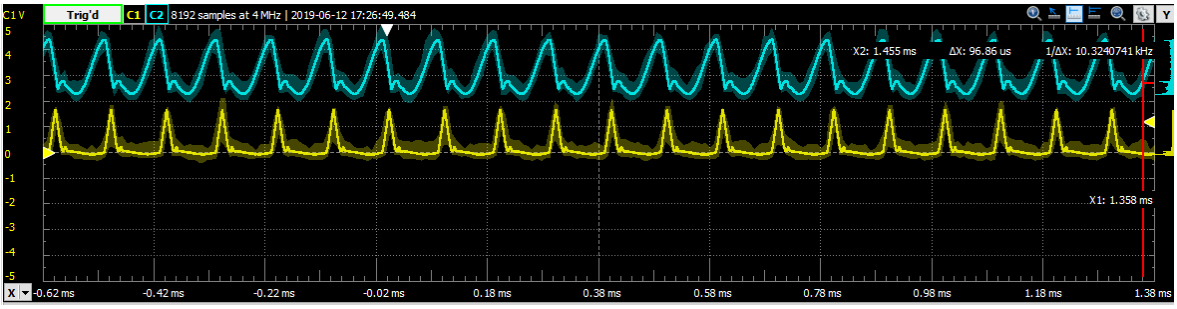

Figure 37. Test C 10kHz sine input

In *Figure 33* one can again see the saw-like shape but also that the reset does not go fully to zero. The fact that the spike needs to be amplified in the feedback loop is more visible in *Figure 32* because the ripple due to the 5kHz signal is wider (slower) than that of the 10kHz. The spike which is not precisely wide is not large or significant enough to really discharge the capacitor. This has a direct consequence on the threshold δ value. If a too low value is chosen there is the possibility that two spikes are fired consecutively due to the two lobes. Consequently, the two spikes would be fed back to the circuit and since they would be practically no time between both of them, at the output of the integrator would have three of these lobes instead of two. Again, if the threshold is too low, the amount of fired spikes would grow and grow as well as the number of lobes and this is an incorrect behavior of the circuit.

TEST D

Figure 34 shows the output signals of the comparator and the circuit when a random signal of 10kHz was injected. The threshold δ value was 3.5 V, which was the same as when the 10kHz sine was fed. A remark to make of these result is that one can appreciate a certain delay between the moment the integrated signal surpasses the threshold and the moment the spike is obtained, which of course has an impact on the feedback and the rest. In addition, not all amplitudes are the same. A possible explanation for this is that the comparator though with a wider bandwidth than in the one used in setup 1, is still not fast enough to saturate properly positively and negatively like it did in the simulations. As a consequence, for parts

where the signal stays above/below the threshold for a longer time, the comparator will reach higher or lower values and the spikes will have different amplitudes.

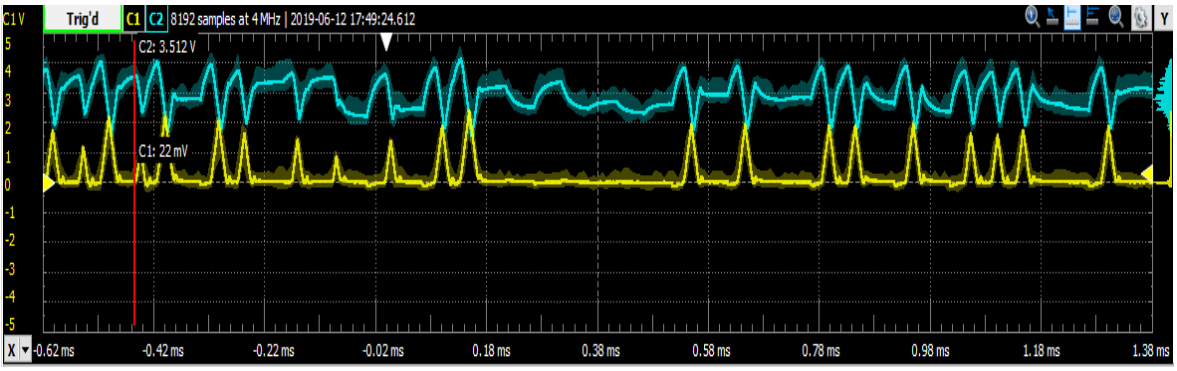

Figure 38. Test D 10kHz noise input signal

POWER CONSUMPTION

It was stated that one of the objectives of the project was to characterize the power consumption of the circuit to check that indeed consumes less power than current state of the art samplers. It must be taken into account that the results obtained are the results of the first design and implementation of this kind of sampler, therefore, a lot of optimization can be done regarding this feature.

The first analysis that was done regarding power consumption was an analysis using the data obtained from the simulations of the circuit performed using LTspice tool. The data was read and processed using a simple MATLAB script written by the author. The power consumption was assessed by averaging and summing up the power consumed by the resistors, the diode and the operational amplifiers. The final power consumed calculated was 0.352 W.

Of course the value of the simulation on its own is not enough, but it is useful so as to get a sense of the circuit. For the calculation of the power consumed by the real circuit the same method as for the simulations was used. The voltage for each power-consuming circuit

was measured and saved into a .txt file to be processed by a MATLAB script, just like in the case of the simulations. This is one of the reasons why *Analog Discovery 2 + Waveform* was used. Using these data, the average power consumption was calculated for each resistor and operational in an approximated way. The final values obtained are the following:

Component	**Power Consumed (w)**	**Percentage %**
Resistors and Diode	0.078	19.5
Operational Amplifiers	0.2925	73.4
Total	0.3987	100

Table 3. Power Consumption

The following figure shows the data for some resistors put into an excel file and its purpose is just to show a piece of the data extracted:

Component	value	avg voltage(v)	power(w)
R1	1k	0,76	5.9e-4
R2	4,7k	2.548	0.0013
R3	1k	2.623	0.0068
R4	1k	2.608	0.0068
R5	1k	2.615	0.00683
R6	1k	2.638	0.0069
R7	100k	0.511	2.61e-6
R8	1k	0.220	4.84e-6
R9	4,7k	0.14	4.17e-6

Figure 39. Extract of calculated powers

The last point to comment on the results regarding power consumption are related to the converter. It was observed in the lab that the component sinks 190mA at 15V which means it consumes 2.85W. It was more or less the expected power consumed that was read from the datasheet.

Chapter 7 CONCLUSIONS AND FUTURE PROJECTS

GENERAL CONCLUSIONS

In general, the main objectives of the project have been reached. The different blocks of the circuit behave as they should and give the expected outputs. In addition, the signals obtained at the output are not square like in [1] but do have a spike-like shape. It must also be mentioned that in order to meet the time constraints mentioned in **CIRCUIT BY A. LAZAR ET AL [1]** the circuit allows to dynamically set the value of δ. The power consumed is aproximately 0.4W which is acceptable for a first prototype.

Going more into the details of the project one can see that there are some things that didn't reach what was originally planned. For instance, the circuit of the simulations was designed to be able to work with signals that go from 10 Hz to 40kHz. However, in the real implementation due to the characteristics of the comparator the maximum frequencies at which the circuit can work are around 12kHz. Also related to the comparator, not all spikes have the same amplitude which is not too relevant for the recovery but was worth mentioning in order to highlight the importance of getting a better or more suitable component. Another fact related to the shape of the spikes is that for the same values and the same circuit, the spikes in the simulations were much narrower than in the real implementation. If this is actually a drawback or an advantage is yet to be analyzed.
The PCB was designed, manufactured and tested in time.

IMPROVEMENTS FOR FUTURE PROJECTS

Because of the HW oriented nature of the project, improvements are aimed towards the circuit design and not the quality of the signal recovery.

Feedback

In order to improve the feedback, it is necessary to amplify the spikes so that they have a bigger impact when subtracting them to the input signal. There are several ways in which they could be amplified:

(a) Increasing the value of resistance R8 shown in *Figure 34.* The value used in the simulations was of $100\text{k}\Omega$ which gave an output around $1V$, however, in the real implementation the output didn't reach the expected value and after passing through the diode it was even smaller. For this reason, the resistance was changed, though it is suggested to use a bigger one to have even more gain.
(b) This option consists on making the feedback resistance even smaller for the gain of the integrator is inversely proportional to this resistance.
(c) The third option is messier and more complicated but also possible: a two-stage amplifier could be added after the differentiator, one to amplify the signal, another so as to invert it back again.

It was also mentioned that another way to improve the reset for signals that are of lower frequencies ($f < 6.875\text{kHz}$) was to try to increase the spike's width. To do this there are also three main possibilities:

(a) Increase the value of C1, that is the capacitor of the integrator.
(b) Increase the value of C2, that is the capacitor of the differentiator and which is a better option than (a) from what was tested in the latest simulations. The value must be increased at least one order of magnitude, however, the problem then comes with high frequency signal, which start to perform worse as the value of the said capacitor increases. In addition, so as to keep the gain reasonable, the feedback resistor R8 of the differentiator must be decreased in value.
(c) The third solution is not related to the design of the circuit itself but to the chosen components, concretely the comparator. If a faster comparator is chosen, faster in the sense that it is able to saturate at its maximum and draw an almost perfect square signal then when differentiating, the width of the spikes will be large. This has been

tested and simulated, not by trying a faster comparator but by using lower frequencies with the chosen one.

Power

Regarding the dual supply during the implementation and the test of the operational amplifiers, it was checked that the components worked well for single supply setup and so did the circuit even though in the simulations this was not possible. Therefore, future prototypes could avoid the use of a dual supply and thus avoid the converter making the circuit simpler and more economical. It would also mean to get rid of 2.85W of power consumption which is quite a significant improvement taking into account that the rest of the circuit consumes 0.4W.

On the other hand, the power consumed by the circuit could have been compared to the power consumed by well-known samplers in the market, but it was finally decided not to due to the fact that the design of this circuit is in prototype phase and the comparison wouldn't be coherent. What it can be done and will be done for the following months is to improve the power consumption of the circuit in this case by detecting whether there is a signal at the entrance. If no signal is detected de DC bias will be switched off.

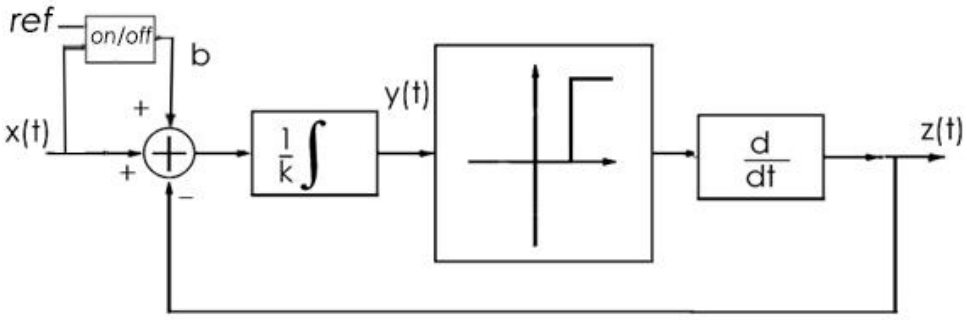

Figure 40. Power Improvement Diagram

Noise

In *Figure 17* one can observe the fine line that draws the signal as well as another blurrier one which represents noise. In our case, the noise that is added to the amplitude is of no

concern since what is important for the recovery of the signal is the time between spike and spike. The noise that will affect the quality of the recovery is the noise related to the sampling technique as well as to the precision at which these time stamps are taken by the sampler that will be used to convert the analog signal to digital.

Cost

In Chapter 4 the costs of the PCB were calculated and estimated to be around 145 CHF or 127 €. It is not precisely cheap, but as it was mentioned in ***Power*** the converter which is 32.4% of the cost is dispensable. Another high percentage cost is related to the manufacturing of the PCB itself which could be reduced by trying another manufacturer or mass production. It is also important to note that this 65.5% represents the cost for manufacturing 2 PCBs, not just one, and thus the price is not as high per PCB.

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ANEXO A

ESCUELA TÉCNICA SUPERIOR DE INGENIERÍA
I.C.A.I.

PROYECTOS FIN DE GRADO
CURSO:

Parte I Ficha de proyecto fin de grado

Titulación y optatividad: Ingeniería en Tecnologías de la Telecomunicación

Alumno 1º Apellido: Segrelles
2º Apellido: Munárriz
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Título del Proyecto Fin de Grado: Circuit design for bio-inspired sampling

Director (nombre y dos apellidos): Karen Adam
Teléfono de contacto: +41 21 69 37663
e-mail: karen.adam@epfl.ch

Breve descripción del proyecto (5 o 6 líneas)

Sampling is a key step in converting any analogue signal to the digital world. Usually, it is done by recording the signal's amplitude at certain predefined time points. In nature, sampling is done differently. A neuron integrates its input until a threshold is reached and then fires a spike. We want to mimic this behavior in hardware. The goal of the project is to build a time encoding machine in hardware.

The final report of the Project will be uploaded to the Comillas Institutional Repository with public access. The student will be able to ask for a restricted access (even "closed" or "confidential") which will be exceptionally accepted if it is fully justified.

Aceptación del Director (firma y fecha)