GRADO EN INGENIERÍA EN TECNOLOGÍAS INDUSTRIALES

TRABAJO FIN DE GRADO

DEVELOPMENT OF AN FPGA CONTROLLER FOR HIGH-POWER MULTI-MHZ CAPACITIVE WIRELESS POWER TRANSFER SYSTEMS

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MADRID

July, 2024

I declare, under my responsibility, that the project presented with the title

DEVELOPMENT OF AN FPGA CONTROLLER FOR HIGH-POWER MULTI-MHZ CAPACITIVE WIRELESS POWER TRANSFER SYSTEMS

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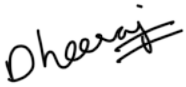
PROJECT DIRECTOR AND CO-DIRECTOR

Signed: Khurram Khan Afridi Date: 07 / 09 / 2024



Signed: Dheeraj Etta Date: 07 / 08 / 2024

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DESARROLLO DE UN CONTROLADOR FPGA PARA SISTEMAS CAPACITIVOS DE TRANSFERENCIA DE ENERGÍA INALÁMBRICA DE ALTA POTENCIA Y MULTI-MHZ

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Director: Afridi, Khurram Khan.
Co-director: Etta, Dheeraj
Entidad Colaboradora: Cornell University

RESUMEN DEL PROYECTO

El objetivo de este proyecto es el desarrollo de un controlador basado en una Matriz de Puertas Lógicas Programable en Campo (FPGA, por las siglas en inglés de *Field-Programmable Gate Array*) diseñado para aumentar las capacidades de transferencia de energía en sistemas de Transferencia de Energía Inalámbrica (WPT, por las siglas en inglés de *Wireless Power Transfer*) capacitiva para vehículos eléctricos. El proyecto se centra en generar múltiples señales de Modulación por Ancho de Pulsos (PWM, por las siglas en inglés de *Pulse-Width Modulation*) de alta frecuencia para controlar hasta 16 inversores. Los resultados experimentales demuestran que las señales PWM se mantienen estables cuando se emplean en múltiples inversores. La integración del controlador en un sistema de WPT capacitivo logró una transferencia de energía de 4 kW con una eficiencia del 86 %.

Palabras Clave: Controlador basado en FPGA, Transferencia de Energía Inalámbrica (WPT), Sistemas WPT capacitivos, Modulación por Ancho de Pulsos (PWM), Control de inversor, Señales de alta frecuencia.

1. Introducción

La Transferencia de Energía Inalámbrica tiene el potencial de aumentar la adopción de vehículos eléctricos (EVs, por las siglas en inglés de *Electric Vehicle*) al permitir la carga estática, semidinámica y dinámica, superando así limitaciones de coste, tiempo de carga y autonomía [1]. Los sistemas WPT inductivos tradicionales utilizan campos magnéticos y sufren pérdidas en el núcleo, lo que limita la frecuencia de operación y la posibilidad de reducción de tamaño [2, 3]. Los sistemas WPT capacitivos, que emplean campos eléctricos, pueden ser más pequeños, ligeros y eficientes a frecuencias más altas [4]. Sin embargo, la capacidad de transferencia de energía de los sistemas WPT capacitivos actuales está limitada a unos pocos kilovatios por las intensidades nominales de los transistores disponibles comercialmente [5].

2. Planteamiento del Problema

El grupo de Laboratorio de Electrónica de Potencia de la Cornell University, liderado por el Profesor Khurram Afridi, ha estado trabajando en sistemas WPT capacitivos. Para lograr altas capacidades de transferencia de potencia en estos sistemas se necesitan múltiples inversores.

Cada inversor contiene cuatro transistores que deben ser controlados mediante señales PWM. Actualmente, el único método disponible para generar señales PWM de alta frecuencia en el grupo es a través de generadores de señales. Sin embargo, la cantidad limitada de estos dispositivos en el laboratorio restringe el número de inversores que pueden utilizarse en sus proyectos.

Para aumentar las capacidades de transferencia de potencia e incluir más inversores, se necesita un nuevo método de generación de señales PWM. Además, las inconsistencias en los semiconductores y los distintos diseños pueden resultar en desequilibrios en las corrientes de salida cuando se conectan en paralelo múltiples inversores, lo que degrada la eficiencia total. Varias redes combinadoras de potencia, tales como combinadores de potencia basados en redes de admitancia, y arquitecturas de inversor apilado, han sido propuestas [6, 7]. Sin embargo, aún se necesita una solución efectiva para generar y gestionar las señales PWM requeridas para un gran número de inversores.

3. Solución Propuesta

Este proyecto tiene como objetivo desarrollar un controlador FPGA capaz de generar32 señales PWM para sistemas WPT capacitivos de varios megahercios y alta potencia. Este controlador permitirá el uso de hasta 16 inversores simultáneamente, mejorando las capacidades de transferencia de potencia. Asimismo, el controlador podrá recibir hasta 8 señales analógicas, para futuros controles de lazo cerrado. La elección de una FPGA sobre un microcontrolador se debe a los requisitos de alta frecuencia de los sistemas WPT capacitivos.

4. Objetivos

Los objetivos del proyecto son los siguientes:

- Probar el chip FPGA en una placa de desarrollo.
- Diseñar una Placa de Circuito Impreso (PCB, por las siglas en inglés de *Printed Circuit Board*) que incorpore la FPGA y los componentes necesarios.
- Ensamblar y soldar la PCB.
- Comprobar el correcto funcionamiento del dispositivo.

5. Descripción del Sistema y Configuración Experimental

El sistema consta de una PCB con un chip FPGA. Las fases de diseño incluyen las pruebas iniciales con el *Kit de Evaluación Intel MAX 10 - 10M08*, el diseño del esquema del circuito, el diseño de la disposición de la PCB, y su soldadura. La FPGA 10M08SAE144C8G fue escogida por su capacidad para generar múltiples señales PWM y se programó utilizando el software *Intel Quartus Prime*. Una PCB personalizada fue creada, incorporando componentes para la alimentación, configuración, generación de PWM y entrada analógica. Dos diseños se han llevado a cabo: una iteración inicial, que se soldó y probó de manera experimental; y una nueva versión con mejoras, que se describe en el informe.

La FPGA funciona a 3,3V, mientras que la PCB se alimenta externamente a 20V, y un regulador de Baja Caída (LDO, por las siglas en inglés de *Low-Dropout*) reduce la tensión a

3,3V. El LDO puede proporcionar hasta 3,3W de potencia, siendo adecuado para la placa, que consume un máximo estimado de 2,2W. Tanto la FPGA como el LDO incluyen condensadores de desacoplamiento para filtrar el ruido y la interferencia electromagnética (EMI, por las siglas en inglés de *Electromagnetic Interference*). Un oscilador de 50MHz proporciona la fuente de reloj para el bloque PLL de la FPGA, utilizado para generar señales PWM; y un conector JTAG (en inglés, *Joint Test Action Group*) permite programar la FPGA desde un ordenador.

Para incrementar la intensidad de las señales y reducir el ruido, se utilizaron puertas de buffer individuales en cada salida de señal PWM. Estas señales se enrutan a través de conectores SMA (en inglés, *SubMiniature version A*), empleados para enviar las señales PWM desde la placa controladora a los inversores externos. Las señales analógicas también se reciben a través de conectores SMA. Unos amplificadores operacionales actúan como buffers para proteger y aislar la FPGA. Esta sección cuenta con provisiones para incorporar filtros paso alto o paso bajo en el futuro, según sea necesario.

La PCB cuenta con cuatro capas de señal y dimensiones de 4150 mil x 4950 mil. La mayoría de los componentes se encuentran en la capa superior, con algunos condensadores de desacoplamiento en la inferior. El diseño final se muestra en la Figura 1.

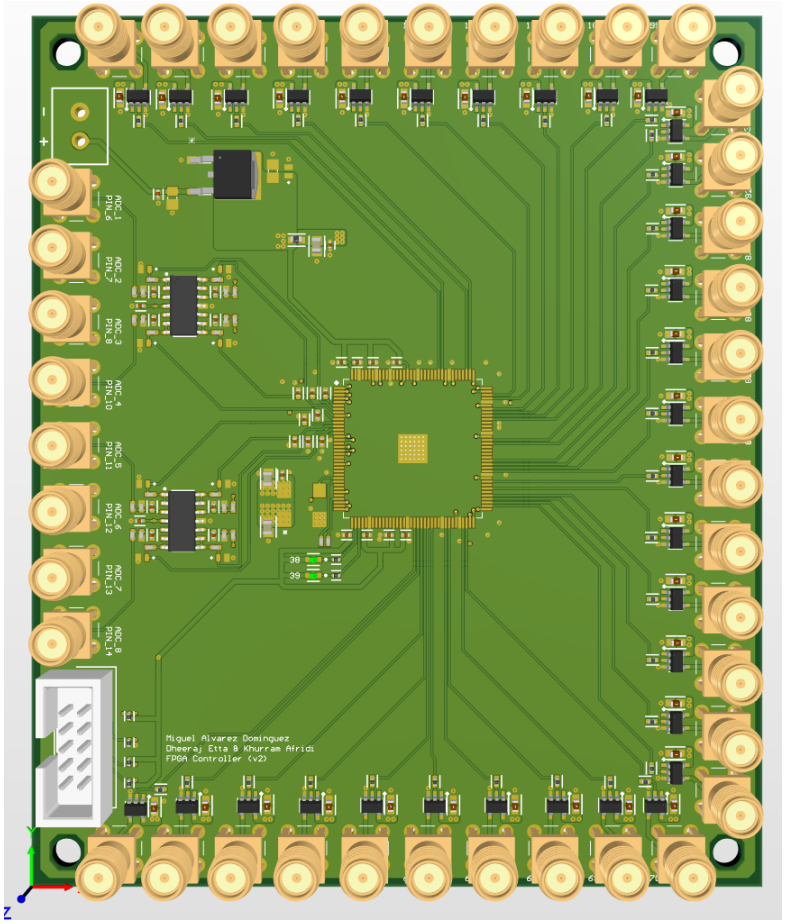

Figura 1. Vista 3D del Diseño Final de la PCB.

La versión inicial del diseño fue soldada y probada bajo diversas condiciones. Las principales diferencias entre los diseños son la ausencia de puertas de buffer, y una especificación diferente de

amplificador operacional. La placa fue soldada con todos los componentes necesarios, incluidos 10 conectores para la generación de PWM y 2 conectores para entradas analógicas.

La configuración de los experimentos es la siguiente. Primero, se evaluó la respuesta ante diferentes cargas de la FPGA, analizando la integridad de las señales PWM cuando se conectan distinto número de inversores. A continuación, el controlador se conectó a un dispositivo con 3 dobles inversores en paralelo, analizando la sincronización de las señales en las puertas de los Transistores de Efecto de Campo Metal-Óxido-Semiconductor (MOSFET, por las siglas en inglés de *Metal-Oxide-Semiconductor Field-Effect Transistor*) paralelos. Por último, el dispositivo se integró en un sistema real de WPT capacitivo dentro del entorno del laboratorio. Además, se verificó la capacidad de la placa para manejar entradas analógicas; aunque se descubrió que los amplificadores operacionales no eran adecuados, y una nueva especificación fue incluida en la versión final del diseño.

6. Resultados

Los resultados experimentales demuestran que la FPGA es capaz de generar señales PWM estables con éxito. Cada señal puede controlar hasta 2 inversores sin una degradación significativa de la misma. La adición de más inversores aumenta la carga y la constante de tiempo del circuito, lo que degrada la señal. La sincronización entre las señales PWM en las puertas de los MOSFET paralelos se mantuvo de manera efectiva (Figura 2), permitiendo controlar múltiples inversores en paralelo y garantizando un funcionamiento eficiente de los dispositivos. En la configuración real del sistema de WPT capacitivo, las pruebas iniciales lograron una transferencia de potencia de 4 kW con una eficiencia del 86 % [8]. En el futuro se realizarán pruebas adicionales para aumentar las capacidades de transferencia de potencia hasta 12 kW.

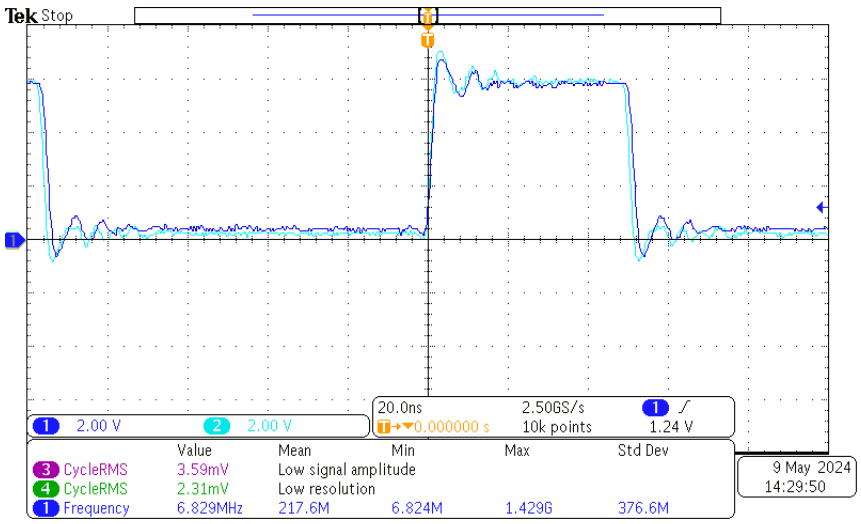

Figura 2. Señales PWM en las puertas de unos MOSFET paralelos.

7. Conclusión

Los experimentos realizados y los resultados obtenidos demuestran que el controlador FPGA ha sido desarrollado con éxito. No obstante, en el futuro se pueden realizar proyectos adicionales para mejorar el dispositivo. La última iteración del diseño, presentada en la memoria, soluciona los problemas encontrados con los amplificadores operacionales e introduce nuevas mejoras,

como las puertas de buffer. Asimismo, se sugiere el uso de conectores de Radio Frecuencia (RF) de múltiples puertos en futuras iteraciones, que permitirá reducir el número de conectores.

En conclusión, el desarrollo de este controlador FPGA representa un avance significativo para el grupo de laboratorio de Electrónica de Potencia de Cornell, especialmente en el caso de los sistemas WPT capacitivos. Este dispositivo desbloquea áreas previamente inaccesibles, apoya la investigación en curso y posiciona al grupo del laboratorio a la vanguardia de la investigación en WPT capacitivo.

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DEVELOPMENT OF AN FPGA CONTROLLER FOR HIGH-POWER MULTI-MHZ CAPACITIVE WIRELESS POWER TRANSFER SYSTEMS

Author: Álvarez Domínguez, Miguel.
Director: Afridi, Khurram Khan.
Co-director: Etta, Dheeraj
Collaborating Entity: Cornell University

ABSTRACT

The goal of this project is the development of a Field-Programmable Gate Array (FPGA)-based controller aimed at increasing power transfer capabilities in capacitive Wireless Power Transfer (WPT) systems for electric vehicles. The project focuses on generating multiple high-frequency Pulse-Width Modulation (PWM) signals to control up to 16 inverters. Experimental results demonstrate stable PWM signal integrity across multiple inverters. The integration of the controller into a capacitive WPT system achieved a power transfer of 4kW with 86% efficiency.

Keywords: FPGA-based controller, Wireless Power Transfer (WPT), Capacitive WPT systems, Pulse Width Modulation (PWM), Inverter control, High frequency signals.

1. Introduction

Wireless Power Transfer (WPT) can potentially increase the adoption of electric vehicles (EVs) by enabling stationary, semi-dynamic, and dynamic charging, thereby helping to overcome cost, charging time, and range limitations [1]. Traditional inductive WPT systems utilize magnetic fields and suffer from core losses, limiting their frequency and size reduction potential [2, 3]. Capacitive WPT systems, which use electric fields, can be smaller, lighter, and more efficient at higher frequencies [4]. However, the power transfer capability of current capacitive WPT systems is limited to a few kilowatts by the current ratings of commercially available transistors [5].

2. Problem Statement

Cornell University's Power Electronics Lab Group, led by Professor Khurram Afridi, has been working on capacitive WPT systems. In order to achieve high power transfer capabilities in capacitive WPT systems multiple inverters are needed. Each inverter contains four transistors, which need to be controlled by Pulse Width Modulation (PWM) signals. Currently, the only available method for the group to generate high-frequency PWM signals is through function generators. However, there is a limited number of these devices available in the Lab, restricting the number of inverters that can be used in their projects.

To increase the power transfer capabilities and include more inverters, a new method of PWM signal generation is necessary. Additionally, inconsistencies in semiconductor devices and

design layouts can result in imbalances in output currents when multiple inverter modules are paralleled, degrading overall efficiency. Various power combining networks have been proposed, such as immittance network-based power combiners and stacked inverter architectures [6, 7]. However, an effective solution to generate and manage the required PWM signals for a large number of inverters is still needed.

3. Proposed Solution

This project aims to develop an FPGA controller capable of generating 32 PWM signals for high-power multi-MHz capacitive WPT systems. This controller will enable the use of up to 16 inverters simultaneously, improving power transfer capabilities. Additionally, the controller will be able to receive up to 8 analog signals for future closed-loop control purposes. A Field-Programmable Gate Array (FPGA) is chosen over a microcontroller due to the high-frequency requirements of capacitive WPT systems.

4. Objectives

The objectives of the project are the following:

- Test the FPGA chip on an evaluation board.
- Design a Printed Circuit Board (PCB) incorporating the FPGA and necessary components.
- Assemble and solder the PCB.
- Test the device's operation.

5. Description of the System and Experimental Setup

The system consists of a PCB with an FPGA chip. The design phases include initial testing with the *Intel MAX 10 - 10M08 Evaluation Kit*, schematic design, PCB layout design, and soldering. The 10M08SAE144C8G FPGA was selected for its ability to generate multiple PWM signals and was configured using *Intel Quartus Prime Design Software*. A custom PCB was created, incorporating power, configuration, PWM generation, and analog input components. Two designs were made: an initial iteration, which was assembled and tested; and a new version with improvements, which is described in the report.

The FPGA works at 3.3V. The PCB is externally powered at 20V, and a Low-Dropout (LDO) regulator steps this down to 3.3V. The LDO can provide up to 3.3W of power. The board is estimated to consume a maximum of 2.2W, thus the chosen LDO is suitable for the device. Both the FPGA and the LDO include decoupling capacitors to filter noise and electromagnetic interference (EMI). A 50MHz oscillator provides the clock source for the FPGA's Phase-Locked Loop (PLL) core, utilized for generating PWM signals; and a JTAG (Joint Test Action Group) connector was included to program the FPGA from a computer.

To drive higher currents and reduce noise, single buffer gates were employed on each PWM signal output. These signals are routed though SMA (SubMiniature version A) connectors, which are used to send the PWM signals from the controller board to the external inverters. Analog signals are also received through SMA connectors. Operational amplifiers act as buffers to

protect and isolate the FPGA. This section has provisions to include high-pass or low-pass filters in the future, as needed.

The PCB features four signal layers and dimensions of 4150 mil x 4950 mil. Components were placed mostly on the top layer, with some decoupling capacitors on the bottom. The final design is shown in Figure 1.

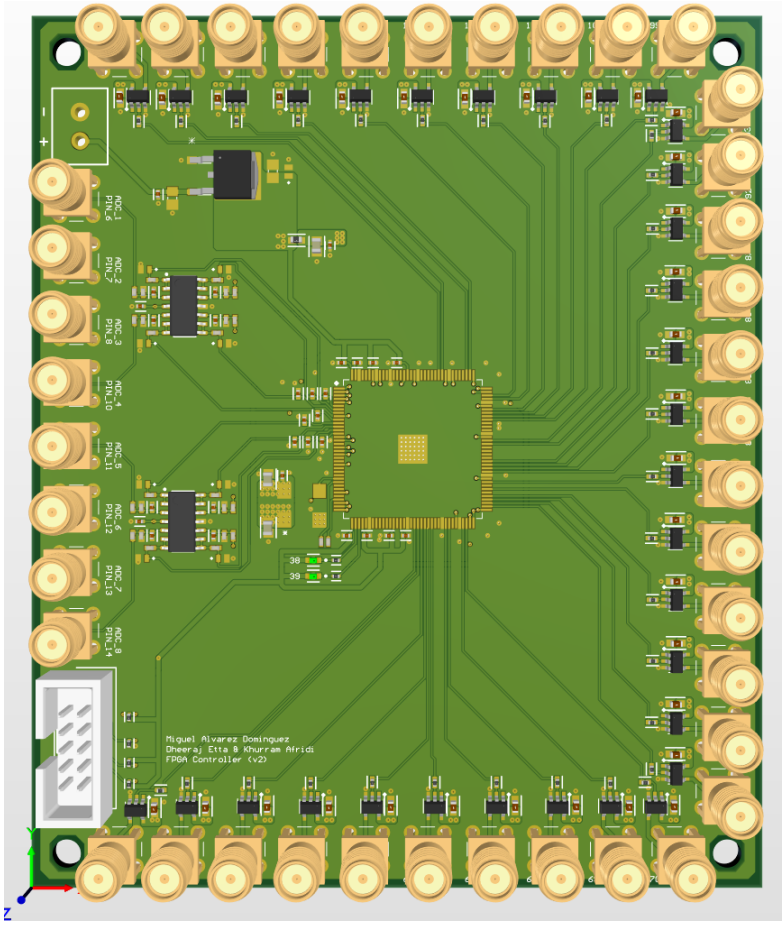

Figure 1. 3D View of the Final Layout of the PCB.

The initial version of the design was assembled and tested under various conditions. The main differences between designs were the absence of buffer gates, and a different operational amplifier specification. The board was soldered with all necessary components, including 10 connectors for PWM generation and 2 connectors for analog inputs.

The experimental setup proceeded as follows. First, the load capacity of the FPGA was evaluated, testing FPGA's ability to maintain PWM signal integrity when connected to multiple inverters. Next, the controller was connected to a 3 two-parallel inverter device, analyzing the synchronization of signals at parallel MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) gates. Last, the device was was integrated into a real capacitive WPT system within the Lab environment. Additionally, the board's ability to handle analog inputs was verified; although the op-amps were found not to be suitable, and a new specification was included in the final version of the design.

6. Results

The experimental results demonstrated that the FPGA successfully generated stable PWM signals. Each signal can control up to 2 connected inverters without significant degradation. Additional inverters increase the load and time constant of the circuit, degrading the signal. Synchronization among PWM signals in parallel MOSFET gates was effectively maintained (Figure 2); thus being suitable for controlling multiple parallel inverters and ensuring efficient operation of the devices. In the real capacitive WPT system setup, initial tests achieved a power transfer of 4 kW with an efficiency of 86% [8]. Further testing will be carried out to increase power transfer capabilities up to 12kW.

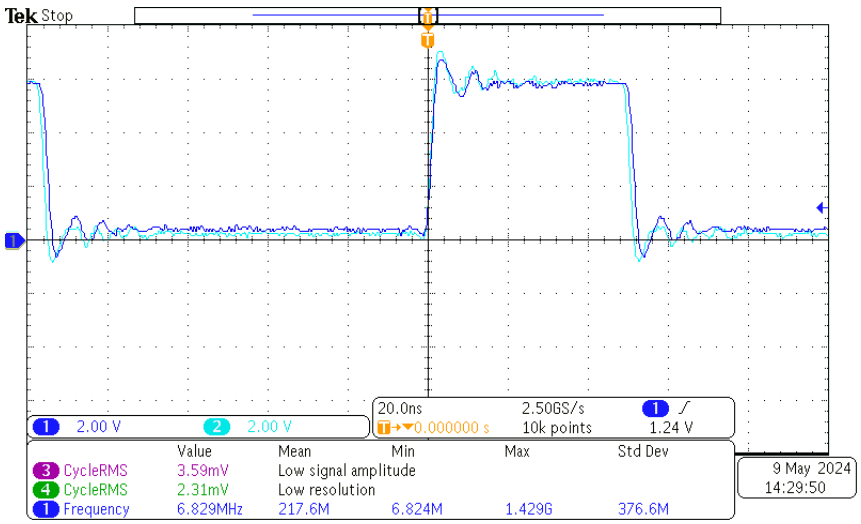

Figure 2. PWM Signals of one of the Parallel MOSFET Gates.

7. Conclusion

The experiments performed, and the subsequent results, demonstrate the successful development of the FPGA controller. Nevertheless, future work can be done in refining the device. The design presented in the report is the last iteration. It fixes some problems found with the operational amplifiers; and introduces new upgrades, such as the buffer gates. Furthermore, the use of multi-port Radio Frequency (RF) connectors is suggested for future iterations, thus reducing the number of connectors.

In conclusion, the development of this FPGA controller represents a significant advancement for Cornell's Power Electronics Lab Group, specially in the case of capacitive WPT systems. This device unlocks previously inaccessible areas, supporting ongoing research, and positioning the Lab group at the forefront of capacitive WPT research.

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A mi abuelo Tomás, que sé que está muy orgulloso de mí;
y a mi abuelo Rafa, por ser una enorme inspiración.

To my grandfather Tomás, whom I know is very proud of me;
and to my grandfather Rafa, for being an amazing inspiration.

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Acronyms

AC	Alternating Current
ADC	Analog-to-Digital Converter
DC	Direct Current
EMI	ElectroMagnetic Interference
EV	Electric Vehicle
FPGA	Field Programmable Gate Array
IC	Integrated Circuit
I/O	Input/Output
JTAG	Joint Test Action Group
LDO	Low-Dropout Regulator
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistors
PCB	Printed Circuit Board
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
RF	Radio Frequency
SMA	SubMiniature version A
WPT	Wireless Power Transfer
ZVS	Zero-Voltage-Switching

Chapter 1

Introduction

THE increasing demand for environmentally sustainable transportation has led to the widespread adoption of electric and plug-in hybrid vehicles. This shift presents significant challenges for car manufacturers and researchers worldwide, such as the high cost of battery energy storage, limited Electric Vehicle (EV) range, battery lifespan, and the expense of deploying fast charging infrastructure. EV charging systems can be classified into three types: wireless charging systems, conductive charging systems, and battery swapping [1]. The project presented here aims to enhance research on the first type: Wireless Power Transfer (WPT) systems.

1.1. Overview of Wireless Power Transfer Systems

Wireless Power Transfer can potentially increase the adoption of electric vehicles by enabling stationary, semi-dynamic and dynamic charging and help overcome their cost, charging time, and range limitations [2]. In EV applications, the conventional approach to wireless charging utilizes inductively coupled coils to transfer power with magnetic fields [3, 4]. The components used in inductive WPT systems are expensive, heavy and bulky ferrites, needed for magnetic flux guidance and shielding. Ferrites also present core losses, limiting the operating frequencies of these systems, and thus their potential for size reduction.

A second approach to EV charging are capacitive WPT systems, which transfer power through coupled plates, using electric fields. Electric fields are relatively directed by nature, so capacitive systems do not require ferrites. This characteristic enable those systems to be smaller, lighter, and easier to embed in the road. Additionally, they can be operated at higher frequencies without incurring in large losses. This outcome can potentially reduce components size and improve system efficiency [5].

However, the maximum power transfer of state-of-the-art capacitive WPT systems is limited by the current ratings of the commercially available transistors used in the inverters of these systems to just a few kilowatts [6]. A common approach to overcome these limitations and increase the power transfer capabilities is to parallel multiple inverter modules. Nevertheless, for high-frequency applications, paralleling inverters is difficult due to inconsistencies in the semiconductor devices and design layouts, resulting in imbalance in the output currents of the paralleled inverters and hence degrading the overall efficiency and power transfer capability.

To reduce current imbalance, various power combining networks have been proposed for these type of systems [7, 8]. Some of these networks encounter some issues when scaling the number of inverters. Even though the present immittance network-based approach is highly

scalable, it has a high component number, which may reduce reliability and increase the total cost of the system. Therefore, a different approach to power combining has also been presented, using stacked inverter architecture [9].

The topology of a large air-gap capacitive WPT system powered by combining multiple high-frequency inverters is shown in Figure 1 [7, 8, 9], which can be applied for both power combining approaches: parallel inverters and stacked inverters architecture. In this topology,

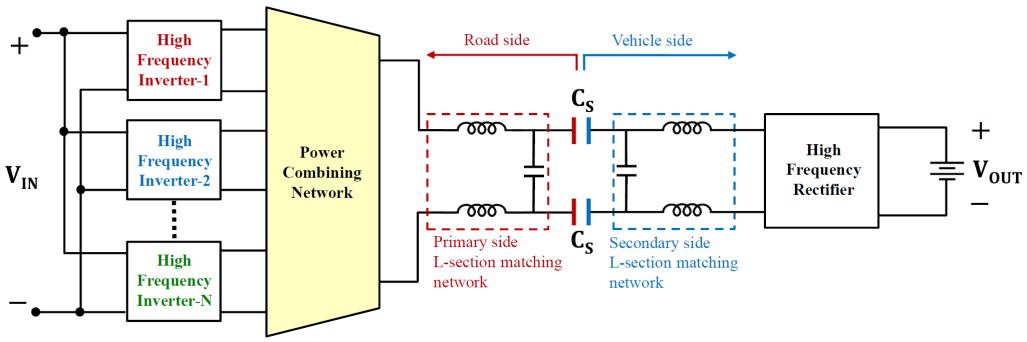


Figure 1. Capacitive WPT system topology with two (or) more inverters combined using a power combiner [7].

power is transferred wirelessly in this system through a large air-gap using a pair of charging pads: one pair pad is embedded in the roadway, and another pad pair is attached underneath the vehicle chassis. Each pad consists of two coupling plates that form capacitive coupling with their counterparts. The coupling capacitance between the roadway side and the vehicle side is very small, hence for effective power transfer, a high frequency of operation is required. The inverters on the ground side convert the DC input voltage to high-frequency AC voltage, and the output of all the inverters are combined using a power combining network. Two L-section matching networks on each side of the couplers step-up and step-down the voltage. Finally, a rectifier on the vehicle side converts the AC voltage to a DC voltage suitable for charging the EV.

Cornell University's Power Electronics Lab Group, led by Professor Khurram Afridi, has been working on capacitive WPT systems. Their research involves the topology presented in Figure 1. The current state of the research is presented in Section 1.2, while the motivation for the project is explained in Section 1.3.

1.2. Current State of Wireless Power Transfer Technology

To overcome maximum power transfer limitations in capacitive WPT systems, two approaches have been proposed, focusing on the use of multiple inverters. The first approach consists of the use of multiple inverters in parallel. This approach requires the use of an auxiliary Zero-Voltage-Switching (ZVS) tank-based circuit to achieve soft switching. Soft switching is required in high frequency applications to reduce switching losses. The auxiliary ZVS-tank based circuit consists on a properly sized inductor coil, which provides the required inductive current to achieve soft switching [10].

In order to reduce current imbalance when paralleling multiple inverters, various power combining networks have been proposed. In [7], four different networks were studied: in-phase

power combiner, out-phased power combiner, quadrature power combiner, and immittance network-based power combiner. Each of these networks were simulated. Immitance network-based power combiners resulted in high power transfer capabilities, with minimal mismatch between inverters. A design was proposed and experimentally validated in [8], with two parallel inverters. The results show that an output power of $4.2kW$ DC output was delivered, with almost equal power through each inverter. The topology of the power combiner is shown in Figure 2.

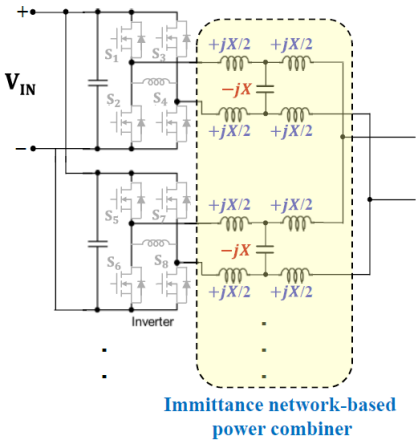


Figure 2. Immittance-network based power combiner for paralleling high-frequency inverters capacitive WPT systems [8].

A second approach to increasing the current carrying capabilities of the inverters has also been proposed. It consists of a highly scalable and compact power combining approach using stacked inverter architecture [9]. This design combines the output of multiple high-frequency inverters using a parallel-in series-out air-core transformer. The primary sides of the transformers provides common ground for each inverter, maintaining a simple gate-drive circuitry design; while the secondary ones are connected in series to combine the output voltages, and thus output power, of the inverters. These transformers can be designed so that the magnetizing inductance substitutes the ZVS inductor auxiliary circuit; and the leakage inductance can be absorbed into the design of the L-section matching networks of the circuit.

The proposed topology is shown in Figure 3. It can be seen that it requires fewer components than the immittance network-based solution, and is highly scalable. The experimental results show that a three stacked inverter-based capacitive WPT system is able to transfer $5.48kW$ of DC power, with an efficiency of 86.6%, and a power transfer density of $72.08kW/m^2$, thus validating the proposed design.

1.3. Motivation

The designs proposed in Section 1.2 show that in order to achieve high power transfer capabilities in capacitive WPT systems multiple inverters are needed. The voltage at the switch nodes of the inverters is typically around $300V - 400V$, while the input current can get to the order of tens of amps. Each inverter contains four transistors, which need to be controlled. One way of controlling these transistors is though Pulse Width Modulation (PWM) signals. PWM signals are square waves with a specific duty ratio and frequency.

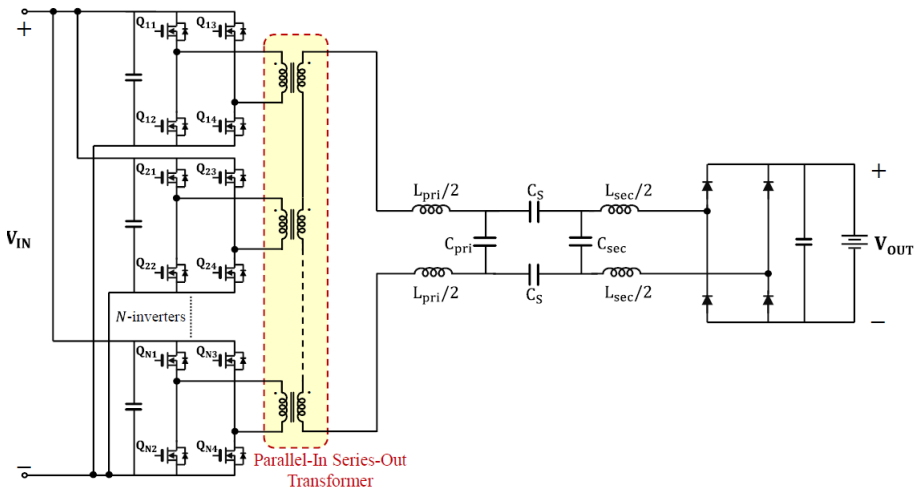


Figure 3. N-Stacked inverter-based capacitive WPT system [9].

Cornell's Power Electronics Lab Group is currently working on research into capacitive WPT systems. At the moment, the only available method for the group to generate high-frequency PWM signals is through function generators. However, there is a small number of these devices available in the Lab. As the group continues their research in capacitive WPT system, it has been proven that increasing the number of inverters can increase the power transfer capabilities of the system. In order to include more inverters in future projects, a new way of PWM signal generation is needed.

The project presented here is aimed at meeting this necessity. A Field Programmable Gate Arrays (FPGA) controller for high-power multi-MHz capacitive WPT systems was developed. FPGAs are integrated circuits that provide the ability to reconfigure the hardware [11]. The FPGA controller is able to provide more than 30 PWM signals. It will be used in the Power Electronics Lab in the future to power up to 16 inverters, with the goal of achieving greater power transfer capabilities. The use of an FPGA instead of a microcontroller is due to the high frequency nature of capacitive WPT systems, as they are operated at $6.78MHz$, in the case of Cornell's Lab.

The remaining of the report is organized as follows. Chapter 2 defines the project, its objectives and the methodology. Chapter 3 describes the main technologies employed for the development of the project. Chapter 4 provides a detailed description of the developed system, including the design of the board and the experimental setup. Chapter 5 provides an analysis on the results obtained during testing. Last, Chapter 6 concludes the report, with directions for future improvements.

Chapter 2

Project Definition

THIS chapter contains a description of the project presented here. The chapter is divided as follows: first, Section 2.1 lists the objectives of the project; next, Section 2.2 contains a report on the work methodology and work distribution; and last, Section 2.3 lists the resources used during the development of the system.

2.1. Objectives of the Project

The project presented here is aimed at developing a FPGA controller that can provide PWM signals and control multiple high-frequency inverters simultaneously. Specifically, the goals of this project are:

- Test the FPGA chip in an evaluation board and verify that it is suitable for the required application. A program will be developed to generate a few PWM signals, which will then be tested with an oscilloscope.
- Design a Printed Circuit Board (PCB) that includes the FPGA chip, with the appropriate connectors and components, that ensure the generation of the desired PWM signals. The PCB design will involve creating the proper schematic for the board, as well as creating a functioning layout, with the necessary electrical connections. The board should be able to generate, at least, 30 PWM signals and receive as an input up to 8 analog signals for closed-loop control purposes in the future.
- Manufacture, populate and solder all the necessary components to the PCB. First, only a few components will be soldered: those needed to generate some PWM signals. After the correct operation is ensured, all components will be soldered.
- Test the correct operation of the device: its ability to program the FPGA, generate PWM signals, and receive analog signals. If some modifications are needed, a second design will be made and tested.
- Test the implementation of the board with real inverters, that will be used in the Lab for the capacitive WPT system.
- During the development of the project, learn and understand how to use the software to program FPGAs, the software to design PCBs, and how to solder and build power electronics components.

2.2. Work Methodology

The work methodology is highly related to the objectives of this project. It can be divided into three different sections: an initial testing and contact with the FPGA chip; the development of the board according to the needs of the project; and a final testing. The schedule for the project is the following:

November and December: An evaluation board with the FPGA was tested. To do this, a small program was written to test the PWM generation capabilities of the chip, and become familiar with it. Additionally, the evaluation board was inspected to determine the necessary components for its correct operation.

January, February and March: After making sure that the FPGA chip suits the project, a custom PCB was made. This board includes the FPGA, connectors to deliver up to 32 PWM signals, connectors for up to 8 analog input signals, a JTAG (Joint Test Action Group) connector to program the board, and other components that ensure the board works, such as power connectors and capacitors, among others. During this phase of the project, all the necessary components were selected; and the PCB was designed. At the same time, the fundamentals of PCB design were learnt, as well as how the necessary software works. The PCB design consists of two parts: first, the schematic, where all the electrical connections are defined; and then, the layout, where all the components are laid out, with proper placement and separation between each other. A schematic was completed before the layout could be defined. In the latter, all the electrical traces and planes are defined, and a 3D view of the board is generated. After the design is finished, it was sent for manufacturing, and all the components were ordered.

March and April: Once the PCB was manufactured, the main components were soldered, along with a few connectors. The board was tested the same way as with the evaluation board. The correct behaviour of all components was also checked.

April and May: With all the necessary components soldered, the board was tested again to prove the generation of PWM signals. It was used with real inverters in the Lab, and tested in different configurations, such as in a real capacitive WPT system. The necessary components needed to assemble the system, such as rectifiers or transformers, were also build during this time. Although analog inputs were not used at this time, they were tested for future instances. After the initial design, an improved version was made with all the necessary corrections.

Additionally, the daily work methodology looked as follows: A daily one hour group meeting was held every Monday between the Professor and all the members of the Lab group. Every student would explain their advancements in their projects of the past week; and some presentations were given on different Power Electronics topics occasionally. Aside from group meetings, one-to-one meetings with the project director or co-director were held as needed as the project evolved, and to ensure all the correct decisions were being taken. The design phase involved working on the computer both in the Lab and from home. However, the testing and soldering phase involved working in the Lab with the hardware.

2.3. Resources Employed

The FPGA Controller project is part of the capacitive WPT system project in Cornell's Power Electronics Lab. Therefore, much of the project took place inside the Power Electronics Lab, which includes the following resources: high frequency oscilloscopes, for testing the signals from the board; a soldering station (with solder paste, solder wire, soldering guns, and soldering pencils), to properly solder all the components to the PCB; a microscope, useful when soldering the individual pins of the FPGA controllers, and multimeters to measure voltages, resistances, and check short-circuits during soldering phase.

Additionally, the project required the use of the *Intel Quartus Prime Design Software* to program the FPGA; and the *Altium Designer* software, used to design PCBs. Last, the FPGA documentation, data-sheet, and design guidelines were useful when designing the PCB.

Other necessary resources include the inverters used in the capacitive WPT system project, which required some adaptations and modifications as the project evolved; as well as the project test bench, used to simulate an EV with capacitive wireless charging capabilities.

Chapter 3

Description of Technologies

THIS chapter describes the different technologies available, as well as those used through the development of the project. All other resources used, that are not included here, were listed in Section 2.3 of the report.

Inverter and Rectifier

An inverter is a power electronic device that transforms direct current (DC) to alternating current (AC). The inverters used in the Lab are built with four power MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors, a type of transistor typically used in power electronics applications), which turn ON or OFF depending on the PWM signals given. Two PWM signals are needed to control one inverter. The schematic for the inverters can be seen in the red boxes of Figure 4. Opposite to inverters, rectifiers transform AC into DC. Full bridge rectifiers are built with four diodes, as shown in the green box of Figure 4.

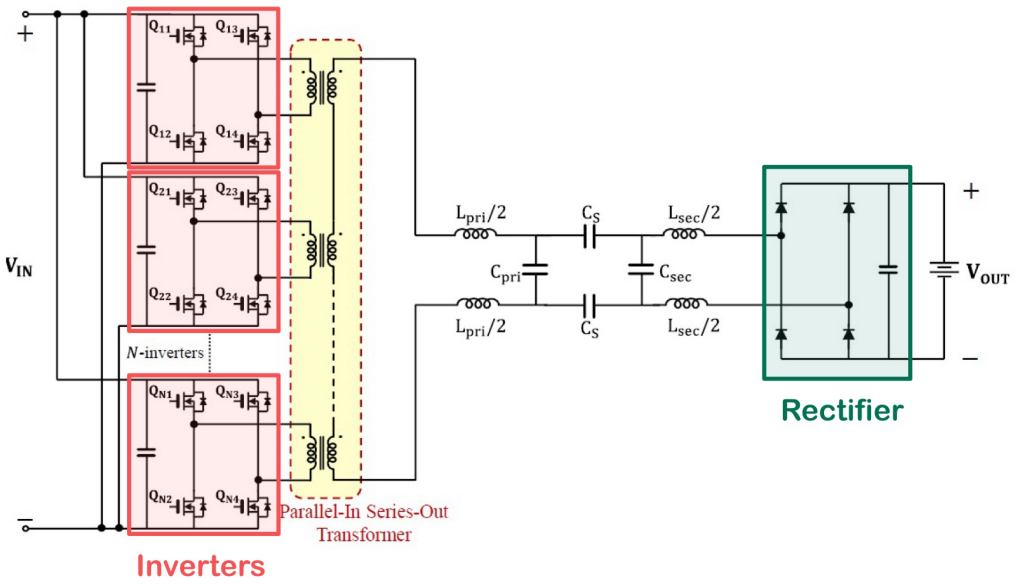


Figure 4. Inverters and Rectifier of the circuit in Figure 3.

Pulse Width Modulation

Pulse Width Modulation (PWM) is a method of controlling the average power or the amplitude of delivered by a signal. PWM are typically square signals. The width of the

pulse is defined by the duty ratio, while the period is set by the frequency of the signal. Figure 5 shows PWM signals of different duty cycles, but same frequency. For example, a PWM of 60% duty cycle will stay HIGH for 60% of the period, and LOW for the remaining 40%. Modifying the duty cycle of a PWM signal is an effective method of controlling when the power MOSFETs of the inverter turn ON or OFF. Additionally, the frequency of these signals also defines the frequency of the AC signal obtained from the inverter.

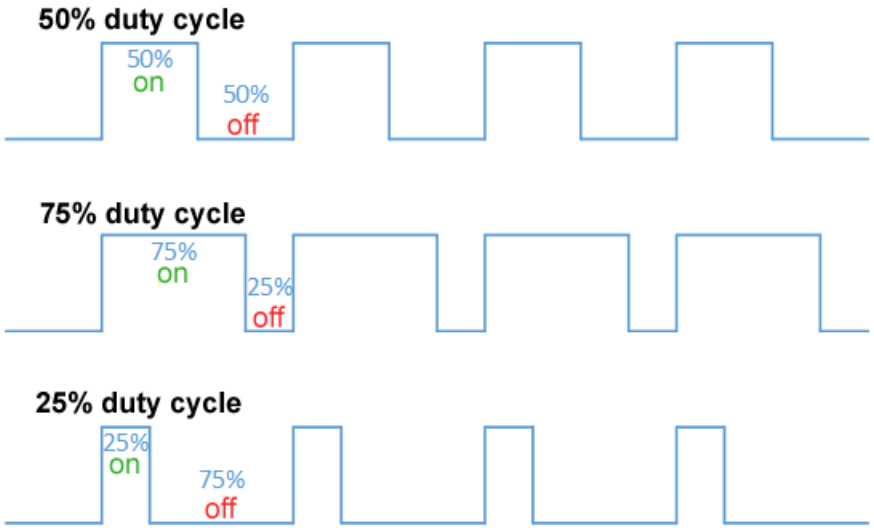


Figure 5. PWM Signals of different Duty Cycles [12].

Waveform Generator

A Waveform Generator is a device that is able to produce signals with different shapes. The waveform generators available in the Lab are the *Agilent 33500B Series* (now available as the *Keysight Technologies 33500B Waveform Generator*. Price: $\$2500 - \$4600$ [13]). Each generator is capable of producing up to two different signals. The main parameters that can be configured in the generator are frequency, amplitude, offset, phase and duty cycle, as shown in Figure 6. The generators available in the Lab have two output channels. Each inverter needs two PWM signal in order to work; therefore, each generator can only control a single inverter. The limited number of generators available in the Lab, and the high price of each device makes the use of waveform generators a non-viable option of controlling multiple inverters at the same time.

Printed Circuit Board

In electronics, a Printed Circuit Board (PCB) is an assembly that uses copper to electrically connect different components, while also providing mechanical support for those components. PCBs are built from alternating layers of conductive copper and layers of electrical insulators [14]. As PCBs are printed, they can be used to replicate a circuit multiple times, reducing the time to build them, compared to hand-wired circuits. Additionally, it is easier to control the impedances of the circuit, as well as the placement of the wires, avoiding loops that will create Electromagnetic Interferences (EMI) at high frequencies. The large number of components in the controller, as well as its high frequency nature, requires the FPGA controller to be designed in a PCB.

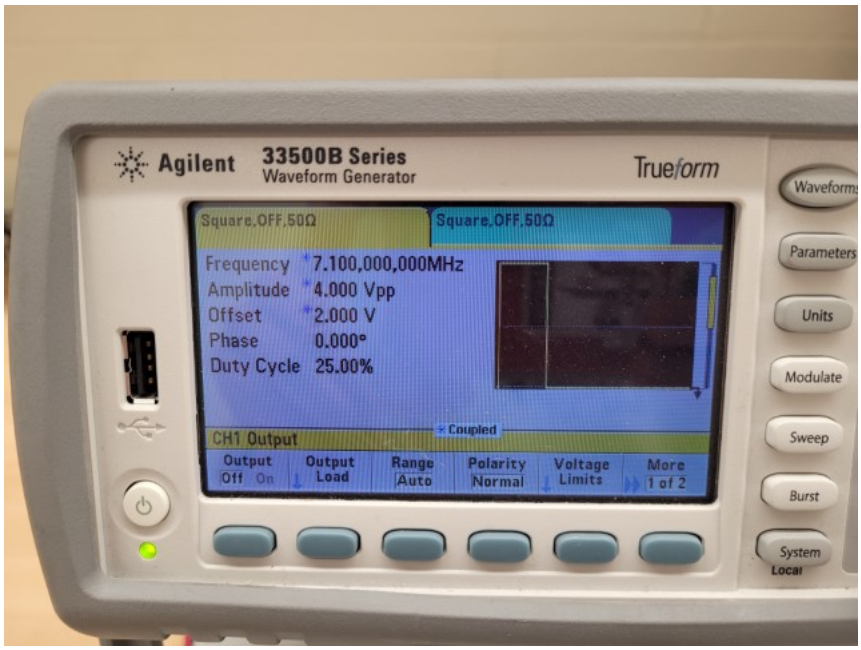


Figure 6. Parameter Configuration screen of the Agilent 33500B Series waveform generator.

Field Programmable Gate Array

Field Programmable Gate Arrays (FPGAs) are integrated circuit that provide the ability to reconfigure the hardware after being manufactured. FPGAs are made of configurable logic blocks and some programmable interconnects, allowing for the connection of multiple blocks. An FPGA can handle the creation of simple logic gates, as well as the design of entire system on a chip (SoC) [11]. In this project, an FPGA will be used to generate the different PWM signals needed to control the inverter. The FPGA model used for the project is the *Intel Altera MAX 10* 10M08SAE144C8G FPGA. This chip contains 144 pins, 1 Analog-to-Digital Converter (ADC) module, 1 Phase Locked Loop (PLL) module, and works at $3.3V$.

Altium Designer

Altium Designer is a professional PCB and electronics design software developed by *Altium Limited*. It has a schematic editor, and a PCB editor, among others. The schematic editor includes features such as schematic symbols, port and net name and automatic component numbering, that facilitate the design. The schematic can be later ported to the PCB editor, where all components are placed and routed according to the schematic. The PCB editor has a 2D view of all the layers, as well as a 3D view of the design. *Altium Designer* supports the use of libraries that contain the symbol and footprint of components [15]. *Altium Designer* is the software used for the PCB design in this project.

Quartus Prime

Quartus Prime Design Software is a design environment developed by *Intel* that enables FPGA programming [16]. The FPGA can be programmed using Verilog or VHDL code, although, for this project, only VHDL was used. The features of *Quartus Prime* include a coding environment with a compiler, a Pin Planner used to select each signal to a specific FPGA pin, and a Programmer used to program the FPGA according to the project. The software includes

some modules such as PLL or ADC, that can be used in the design. As the FPGA used in the project is from *Intel Altera*, *Quartus Prime* is used to program the chip.

Intel MAX 10 - 10M08 Evaluation Kit

The *Intel MAX 10 - 10M08 Evaluation Kit* is a board used for the evaluation of the *Intel MAX 10* FPGA. The board numbered EK-10M08E144 contains the 10M08SAE144C8G chip (used in the project) [17]. This board was used to test the behavior of the FPGA before the design of the controller. The kit contains the necessary connectors to power, program, and probe the board. It also contains other necessary components, such as capacitors, resistors, or the oscillator, as shown in Figure 7.

Figure 7. Intel MAX 10 - 10M08 Evaluation Kit [17].

Chapter 4

Description of the Developed System

THIS chapter contains a detailed explanation the developed system, including the justification of each decision made. The chapter is divided in two: Section 4.1 will explain the FPGA controller design process, and Section 4.2 will describe all the experiment setups used to test the controller.

4.1. Board Design

The design of the board can be divided into several phases: An initial testing and hands-on with the *Intel MAX 10 - 10M08 Evaluation Kit*; the circuit schematic design with the selection of all components; and the PCB layout design, where all components were placed and routed accordingly. Last, a soldering phase, where all components were assembled and soldered to the board. The design explained in this Chapter is the final version. However, an initial iteration of the design was also made, and is the version that was soldered and tested. The differences between both designs are listed in Section 4.1.4.

4.1.1. Evaluation Board Testing

The *Intel MAX 10 - 10M08 Evaluation Kit*, contains the *Intel Altera MAX 10* 10M08SAE144C8G FPGA chip with all the necessary components and connections for proper operation. The selection of the FPGA chip had already been made by the Lab, due to its abilities to generate multiple PWM signals, and the inclusion of modules such as the PLL module or the ADC module. This kit was utilized to ensure that the chosen FPGA is suitable for the control purposes of the capacitive WPT project.s

A Phase-Locked Loop (PLL) is a circuit that maintains the same phase and frequency between the input and output of the system. If a frequency divider is incorporated, it is possible to generate different clock signals based on an input signal. The *Altera PLL IP Core*, inside the *Quartus Prime* software, is utilized to program the PLL module in the FPGA. The *PLL IP Core* provides the ability to receive a clock signal as an input, and generate up to 5 different signals with a specific frequency, duty cycle, and phase between them. This core is used to generate the necessary PWM signals to control the inverters.

In order to use the PLL core, it should be selected from the *IP Catalog*, inside the *Tools* tab. The PLL core is found under *Library - Basic Functions - Clocks; PLLs and Resets - PLL - ALTPLL*. It should be included as a component in the FPGA architecture code, as shown in Code 1.

```
component my_pll is
  port (
    areset : IN std_logic := '0';
    inclk0 : IN std_logic := '0';
    c0     : OUT std_logic;
    c1     : OUT std_logic;
    c2     : OUT std_logic;
      -- Add as many clocks as used...
    locked : OUT std_logic
  );
end component my_pll;
```

Code 1. Inclusion of the PLL Component

The *PLL IP Core* has several options and settings. The two main windows are *General*, inside *Parameter Settings*; and *Output Clocks*. *General* is used to select the frequency of the input clock. In the case of the *Evaluation Kit*, the oscillator has a $50MHz$ frequency; so that frequency was selected, as seen in Figure 8. The *Output Clocks* setting is used to select the frequency, phase and duty cycle of the output signal. It is also employed to select whether the signal will be used or not. As the capacitive WPT System works at $6.78MHz$, that was the output frequency selected, as seen in Figure 9.

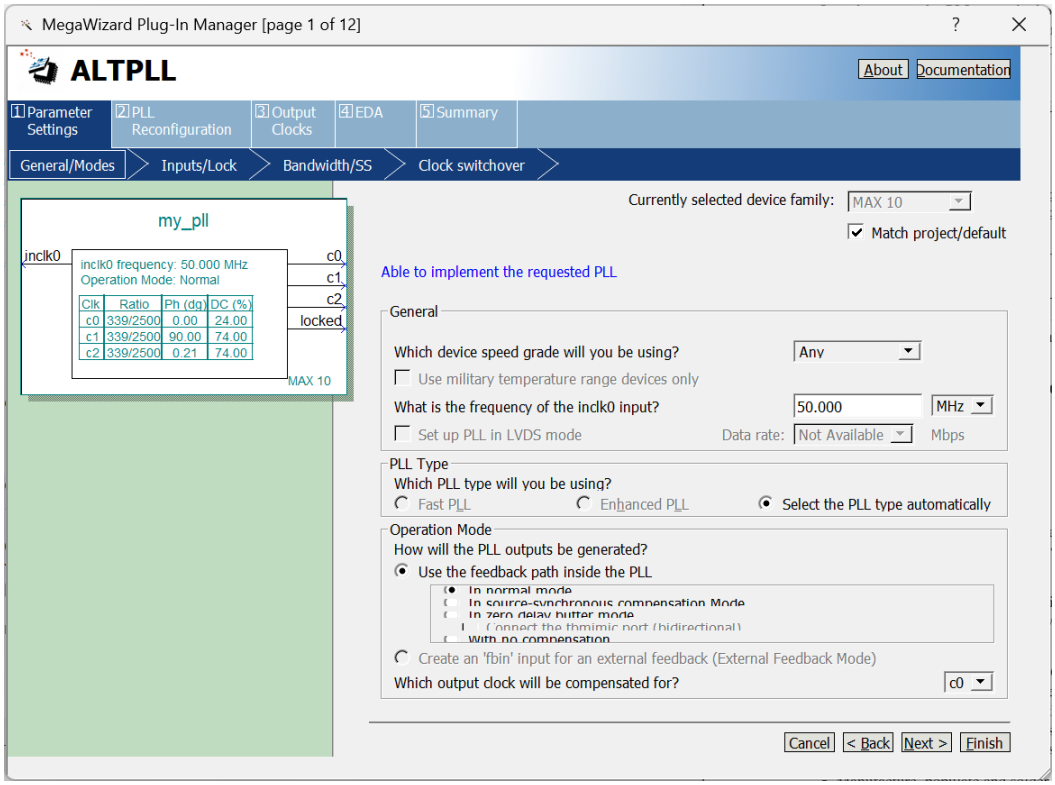


Figure 8. *General* - Input Clock Frequency Configuration.

The FPGA kit was then configured, following the device's User Guide [18] to give three PWM signals at $6.78MHz$: one with a 24% duty cycle and $0°$ phase; and two with 74% duty

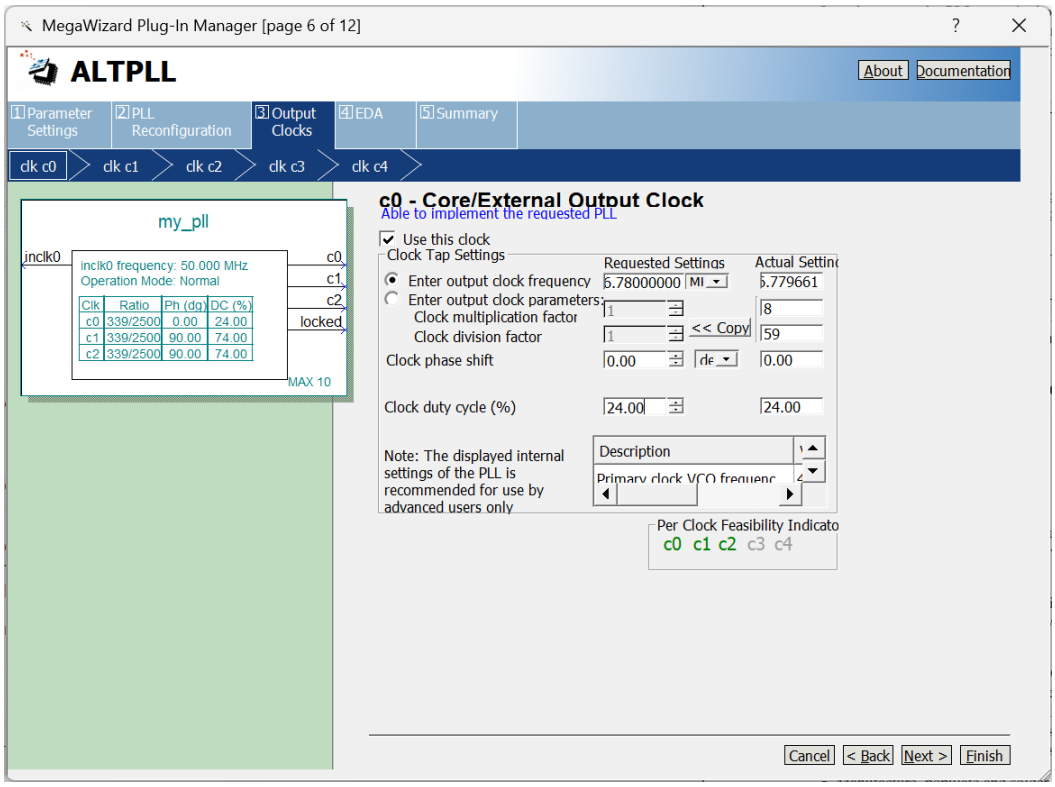


Figure 9. *Output Clock* Configuration.

cycle and $90°$ phase. The output signals were probed with an oscilloscope. The first two signals were measured with a vertical scale of $1V/div$; while the last one had a scale of $2V/div$ (thus it should appear as half the other two signals). The results are displayed in Figure 10.

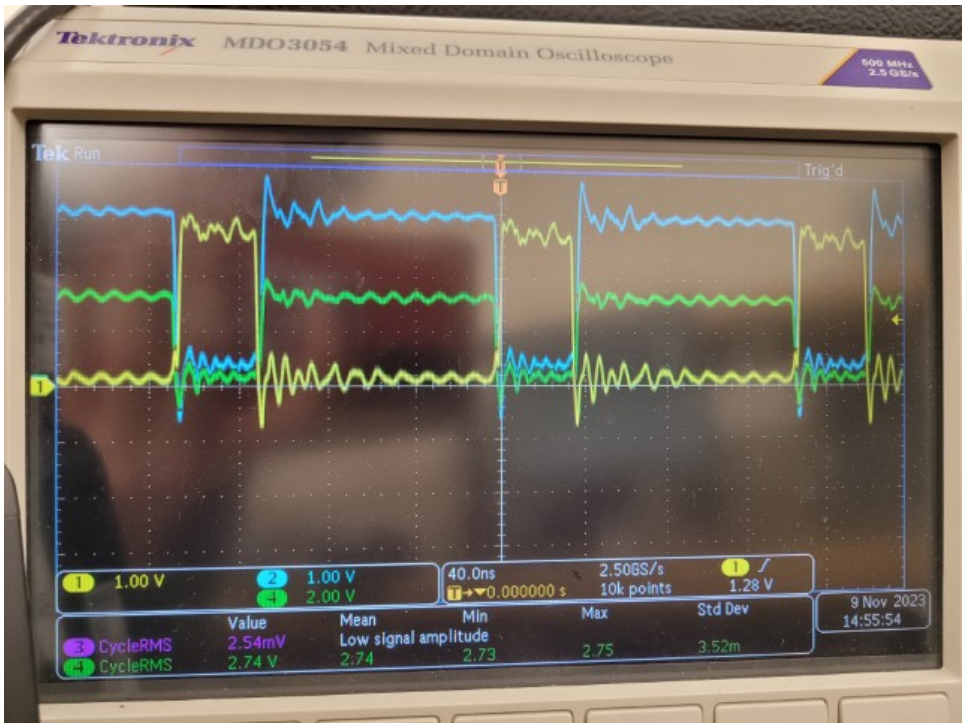


Figure 10. $6.78MHz$ PWM signals from the FPGA Evaluation Kit.

The oscilloscope screen shows the three PWM signals with the characteristics specified above. Therefore, it was experimentally confirmed that the chosen FPGA is able to generate multiple custom PWM signals. The next subsections detail the design process of the controller board. The main component of the board is the 10M08SAE144C8G FPGA chip, which has been proven to be suitable for the inverter control requirements of the capacitive WPT system.

4.1.2. Schematic Design and Component Selection

With the FPGA chip already selected and tested, a custom PCB was made for the controller. The board was developed according to the evaluation kit documentation (found in Table 3 of [17]), which includes schematic and PCB files; and the *Intel MAX 10 Device Handbook* [19], which contains the FPGA Datasheet, as well as the Design Guidelines. The final schematic of the PCB is included in Appendix C.

The components of the controller PCB can be divided into four different categories: power, configuration, PWM generation, and analog input. The central component of the board is the FPGA chip, thus it is included in the four categories.

4.1.2.1. Power Subsystem

The FPGA works at $3.3V$, and needs to receive power through multiple pins. However, the controller board will be working alongside other inverters, whose gate driving sections are externally powered at $20V$. Therefore, the controller board will also be able to be powered with up to $20V$. In order to step down the voltage, a linear voltage regulator is used. Specifically, a low-dropout regulator (LDO) is utilized due to its small size. The LMS8117ADTX-3.3/NOPB [20] LDO was chosen, which maintains a constant $3.3V$ output voltage, and can receive an input voltage of $20V$. Additionally, it has an output current of $1A$, providing $3.3W$ of power to the board, which is sufficient to power all components, as explained below.

The active components of the board that will be drawing all of the power are:

- Two OPA4354AIDR [21], quad Operational Amplifiers, used in the analog section. They have a maximum quiescent current of $6mA$ per amplifier . These amplifiers are used as buffers, thus with negligible output current. Therefore, the total power consumption of all the amplifiers is $2 \times 4 \times (6mA) \times (3.3V) = 158.4mW$.
- One CB3LV-3C-50M0000 [22], $50MHz$ oscillator. It is used as a clock source for the FPGA, and draws $20mA$, consuming $66mW$.
- 32 SN74LVC1G34DBVR [23], single buffer gates, used in the PWM generation section. The quiescent current is negligible (in the order of micro-amps), and can deliver up to $16mA$ of output current. The total power consumption is $32 \times (16mA) \times (3.3V) = 1689.6mW$.
- One 10M08SAE144C8G [19] FPGA. Its power consumption depends on how the chip is programmed and used. In order to estimate the power consumption, *Intel* provides an *Early Power Estimator* calculator [24]. After configuring the calculator with the number of Input/Output (I/O) pins, the use of the PLL block, and the clock frequency, a total power consumption of $220mW$ was obtained, as seen in Figure 11.

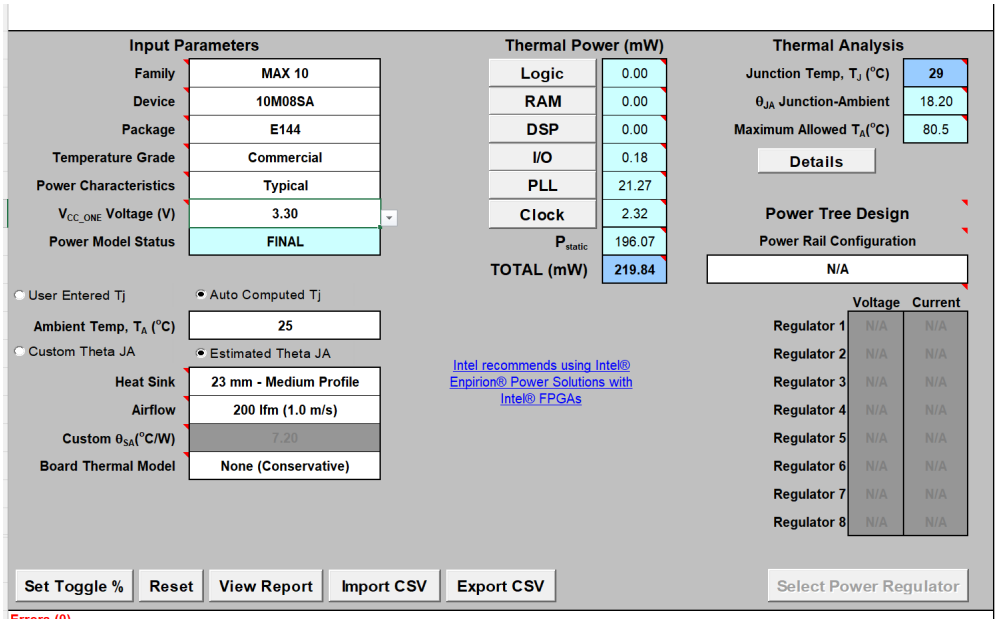


Figure 11. Screenshot of *Early Power Estimator* results.

Taking into account all these components, the total maximum power consumption is $2134mW$. The LDO is capable of providing that amount of power, with a safety factor of 1.55. Therefore, the board can be externally powered with up to $20V$ (VCC). The LDO steps that voltage down to $3.3V$ (VCC_ONE). In order to filter possible external noise, $10\mu F$ and $0.1\mu F$ decoupling capacitor were included at the input and output of the regulator, as specified by the device datasheet [20]. Additionally, a $3.3V$ zener diode was placed at the output in order to limit the output voltage and protect the FPGA. The LDO connection is shown in Figure 12.

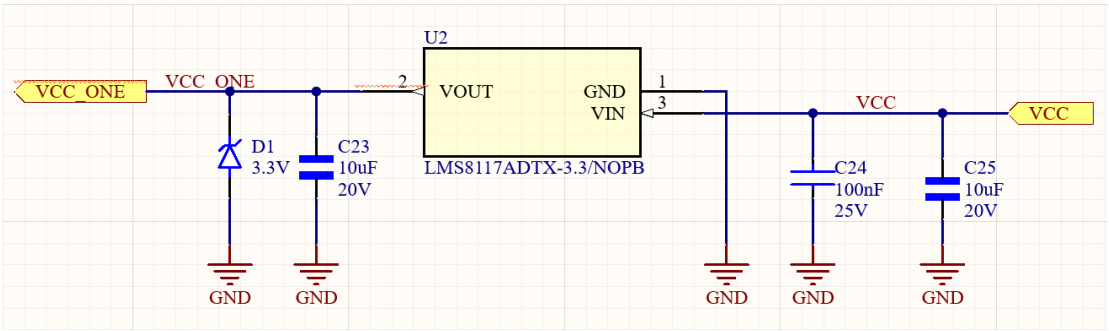


Figure 12. Detail of the LDO Schematic.

The FPGA has 10 power pins, which receive VCC_ONE. Next to each pin, a $0.1\mu F$ decoupling capacitor was added to filter any noise. Each of the FPGA's I/O banks needs to be powered as well at $3.3V$ (VCCIO). Two $10\mu F$ decoupling capacitors were added between VCC_ONE and VCCIO, as well as one $0.1\mu F$ decoupling capacitor next to every I/O bank power input pin. Last, the analog section is also powered at $3.3V$ with VCCA. A ferrite bead, and $10\mu F$ and $1\mu F$ decoupling capacitors were added between VCC_ONE and VCCA to filter noise and EMI. Again, every analog power input pin contains a $0.1\mu F$ decoupling capacitor next to it, for the same purposes.

4.1.2.2. Configuration Subsystem

The FPGA chip needs a series of components in order to work properly. Specifically, a clock source is needed to generate PWM signals, and a JTAG connector is required to program the chip.

As explained in Section 4.4.1, a PLL is utilized to generate PWM signals. An external clock source is needed to drive the PLL. The clock frequency should be higher than that of the PWM signals, so that a frequency divider can be used to provide the desired frequency. The CB3LV-3C-50M0000 [22] oscillator was chosen as the clock source. It works at $3.3V$ and provides a clock signal of $50MHz$. It is also the same clock used in the *Evaluation Kit*, which was proven to work properly. The oscillator is powered with VCC_ONE and a $0.1\mu F$ decoupling capacitor; and the enable signal is tied to power, as there is no need to disable the oscillator for the purposes of the controller. The connection of the oscillator is shown in Figure 13.

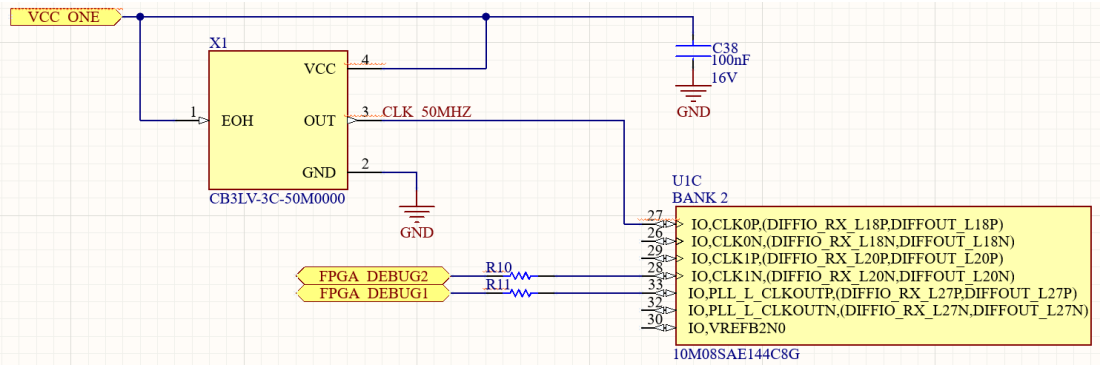


Figure 13. Detail of the Oscillator Schematic.

In order to program the FPGA, a Joint Test Action Group (JTAG) connector is needed. It contains a series of pins that carry the necessary information for the computer to communicate with the FPGA. The connector of choice is the 70246-1004 [25]. This is the same connector as the one used in the Evaluation Board, which is known to work well with the FPGA. According to the FPGA design guidelines [19], the signals TMS, TDI and JTAGEN need a $10k\Omega$ pull-up resistor connected to VCCIO; while the signal TCK needs a $1k\Omega$ pull-down resistor, as shown in Figure 14.

Last, two green LEDs were connected to two I/O pins through $1k\Omega$ resistors as custom output elements, and are used to test that the board is powered correctly.

4.1.2.3. PWM Generation Subsystem

The main task of the FPGA is PWM signal generation. The chip can be programmed to provide PWM signals through specific pins. In order to use those signals, proper connectors are needed. The board will be connected to the inverters through SubMiniature version A (SMA) connectors. These are a type of Radio Frequency (RF) connectors and are suitable for high frequency purposes.

Instead of sending the PWM from the FPGA to through the connector, a single buffer gate was added to every signal to drive higher currents and reduce noise. The buffers used is the same as those used in the inverters in the Lab, the SN74LVC1G34DBVR [23], with a maximum

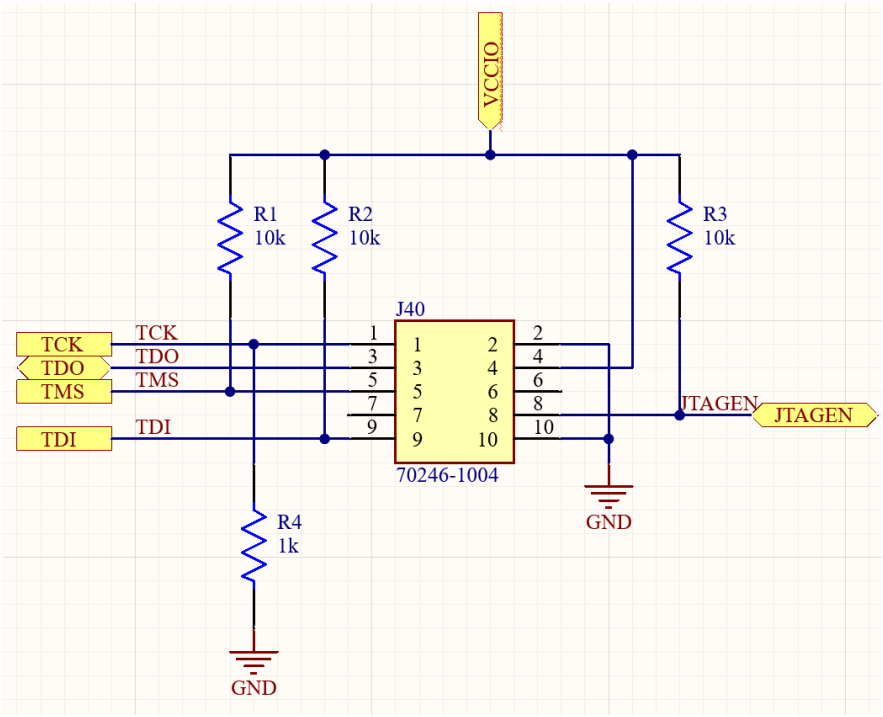


Figure 14. Detail of the JTAG Connector Schematic.

supply voltage of $5.5V$ and output current of $16mA$. When the input signal (in this case, the PWM signal) is LOW, the output voltage of the buffer will be $0V$; while when the input signal is HIGH, the output voltage will be the same as the supply voltage. As the buffers are powered with VCC_ONE, the output voltage when HIGH will be $3.3V$. In the case of this buffer, a signal is LOW when the voltage is lower than $0.8V$; and it is HIGH when the voltage is higher than $2V$. As the PWM signals are either $0V$ or $3.3V$, these buffers are suitable for the board. A $10\mu F$ decoupling capacitor was added next to each power for noise filtering purposes, as shown in Figure 15. Note that these buffer gates were added in the second version of the designed, thus the soldered board does not contain them.

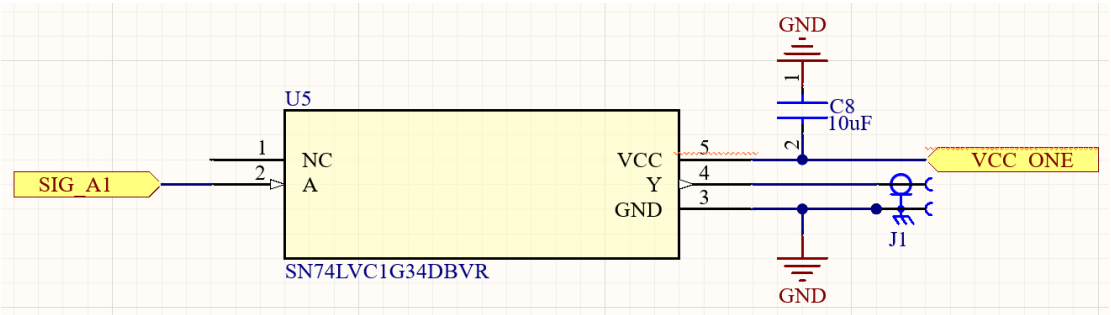


Figure 15. Detail of a Single Buffer Gate and SMA Connector Schematic.

Additionally, a 0Ω resistor was added between the FPGA PWM output signal and the buffer gate; as a means of connecting or disconnecting the output signal when desired. The resistor can be replaced by soldering the two pads, obtaining the same function.

4.1.2.4. Analog Subsystem

The ADC block of the FPGA needs an analog voltage and ground reference reference. The analog reference is connected to VCCA with a $1\mu F$ decoupling capacitor and a 0Ω resistor, to manually connect or disconnect the reference signal. The analog ground is tied to the board ground through a ferrite bead to filter noise and EMI.

The analog signals are received from SMA connectors. The OPA4354AIDR [21] operational amplifier acts as a buffer between the signal and the FPGA to protect and isolate the chip. This buffer is a rail-to-rail operational amplifier, meaning the output voltage can get as high as the supply voltage. Additionally, it has a $250MHz$ unity gain bandwidth, thus making it suitable for the Lab's applications, as the capacitive WPT system works at $6.78MHz$. A previous iteration of the board design included a different non-rail-to-rail operational amplifier, the LM2902DR2 [26]. As a result, the analog signal was clamped at a lower voltage than the supply voltage.

Each OPA4354AIDR Integrated Circuit (IC) [21] contains four operational amplifiers. Each IC is powered from VCAA with a $0.1\mu F$ decoupling capacitor. Additionally, provision for low-pass or high-pass filters was added at the input and output of each buffer. The capacitors and resistors can be switched and modified, as they all have the same dimensions. Last, $3.3V$ zener diodes were added between the buffer and the FPGA to prevent high voltages from damaging the FPGA. With the specified configuration, the analog input signals can vary from $0V$ to $3.3V$. Figure 16 shows the connection of a buffer with the SMA connector and the input filter.

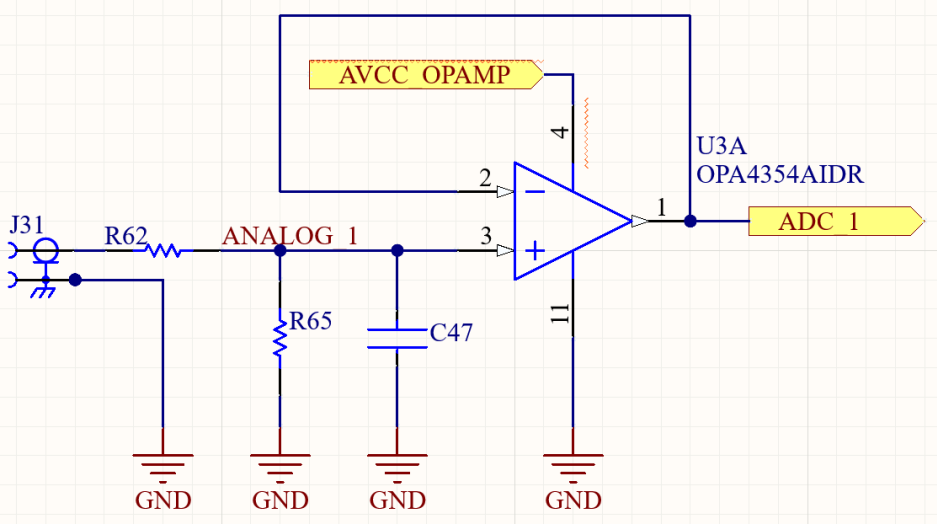


Figure 16. Detail of a Single Buffer, Input Filter, and SMA Connector.

All other resistors and capacitors utilized in the board, that were not mentioned in the sections above, were added following the FPGA Design Guidelines [19], to ensure the correct behavior of the FPGA. The voltage rating of these components was selected according to the FPGA voltage ratings: as the board works at $3.3V$, most components are rated at $10V$ or $16V$. However, those close to the LDO are rated at higher voltages: $20V$ and $25V$. The size of most resistors and capacitors is 0402. Nevertheless, some capacitors of $1\mu F$ or larger are 0603 or 0805 size. Additionally, all pin connections to the FPGA were made according to those guidelines. Table 1 contains a list of all the components employed in the PCB. The cost of all components when bought from Mouser [27] is approximately $\$110$.

Part Number	Description	Quantity
C1005X5R1C104K050BA	CAP 100nF 16V 0402	32
MLAST105SB5104KFNA01	CAP 100nF 25V 0402	1
CL10X106MP8NRNC	CAP 10uF 10V 0603	32
GRM21BC81D106KE51K	CAP 10uF 20V 0805	2
0402ZD105KAT2A	CAP 1uF 10V 0402	2
C0805C106K8PACTU	CAP 10uF 10V 0805	3
GRM1555C1H102JA01D	CAP 1000pF 50V 0402	16
TSZU52C3V3_RGG	ZENER 3.3V 0603	9
LTST-C190GKT	GREEN LED	2
BLM18PG331SN1D	FERRITE BEAD 0603	2
SMA_CONNECTOR	SMA Connector	40
70246-1004	JTAG Connector	1
Power Supply Connector	POWER CONNECTOR 4.15mm	1
CRG0402F10K	RES 10K OHM 0402	3
CRG0402F1K0	RES 1K OHM 0402	7
CRG0402ZR	RES 0 OHM 0402	34
CRCW040224K0FKED	RES 24K OHM 0402	2
RC0402FR-07100RL	RES 100 OHM 0402	24
10M08SAE144C8G	IC MAX 10 FPGA	1
LMS8117ADTX-3.3/NOPB	LDO 3.3V	1
OPA4354AIDR	QUAD OP-AMP 2.7 to 5.5 V	2
SN74LVC1G34DBVR	BUFFER GATE	32
CB3LV-3C-50M0000	OSCILLATOR 50MHz 3.3V	1

Table 1. List of Components

4.1.3. PCB Layout

Once the schematic was completed, the PCB Layout was designed. A PCB can have multiple layers. In the case of this project, a 4-layer design was chosen due to the relatively small number of signals and traces. The PCB contains 4 signal layers made of copper, and separated by dielectric layers, made of insulating material. The parameters of each layer were chosen according to those used in the Lab for other projects. Therefore, the copper is material CF-004, with a weight of $2oz$ and a thickness of $0.07mm$ (or $2.756mil$). The middle dielectric layer is made of FR-4 and has a thickness of $25mil$, while the other two dielectric layers are made of FR-04, with a thickness of $15mil$. Additionally, there is an overlay layer and a solder layer, both at the top and the bottom of the PCB. The layer design is symmetric, as shown in Figure 17.

Next, the PCB was sized to fit all the components. The board was designed to contain the FPGA in the center, with all the connectors in the edges of the board. The project requires the use of at least 30 PWM signals, and 8 analog signals. As each pair of PWM signal is typically going to be used at the same time, it was decided to include an even number of SMA connectors on each edge. The final design contains the 8 analog signals SMA connectors, as well as the

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.4mil	3.5	
1	Top Layer 1	CF-004	Signal	2oz	2.756mil		
	Dielectric 2	FR-04	Prepreg		15mil	4.1	0.02
2	Layer 1	CF-004	Signal	2oz	2.756mil		
	Dielectric 1	FR-4	Dielectric		25mil	4.8	
3	Layer 2	CF-004	Signal	2oz	2.756mil		
	Dielectric 5	FR-04	Prepreg		15mil	4.1	0.02
4	Bottom Layer 1	CF-004	Signal	2oz	2.756mil		
	Bottom Solder	Solder Resist	Solder Mask		0.4mil	3.5	
	Bottom Overlay		Overlay				

Figure 17. Layer Configuration of the PCB.

JTAG and power connectors in one edge; 10 PWM connectors in two other edges each, and 12 PWM connectors in the last edge. Therefore, the board can generate 32 PWM signals, thus it can control 16 inverters. A separation of $100mil$ between each SMA connector was added so that each cable can fit properly. The final dimensions of the PCB are $4150mil$ $(125.73mm)$ of width and $4950mil$ $(105.41mm)$ of height, as shown in Figure 18. Additionally, a hole was added in each corner in order to add stand legs to the board.

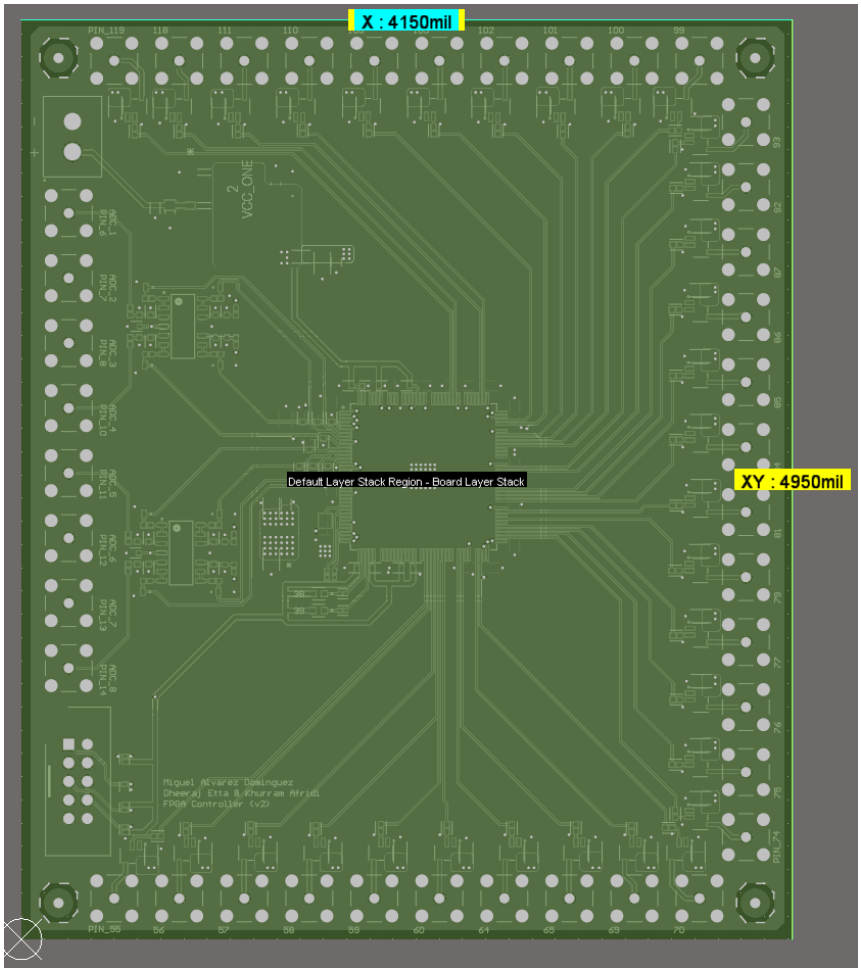


Figure 18. Dimensions of the PCB.

With the PCB shape and dimensions specified, all components were placed. A few rules were followed during this process:

- Most components will be placed in the top layer of the board.
- The FPGA should be in the center of the board, so that the trace of every PWM signal is approximately the same length; thus avoiding additional losses and any de-synchronization issues.
- All decoupling capacitors should be as close as possible to their respective IC pins, to filter as much noise as possible.
- The buffer gates for the PWM signals should be close to the SMA connector to maintain signal integrity, reduce noise and EMI and protect the FPGA from possible overloads.
- In the same way, the buffers for analog singals should be close to the SMA connectors.
- The oscillator should be as close as possible to the clock pin in the FPGA to maintain signal integrity.
- As most signals are high frequency, components should be placed in such a way that the traces create minimal loops. Additionally, a high frequency signal should stay on the same layer to reduce noise and EMI.

In order to add a component to the layout, it should have a footprint. Most commercially available components have a schematic designs, footprint, and 3D view available online in *Mouser* [27], *SnapEDA* [28], or *Ultra Librarian* [29]; while others can be downloaded directly from the *Altium Designer* software [15]. The component can be downloaded and included as a library, and then imported to the project. Each component library contains the schematic drawing, as well as all the 3D dimensions and the location and size of each copper pad that matches the physical characteristics of the device. The final layout of the PCB is shown in Figure 19. Note that the FPGA chip and the oscillator lack a 3D view, and only contain the location of all the copper pads. Additionally, some decoupling capacitors had to be added to the bottom of the PCB as they didn't fit in the top layer.

Once all components were placed, they were connected with traces and polygon pours. The traces have different widths depending on the type of signal. The power signals, such as VCC, VCC_ONE, VCCIO or VCCA will carry more current than analog and PWM signals. A PCB Trace Width Calculator [30] was used to determine the trace width. Power traces were sized to carry 1A of current and a 1.5 security factor, resulting in a trace width of $25mil$. In the case of PWM, analog and JTAG traces, that carry less than $100mA$, the default $8mil$ trace size was enough, with a security factor of more than 10.

All traces were routed to avoid loops and $90°$ corners, reducing losses, noise and EMI. In order to connect traces of different layers, vias were used. The vias had a $20mil$ diameter with a $10mil$ hole, which is suitable for the trace dimensions specified before. When multiple pads of the same signal were close together, a polygon was used instead of multiple traces. In order to connect polygons between layers, multiple vias were used. Figure 20 shows all the VCC_ONE traces and polygons. Those in red are in the top layer; those in yellow are in the second layer; while those in blue are in the bottom layer. Note the use of vias to connect different layers, and the use of polygons when multiple components are nearby.

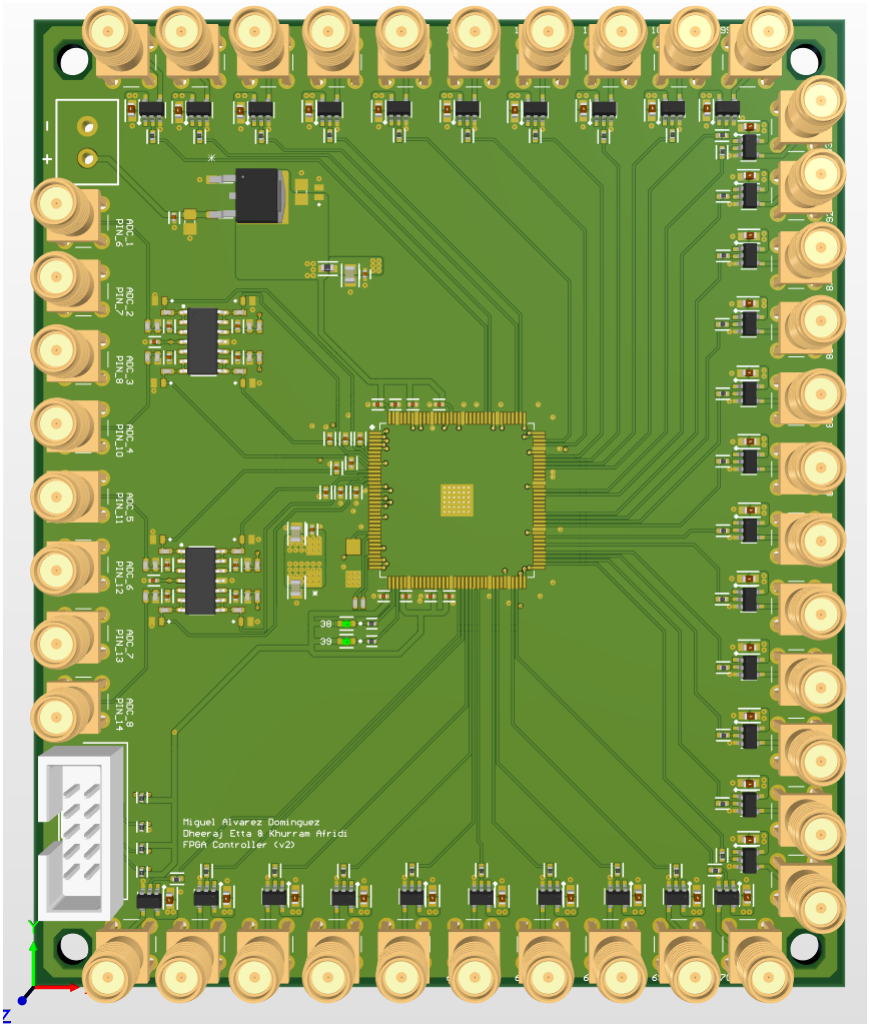


Figure 19. 3D View of the Final Layout of the PCB.

The signal VCC_ONE is obtained at the output of the LDO, in the polygon on the top-left corner, that connects the LDO output with the decoupling capacitors, the zener diode, and the ferrite bead. That ferrite bead is used to reduce noise from the analog secion between VCC_ONE and VCCA. The same approach was followed for the analog power VCCA signal, shown in Figure 21 (a). This signal is obtained from the top-left polygon, after the already mentioned ferrite bead.

The remaining traces were routed. Most of these traces consisted in a single connection between components. Most traces were routed in the top layer. However, in the case of the analog signals buffers, it was physically impossible to keep all traces in the top layer, thus the need to use the bottom layer for some signals, as shown in Figure 21 (b). This approach was necessary for both ICs.

After all components were placed and routed, a ground plane was added to fill the empty space of every layer. As these planes have a large surface, they also act as heat sinks, providing better cooling to the board. The final layout of the PCB was shown in Figure 19, while the design of all the layers is included in Appendix D.

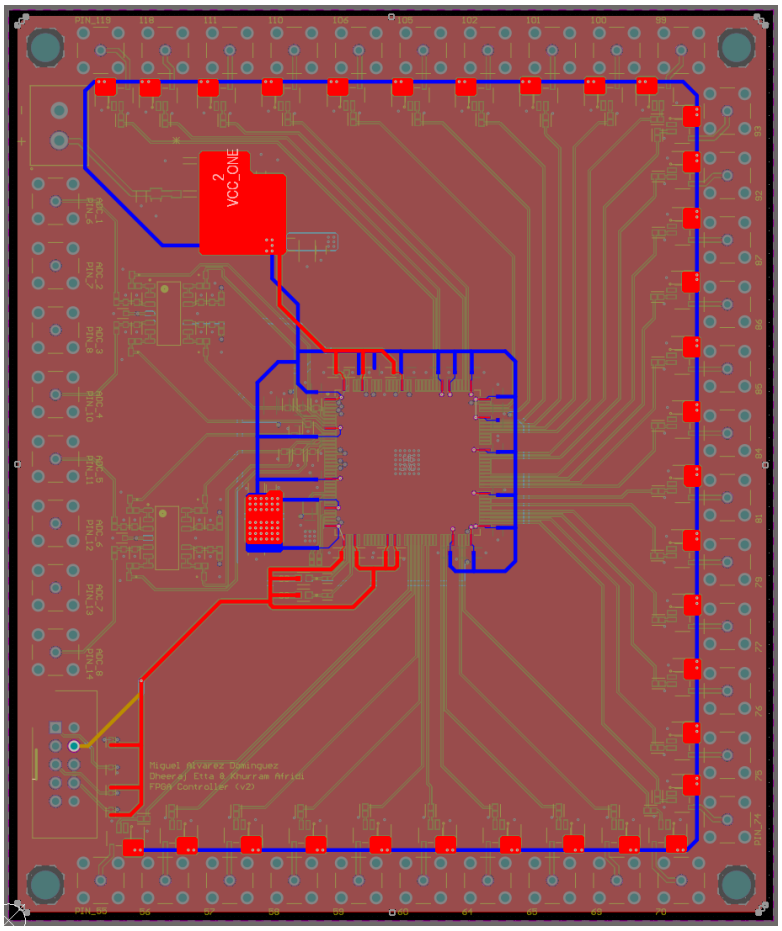
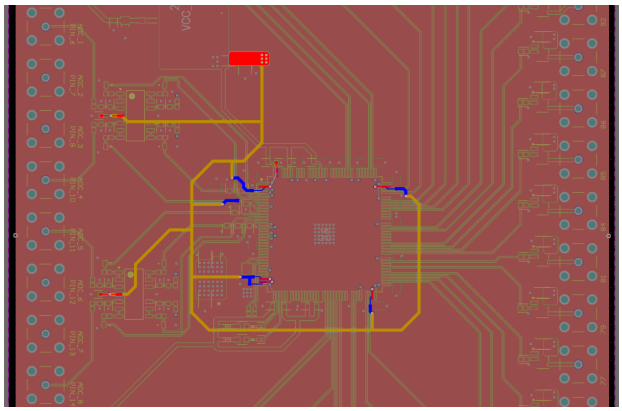
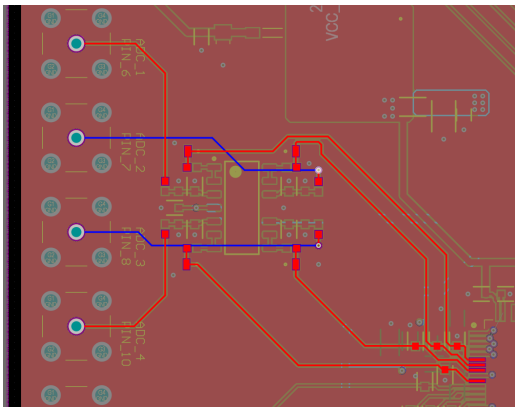


Figure 20. Highlight of Traces and Polygons of the VCC_ONE power signal.



(a) Traces and Polygons of the VCCA power signal.



(b) Traces of the Analog signals into and out of one Operational Amplifier.

Figure 21. Highlight of Traces of the VCCA power signal and Analog signals.

4.1.4. Soldering and Assembly

With the design finalized, the board was manufactured at a cost of less than $100, with exact price and order details maintained by the Lab. As mentioned before, there had been two design versions. The design explained above is the final version. However, the design that was sent for manufacturing is the first iteration. The main differences between both versions are:

- The first design didn't include the buffer gates for the PWM signals.

- The operational amplifiers output for the analog signals were clamped, as mentioned in the component selection section. The new design contains different operational amplifiers, which are rail-to-rail; thus having a larger upper threshold for the amplitude of the signals.
- The FPGA pins corresponding to each SMA connector was printed to improve the user experience of the board.
- The original LDO footprint had wrong pin numbers; which were fixed in the final version.

The manufactured board, with the stand legs, is shown in Figure 22. The FPGA chip can be seen on top of the board. However, the board comes without any component, which have to be soldered.

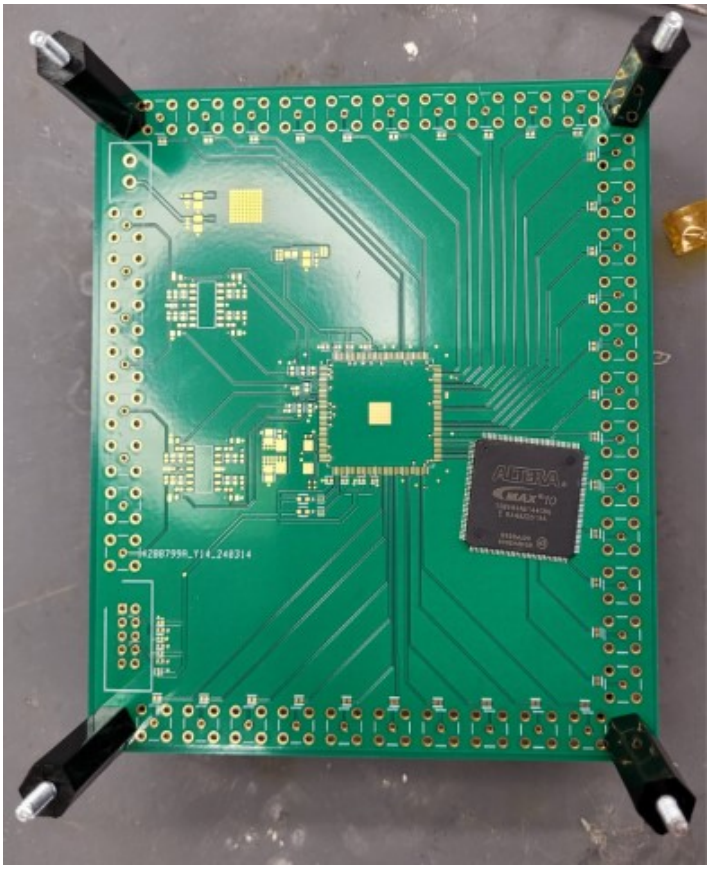


Figure 22. Empty Manufactured Board with Stand Legs and FPGA chip.

The first component to be soldered is the FPGA due to its high pin number. Each pin was soldered individually. The soldering process consists of adding solder paste, and later applying heat with a heat gun or a soldering iron. The temperature of the air from the heat gun was set to $380°C$, with an air flow of 12%. After soldering the FPGA, all decoupling capacitors and necessary components for the FPGA to work, such as the oscillator, were soldered, as shown in Figure 23.

Last, the JTAG connector, the LDO, one operational amplifier, and 12 SMA connectors (2 for analog signals, and 10 for PWM signals) were soldered with their respective resistors and capacitors. All components were soldered, with the exception of some SMA connectors and

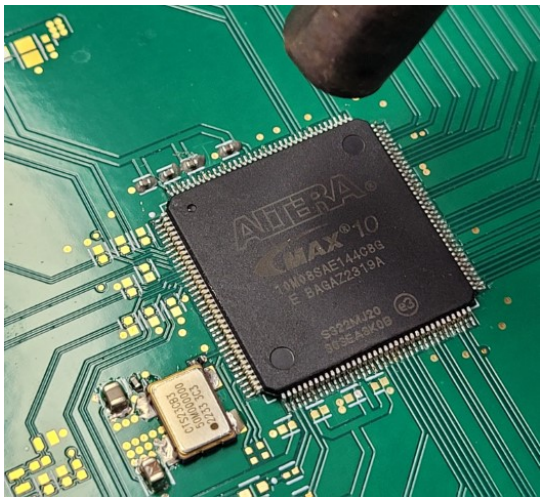
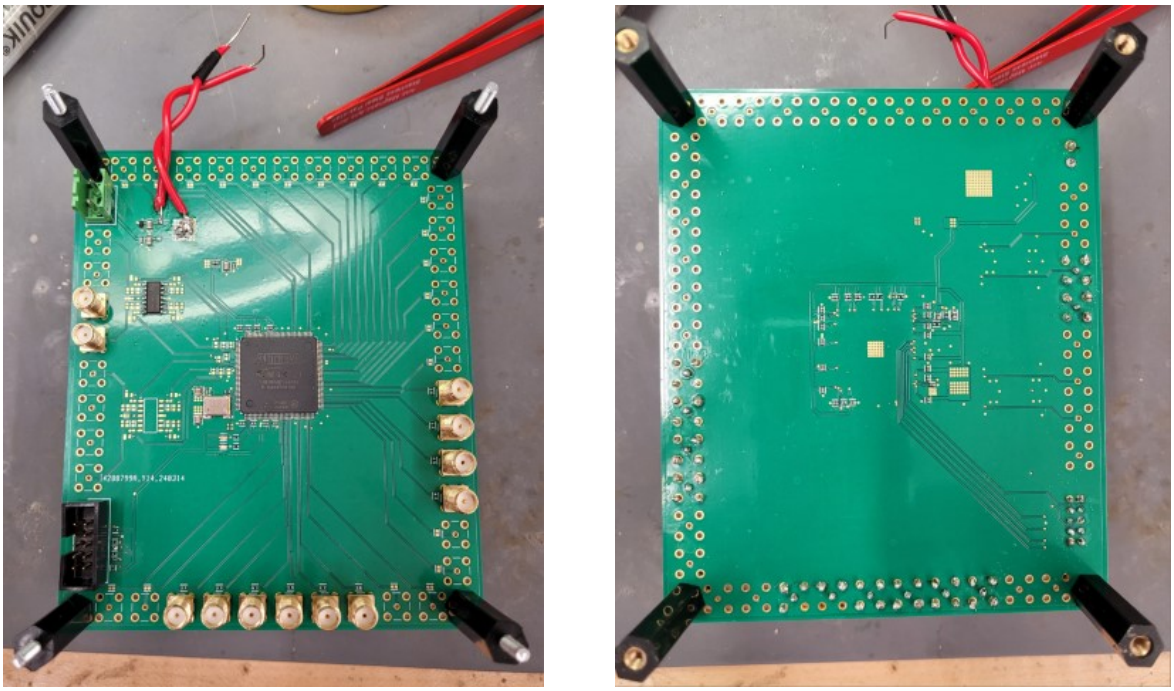


Figure 23. FPGA chip, Decoupling Capacitors, and Oscillator being soldered to the Board.

one operational amplifier, which were not needed at the time. When soldering the LDO it was discovered that some pin pads were not correctly configured, as mentioned above. Therefore, two wires were connected to the VCC_ONE and ground pads to externally power the board at $3.3V$, instead of $20V$, and the LDO was removed. The final board with all the necessary components is shown in Figure 24. As new projects requiring additional inverters are carried out, the necessary components to provide more PWM signals will be soldered.



(a) Top View **(b)** Bottom View

Figure 24. Top and Bottom View of the Soldered Board.

This version of the board was used for testing, as well as in different Lab projects with inverters. The next section will explain the how each experiment was set up, as well as all the different devices and components used in each of them.

4.2. Experimental Setup

The board was tested in various environments and configurations to ensure the system's correct behavior. First, the loading capacities of the board were evaluated. Next, the integrity of the PWM signals was verified. Last, the board was tested in a real WPT system with 6 inverters. Additionally, the analog input capabilities of the board were also assessed. The code employed to program the FPGA and generate PWM signals is listed in Appendix B.

4.2.1. Load Capacity Evaluation

The first experiment consisted of evaluating the performance of the controller when attached to different loads. Inverters already available in the Lab were used as loads. Each inverter was designed to receive two PWM signals. Additionally, each inverter could be configured to receive their own PWM signals, or to share them with other inverters, by shorting or opening certain pads in their PCB. Note that the devices were not inverting any current at the time of testing; they were only used as loads. The following scenarios were tested:

a) Providing 2 PWM signals to 1 full bridge inverter using 2 SMA connectors.

b) Providing 2 PWM signals to 2 full bridge inverters using 2 SMA connectors.

c) Providing 2 PWM signals to 3 full bridge inverters using 2 SMA connectors.

d) Providing 2 PWM signals to 1 two-parallel device full bridge inverter using 2 SMA connectors.

e) Providing 2 PWM signals to 1 two-parallel device full bridge inverter using 2 SMA connectors, $180°$ apart.

All PWM signals were configured to be $6.78MHz$, 25% duty ratio, and $0°$ phase (with the exception of the last case, where the signals are $180°$ apart). The method used to program the FPGA is the same as the one explained in Section 4.1.1. The complete code used to program multiple pins of the FPGA to provide PWM signals is reproduced in Appendix B.

The board was externally powered at $3.3V$. A JTAG connector was used to connect the FPGA to the computer and program it; and cables with SMA connectors were used to connect the controller board to the inverters. This experiment, aside from testing the load capacity of the controller, was used to test that the board worked properly, and everything was correctly soldered. The PWM signals were probed with an oscilloscope at the inverter's side. The results are shown in Chapter 5.

4.2.2. PWM Signal Integrity Verification

Next, the integrity of the PWM signals was verified with the inverter that was going to be later used in a real WPT system. The inverter was designed by other members of the Lab. It consisted of 3 two-parallel device full bridge inverters in a single PCB, for a total of 6 inverters. Although the device had already been designed, it needed to be assembled, thus help during the soldering process was provided. The top view of the device, containing 3 of the inverters, is shown in Figure 25. The bottom view contains the other 3 parallel inverters, and is symmetrical to the

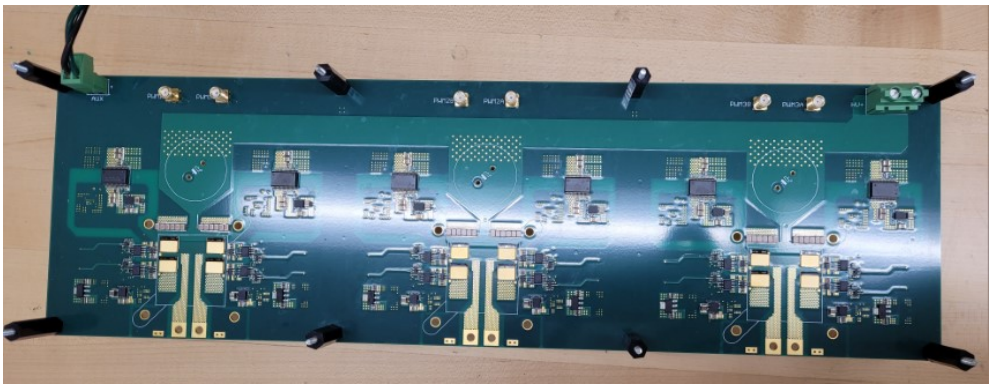


Figure 25. Top View of the 3 two-parallel device full bridge inverters.

top one. Note that the device lacks decoupling capacitors, that were added when assembling the WPT system.

The device comprises two sections: one containing the gate drives and MOSFET control mechanism (including necessary buffers and voltage regulators), and another housing the MOSFETs responsible for current inversion. The gate drive section is externally powered at $20V$. Internal voltage regulators convert the voltage down to $6V$. The PWM signals at $3.3V$ are feeded into this section. Buffer gates are added to convert the waveform to $6V$ volt signals. The buffer gates threshold for HIGH or LOW values is at approximately $2.5V$, so HIGH and LOW values from the PWM signals are correctly detected. Next, the adjusted $6V$ PWM signals are connected to the gate drives and the MOSFETs to control the inversion process.

The inverter device contains 3 two-parallel inverters. Each two parallel inverters receive their own 2 PWM signals (the 2 signals are shared between the two parallel devices). However, for the parallel devices, they should be synchronized in order to maximize the efficiency, as their outputs are combined. This experiment verifies that the integrity of the PWM signals arriving at the inverters is maintained, thus being synchronized. Each inverter was controlled with 2 PWM signals, with parallel devices sharing. All signals were configured to be $6.78MHz$, 40% duty ratio, and $180°$ phase between the 2 PWM signals each inverter receives. As in the previous experiment, the FPGA board was powered at $3.3V$, and connected to the inverter device and to the computer, for programming with the code in Appendix B. The inverter device was powered at $20V$. To ensure that all signals are correctly synchronized, the gates of every two parallel MOSFETs were probed simultaneously, for every MOSFET.

The experimental setup is shown in Figure 26. The image shows the external power source, the controller board, and the inverter device. The latter is positioned vertically so that the two parallel MOSFET gates could be probed at the same time. The obtained results are displayed in Chapter 5.

4.2.3. Real System Application

Once the board was tested, it was employed in a real Capacitive WPT System. This system, designed by other members of the Lab, combines the parallel inverters and the stacked inverters architectures proposed in Section 1.2. The topology of the system is the same as the one shown in Figure 1, with a few adjustments.

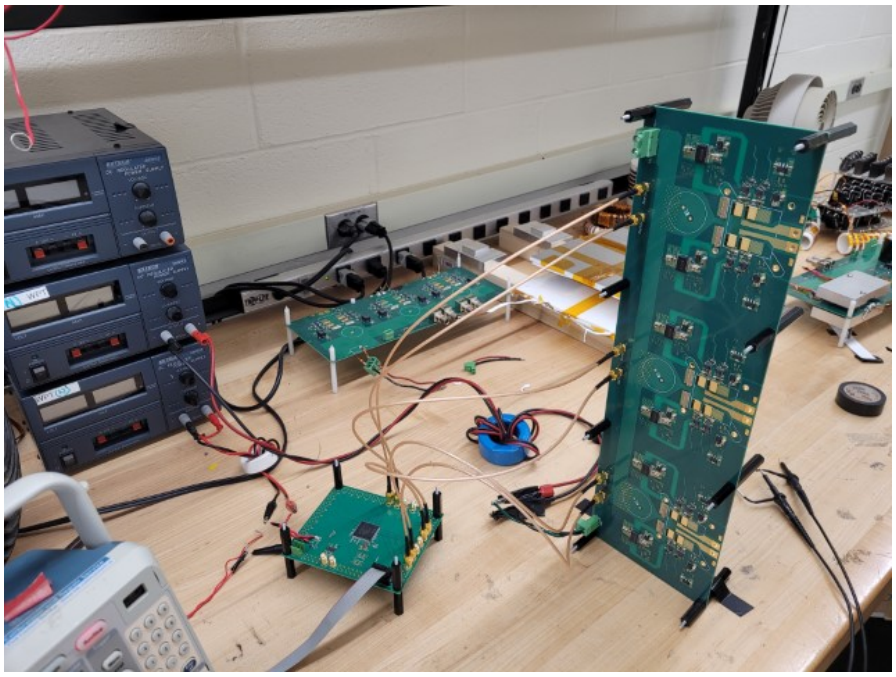


Figure 26. Experimental Setup to Verify PWM Signal Integrity.

The device explained in the previous section was used, with 3 two-parallel inverters, for a total of 6 inverters. Every pair of parallel inverters were connected to a parallel-in, series-out transformer, combining all of the inverters. Next, the system contains the primary side matching network, the two capacitors, and the secondary side matching network. Instead of using a single rectifier, 3 parallel ones were used to increase the maximum power capabilities of the system. Three series-in, parallel-out transformers were used to divide the power into the three rectifiers. The outputs of the rectifiers were then connected in parallel.

As with the inverter device, the WPT system had already been designed by Lab member Dheeraj Etta. However, some components needed to be built: the six transformers, and the three rectifiers. The rectifiers were built screwing 4 diodes to a heat sink. The legs of the diodes were appropriately connected using copper wire. Last, a $2\mu F$, $400V$ decoupling capacitor was added at the output of each rectifier. The three rectifiers are shown in Figure 27.

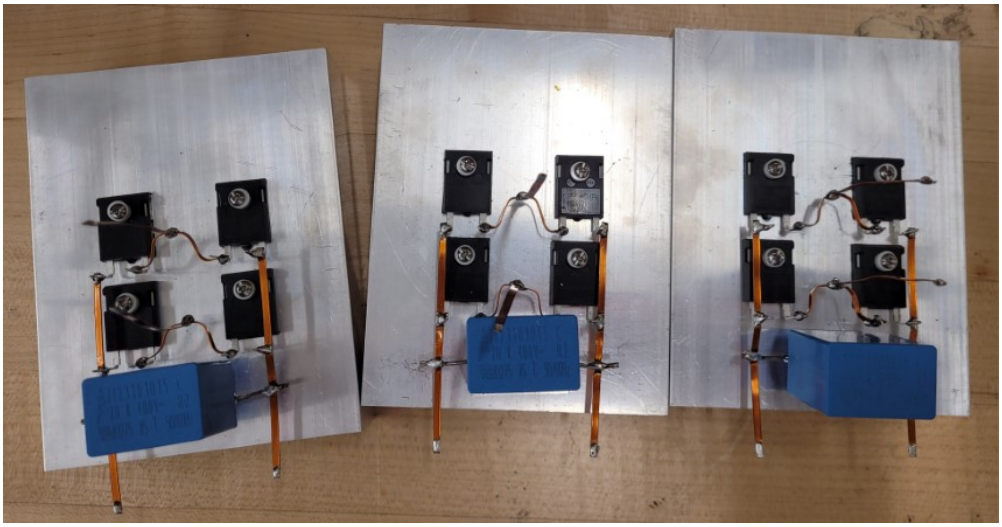


Figure 27. Three Rectifiers Used in the Capacitive WPT System.

The requirements for the transformers were: air core to reduce core losses at high frequency, 3 turns in both primary and secondary sides (three of the six transformers required provision for 2 and 1 turns), and an open circuit inductance of close to $460nH$. The transformers were built using $.015x.280$ inch flat copper wire, electrically insulating tape, and empty plastic tubes as support. The final transformers are shown in Figure 28. Note that the thin soldering wires

Figure 28. Six Rectifiers Used in the Capacitive WPT System.

attached to every end were only used to measure the inductance of each device, as shown in Figure 29, and were later removed when attached to the system. The inductance values obtained for each transformer are listed in Table 2, which are close to the required value, meaning these transformers can be used in the system.

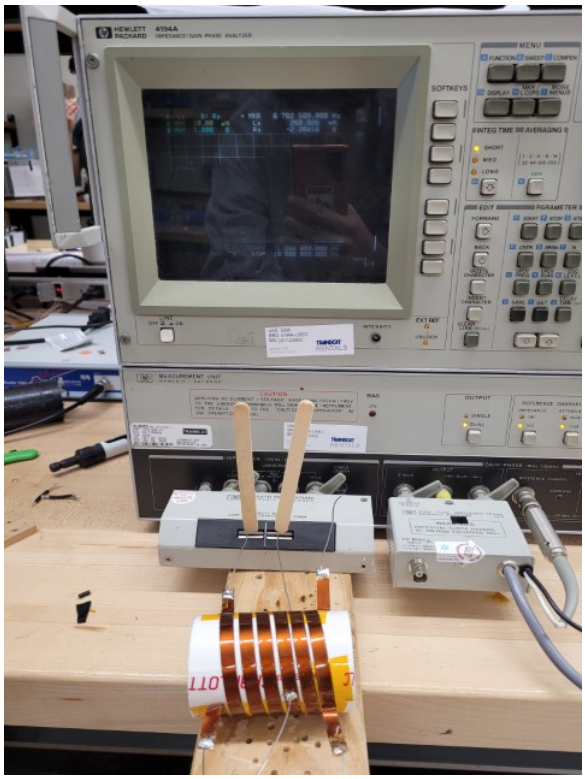


Figure 29. Measurement of the Inductance of one Transformer.

Transformer #	Open Circuit Inductance (nH)	Short Circuit Inductance (nH)
1 (3 turns)	451.06	332.348
1 (2 turns)	318.706	260.218
1 (1 turn)	199.415	187.513
2 (3 turns)	470.319	346.825
3 (3 turns)	463.977	333.95
4 (3 turns)	468.956	337.579
5 (3 turns)	478.339	349.025
5 (2 turns)	319.602	260.862
5 (1 turn)	184.67	171.288
6 (3 turns)	471.075	343.695
6 (2 turns)	321.885	263.852
6 (1 turn)	187.597	174.786

Table 2. Inductance Values of Each Transformer

All the components were connected to the Capacitive WPT System, including the inverters and the FPGA controller board, as shown in Figure 30. Different oscilloscopes were later included to probe the voltage and current of certain nodes. The testing was carried out by Lab member Dheeraj Etta. The goal of the project is to transfer $12kW$ of power. However, at the time of writing, only $4kW$ of power transfer have been tested. The results, obtained by Dheeraj, using the controller board presented here, are shown in Chapter 5.

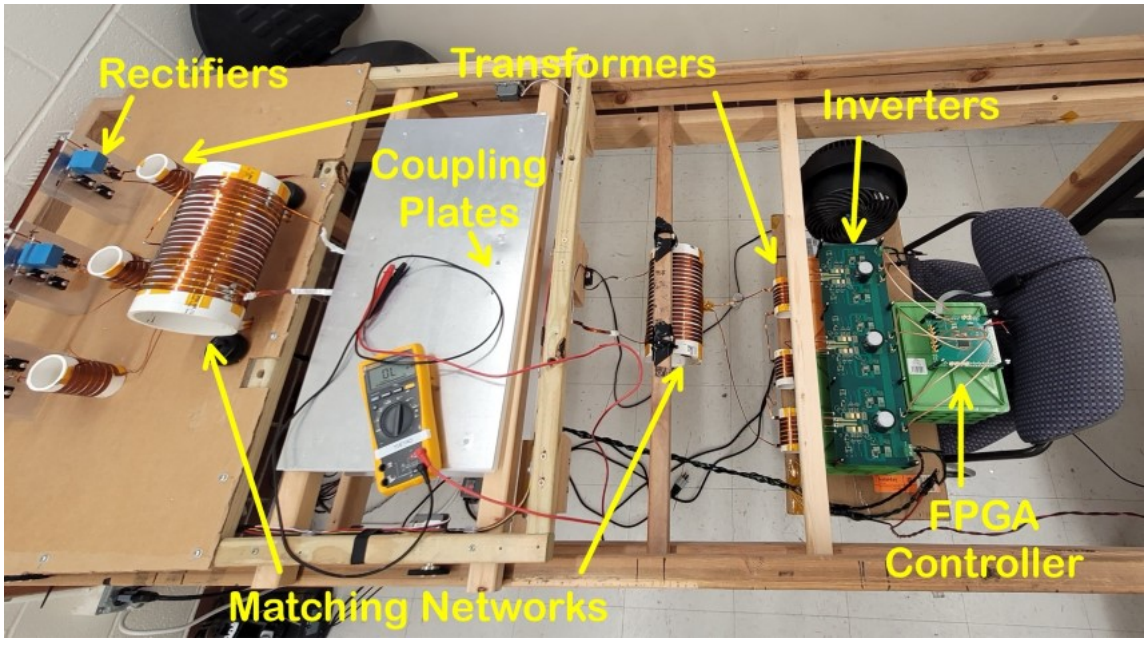


Figure 30. Setup for the Testing of the Capacitive WPT System.

4.2.4. Analog Input Capabilities Assessment

Last, analog inputs to the board were tested. To assess the capabilities of the board, a waveform generator was used. It was connected through SMA connectors to the analog section

of the board. Sine waves with an amplitude of $3.3V$ and $1MHz$ frequency were given to the board. The output of the buffer was probed to test the signal. It was discovered that the signals were clamped at $2V$, due to the Input Voltage Range of the LM2902DR2 operational amplifiers (Figure 31), which were not rail-to-rail devices. New rail-to-rail operational amplifiers were added to the final design of the FPGA board, as mentioned in Section 4.1.2.4, which should then be tested once the board is manufactured and assembled in the future.

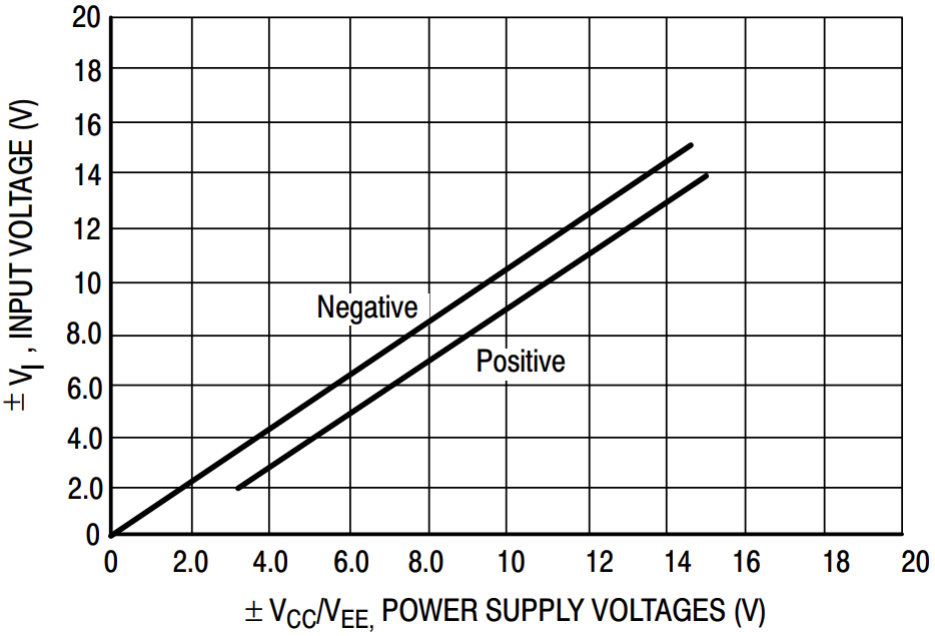


Figure 31. Input Voltage Range of the LM2902DR2 [26].

Chapter 5

Analysis of Results

THIS chapter presents and discusses the results obtained from the different experiments explained in Section 4.2.

5.1. Load Capacity Evaluation

Figure 32 shows the PWM waveforms obtained at the inverter side for every scenario. The dark blue and light blue waveforms represent the respective PWM signals. For convenience, each scenario is listed again below.

a) Providing 2 PWM signals to 1 full bridge inverter using 2 SMA connectors.

b) Providing 2 PWM signals to 2 full bridge inverters using 2 SMA connectors.

c) Providing 2 PWM signals to 3 full bridge inverters using 2 SMA connectors.

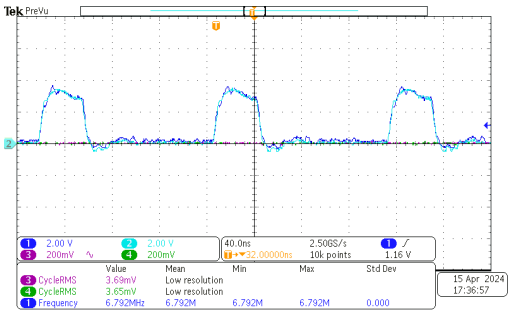
d) Providing 2 PWM signals to 1 two-parallel device full bridge inverter using 2 SMA connectors.

e) Providing 2 PWM signals to 1 two-parallel device full bridge inverter using 2 SMA connectors, $180°$ apart.

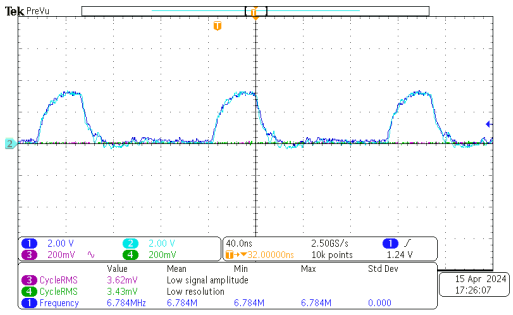
The amplitude of every signal is $3.3V$, and the frequency is $6.78MHz$. The duty ratio is also 25%, as specified. However, the rise time of each scenario is different. As the number of inverters increases, the load of the controller increases. As the load increase, the time constant increases (Equation 1), and the PWM signal gets an exponential shape.

$$\tau = R \cdot C \tag{1}$$

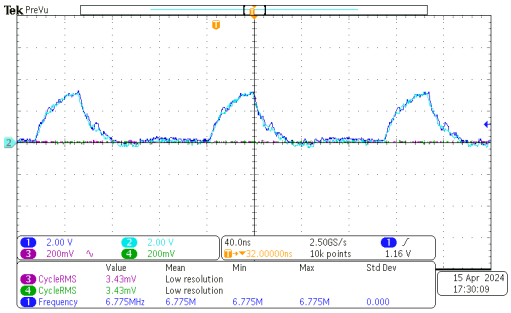
The PWM signal degrades significantly after 3 inverters are added (Figure 32 (c)); therefore, a single PWM can successfully control up to 2 inverters. Additionally, paralleling two inverters can improve the response of the PWM, as each inverter receives their own PWM signal. Last, the correct phase is applied to the PWMs: waves in scenarios a) through d) are in phase, while the waves in scenario e) are out of phase $180°$. Throughout this experiment it was confirmed that the controller board worked as expected, and was able to produce the desired PWM signals.



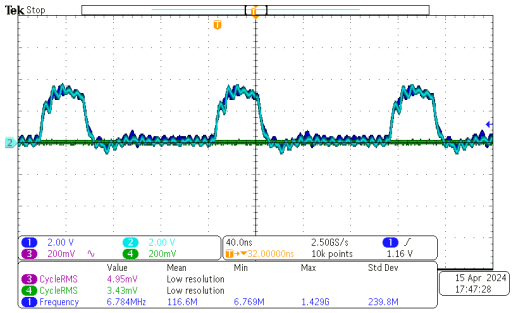
(a) 1 full bridge inverter.



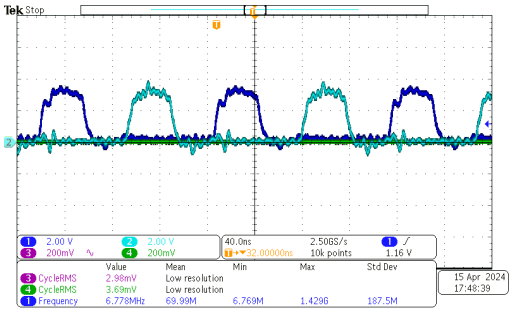
(b) 2 full bridge inverters.



(c) 3 full bridge inverters.



(d) 1 two-parallel device.



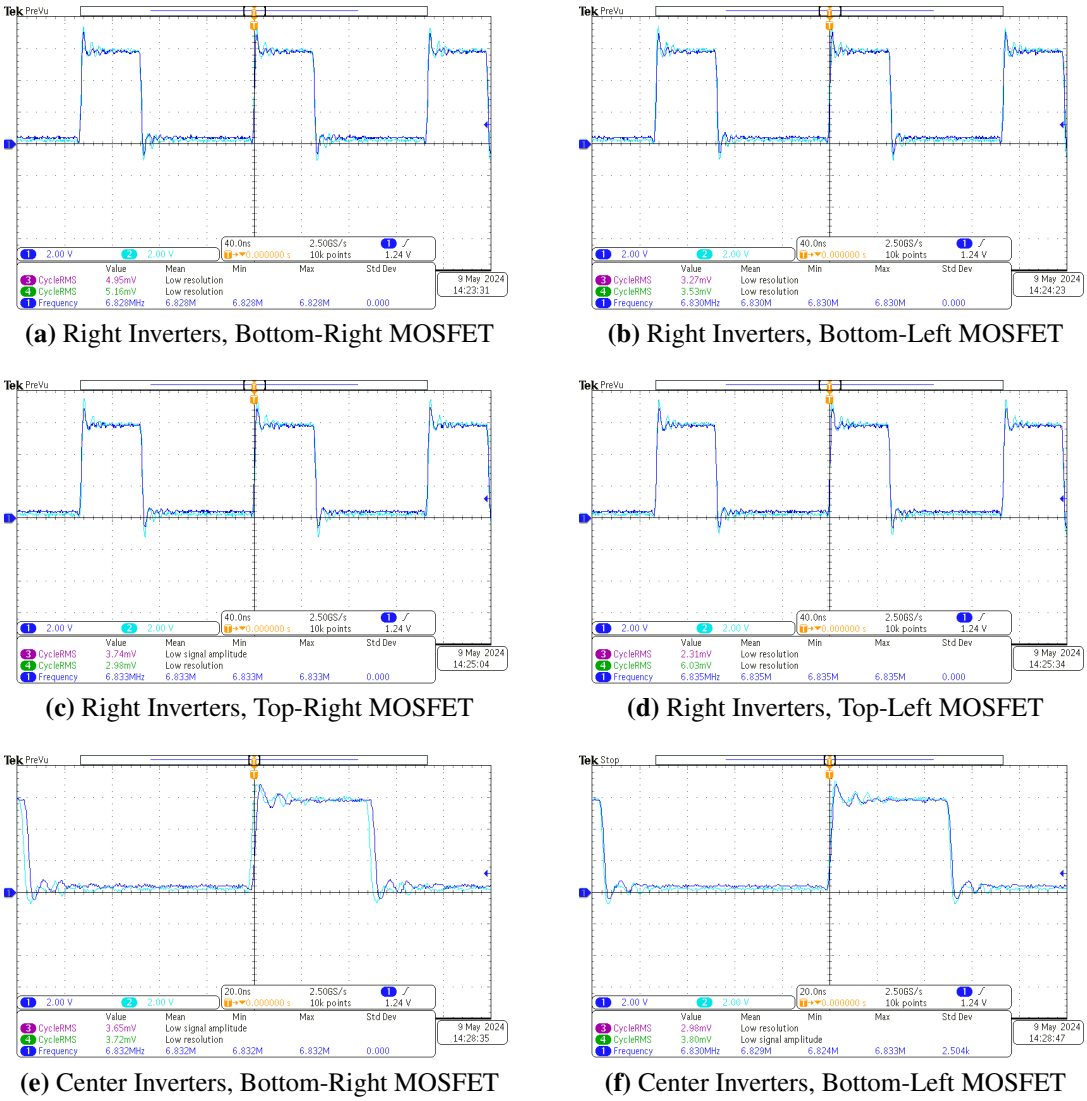
(e) 1 two-parallel device, 180° apart.

Figure 32. PWM Waveforms of each Scenario.

5.2. PWM Signal Integrity Verification

The PWM signals obtained at the gate of every two parallel MOSFETs are shown in Figure 33. The dark blue signal corresponds to the gate of the MOSFET in the top inverter, while the light blue one corresponds to the gate of the MOSFET in the bottom inverter. The waveform labels are referred to the device's view in Figure 25.

The results show PWM waveforms of $6V$ and 40% duty cycle. The increase in voltage from the FPGA at $3.3V$ to $6V$ at the MOSFET gate is due to the buffer gates before the gate drives in the inverter board, as mentioned in Section 4.2.2. All signals are synchronized, with the exception of Figure 33 (e), where there is a slight mismatch between the PWM at the parallel MOSFET gates. All of the other Center Inverters waveforms are synchronized. Therefore, there is a problem with some component in the inverter board, as the two PWM signals used for each of the 4 parallel MOSFET gates are exactly the same. Replacing the buffer gates for the bottom-right MOSFETs in the middle inverters fixed the problem.



(a) Right Inverters, Bottom-Right MOSFET

(b) Right Inverters, Bottom-Left MOSFET

(c) Right Inverters, Top-Right MOSFET

(d) Right Inverters, Top-Left MOSFET

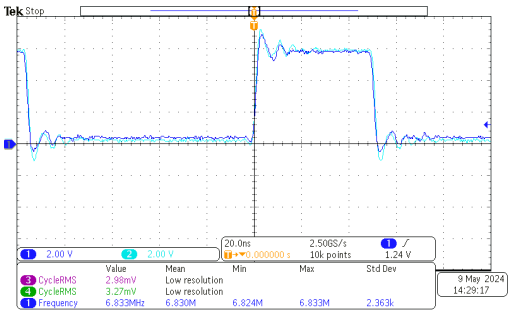
(e) Center Inverters, Bottom-Right MOSFET

(f) Center Inverters, Bottom-Left MOSFET

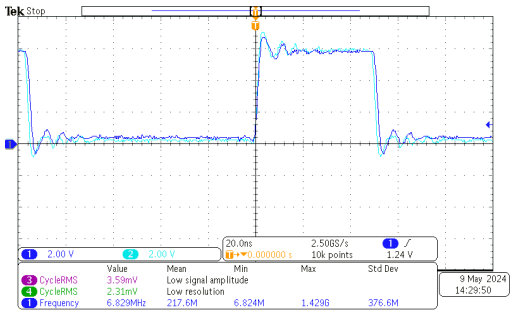
Figure 33. PWM Signals of Parallel MOSFET Gates (Part 1)

Even though the two PWM signals for every inverter were configured to be $180°$ apart, Figure 33 shows the PWMs at parallel MOSFETs, and not between MOSFETs of the same inverter, thus they always have the same phase.

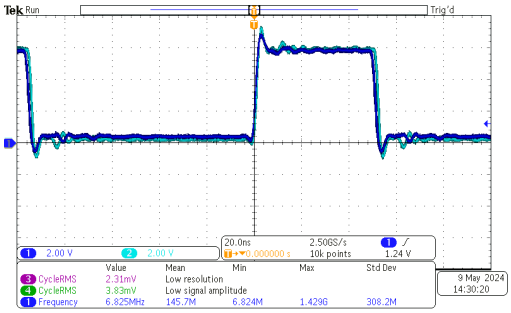
The experiment presented here, as well as the previous one in Section 5.1, prove that the controller board can generate multiple PWM signals to control multiple inverters, with the desired parameters, and while staying synchronized. The last step in the testing phase is using the controller board in a real WPT system.



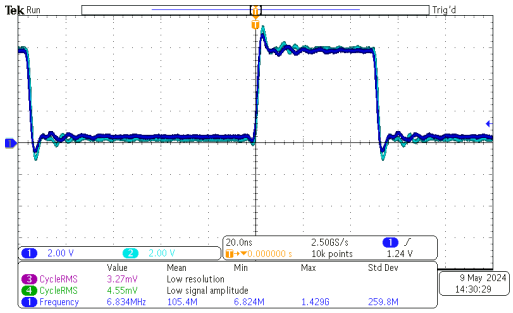
(g) Center Inverters, Top-Right MOSFET



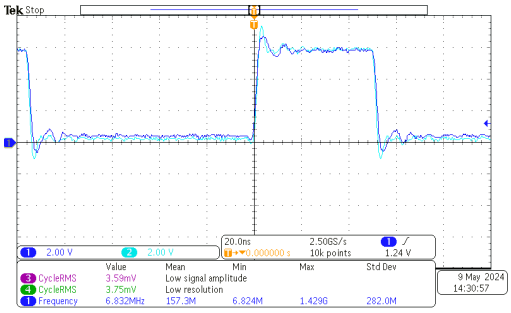
(h) Center Inverters, Top-Left MOSFET



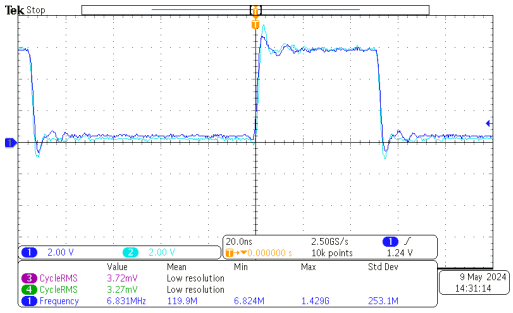
(i) Left Inverters, Bottom-Right MOSFET



(j) Left Inverters, Bottom-Left MOSFET



(k) Left Inverters, Top-Right MOSFET



(l) Left Inverters, Top-Left MOSFET

Figure 33. PWM Signals of Parallel MOSFET Gates (Part 2)

5.3. Real System Application

As explained in Section 4.2.3, the controller board was employed to control a real capacitive WPT system. Help was provided in the setup process, building and connecting the necessary components. However, the experiment was run by Dheeraj Etta, and the results obtained are his own [31].

The controller board was used to control the 6 inverters. The system was able to transfer $4kW$ of power, with an efficiency of 86% [31], as shown in Figure 34. The voltage at the switch nodes of each two parallel inverters is $288V$, $266V$, and $277V$, respectively. The input DC current at the transistors is $17.5A$; and the output DC voltage after rectification is $400V$. The system has not been tested at full power, yet. It will be tested again in the future, as it has been designed to transfer a maximum of $12kW$ of power.

This experiment shows that the board can successfully control multiple inverters (in this case, 6 inverters). Therefore, it can be used for further projects in Capacitive Wireless Power Transfer

research, enabling the increase of power transfer capabilities of capacitive WPT systems. This board can also be used in any other scenario that requires precise PWM signal generation.

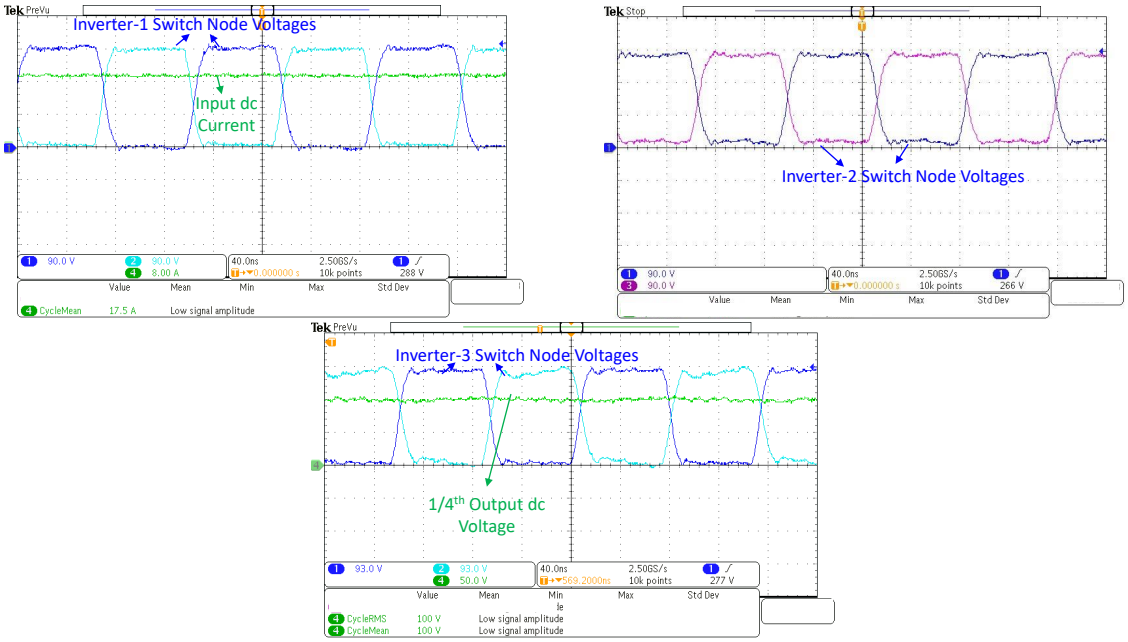


Figure 34. Results from the Capacitive WPT System using the FPGA board [31].

Chapter 6

Conclusions and Future Directions

THE experiments performed, and the subsequent results, demonstrate the successful development of an FPGA Controller for High-Power, Multi-MHz, Capacitive WPT System. The total cost of the device is less than $\$210$ ($\$110$ for components and $\$100$ for the board), which is a tenth of the price of the cheapest waveform generator.

The objectives of the project have also been met: the FPGA was first tested in the evaluation board, verifying that it was suitable for the purposes of the project. A code was also developed to program the FPGA, which became the foundation of the code used to control real inverters. Next, a PCB was designed with all the necessary components, which is capable of producing 32 PWM signals, and receiving 8 analog signals. The PCB was also manufactured, populated, and soldered. The operation of the device was tested, and proven to be successful: the integrity of the signals was maintained, while being synchronized. The board was successfully employed in a real capacity WPT system, obtaining a $4kW$ power transfer, with an 86% efficiency. Additionally, the skills needed to program the FPGA, design the PCB, and build and solder power electronics were acquired during the development of the project.

This project, however, can be further evolved. Issues with the LDO and operational amplifiers found during testing have been fixed and incorporated into the new proposed design. The new design, aside from fixing problems that arose during testing, incorporates other improvements, such as pin numbering for every connector, and the use of buffer gates to increase the output current of the PWM signals. This design is to be manufactured and soldered in the future by other members of the Lab.

Future iterations of the design can further improve the board. As each inverter board contains 6 inverters, 6 different cables and SMA connectors are needed to connect the FPGA board to the inverter device. In order to reduce the number of components, and facilitate the connection, multi-port RF connectors are suggested [32]. Each of these connectors contains multiple RF ports; thus a single component could be used to send 6 PWM signals from the controller board to the inverter device. Additionally, they are suitable for high frequency applications. Commercially available options are yet to be found.

In conclusion, the development of this FPGA controller represents a significant advancement for Cornell University's Power Electronics Lab Group, specially in the case of High Power Capacitive Wireless Power Transfer Systems. By providing PWM waveform generation at a low cost, this device unlocks previously inaccessible research areas. Beyond its immediate application, the FPGA board can be utilized across various projects requiring precise multiple-

PWM generation. This innovation not only supports ongoing research but also positions the Lab group at the forefront of Capacitive Wireless Power Transfer research.

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Appendix A

Alignment with Sustainable Development Goals (SDGs)

THE development of the FPGA Controller is part of a bigger project in Cornell's Power Electronics Lab Group: the research in capacitive WPT systems for EVs. This primary Sustainable Goal (SDG) this project addresses is *Goal 9*.

- *Goal 9. Build resilient infrastructure, promote inclusive and sustainable industrialization and foster innovation.*
  The FPGA Controller will broaden the research limits for the capacitive WPT system, enabling better testing and reliable results, closer to real world scenarios. The capacitive WPT project will enable the industry to modernize, building an infrastructure that will potentially increase the mass adoption of EVs, with more convenient and efficient means of charging.

Nevertheless, this project also addresses other SDGs.

- *Goal 7. Ensure access to affordable, reliable, sustainable and modern energy for all.*
  The capacitive WPT system will increase the access to affordable and clean energy, while potentially reducing its cost. EVs will be charged more conveniently, reducing charging time and range limitations; thus promoting the use of sustainable energy transportation.
- *Goal 11. Make cities and human settlements inclusive, safe, resilient and sustainable.*
  The use of capacitive WPT systems can contribute to more sustainable cities, increasing the use of EVs, and therefore reducing the dependence on fossil fuels, and other polluting means of transport.
- *Goal 13. Take urgent action to combat climate change and its impacts.*
  In relation to the previously mentioned goals, an improved charging infrastructure that promotes the use of EVs can significantly reduce the number of conventional gas vehicles, thus reducing the total greenhouse gas emissions from the road.

Appendix B

FPGA Code

THE following, Code 2, is the VHDL code used to program the FPGA board and generate PWM signals during the experiments. Note that, in order for it to work, the *Altera PLL IP Core* needs to be included in the project: it should be selected from the *IP Catalog*, inside the *Tools* tab, and is found under *Library - Basic Functions - Clocks; PLLs and Resets - PLL - ALTPLL*. Additionally, every I/O signal should be connected to its corresponding FPGA pin with the *Pin Planner* tool, inside the *Assignments* tab.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all; -- for addition & counting
use ieee.numeric_std.all; -- for type conversions
use ieee.std_logic_arith.all;

entity WirelessChg is
  port (
    clk : in std_logic;

    PWM_A_1, PWM_A_2, PWM_B_1, PWM_B_2, PWM_C_1, PWM_C_2 : out
       std_logic;
    PWM_D_1, PWM_D_2, PWM_E_1, PWM_E_2, PWM_F_1, PWM_F_2 : out
       std_logic;
    PWM_G_1, PWM_G_2, PWM_H_1, PWM_H_2, PWM_I_1, PWM_I_2 : out
       std_logic;
    PWM_J_1, PWM_J_2, PWM_K_1, PWM_K_2, PWM_L_1, PWM_L_2 : out
       std_logic;
    PWM_M_1, PWM_M_2, PWM_N_1, PWM_N_2, PWM_O_1, PWM_O_2 : out
       std_logic;
    PWM_P_1, PWM_P_2 : out std_logic;

    LED_1, LED_2 : out std_logic;

    enable : in std_logic
  ) ;
end WirelessChg;


architecture Behavioral of WirelessChg is
```

```
  signal cOutput0, cOutput1, cOutput2, cOutput3, cLocked : std_logic;

  component my_pll is
    port (
      areset : IN std_logic := '0';
      inclk0 : IN std_logic := '0';
      c0     : OUT std_logic;
      c1     : OUT std_logic;
      c2     : OUT std_logic;
      c3     : OUT std_logic;
      locked : OUT std_logic
    );
  end component my_pll;


begin

  my_pll_1 : my_pll
    port map (
      areset => '0',
      inclk0 => clk,
      c0     => cOutput0,
      c1     => cOutput1,
      c2     => cOutput2,
      c3     => cOutput3,
      locked => cLocked
    );

  -- Signals to be connected to the desired clock output.
  -- Clocks can be configured in the Altera PLL IP Core.
  -- Connect the PWM signals in the Pin Planner to the desired FPGA
     pin, according to the PIN numbers printed in the controller
     board.

  PWM_A_1 <= cOutput0;
  PWM_A_2 <= cOutput1;

  PWM_B_1 <= cOutput2;
  PWM_B_2 <= cOutput3;

  PWM_C_1 <= cOutput0;
  PWM_C_2 <= cOutput1;

  PWM_D_1 <= cOutput2;
  PWM_D_2 <= cOutput3;

  PWM_E_1 <= cOutput0;
  PWM_E_2 <= cOutput1;

  PWM_F_1 <= cOutput2;
  PWM_F_2 <= cOutput3;
```

```
  PWM_G_1 <= cOutput0;
  PWM_G_2 <= cOutput1;

  PWM_H_1 <= cOutput2;
  PWM_H_2 <= cOutput3;

  PWM_I_1 <= cOutput0;
  PWM_I_2 <= cOutput1;

  PWM_J_1 <= cOutput2;
  PWM_J_2 <= cOutput3;

  PWM_K_1 <= cOutput0;
  PWM_K_2 <= cOutput1;

  PWM_L_1 <= cOutput2;
  PWM_L_2 <= cOutput3;

  PWM_M_1 <= cOutput0;
  PWM_M_2 <= cOutput1;

  PWM_N_1 <= cOutput2;
  PWM_N_2 <= cOutput3;

  PWM_O_1 <= cOutput0;
  PWM_O_2 <= cOutput1;

  PWM_P_1 <= cOutput2;
  PWM_P_2 <= cOutput3;

  -- LEDs are configured to turn ON when the board is powered.
  -- They can be configured as desired.

  LED_1 <= '0';
  LED_2 <= '0';

end architecture Behavioral;
```

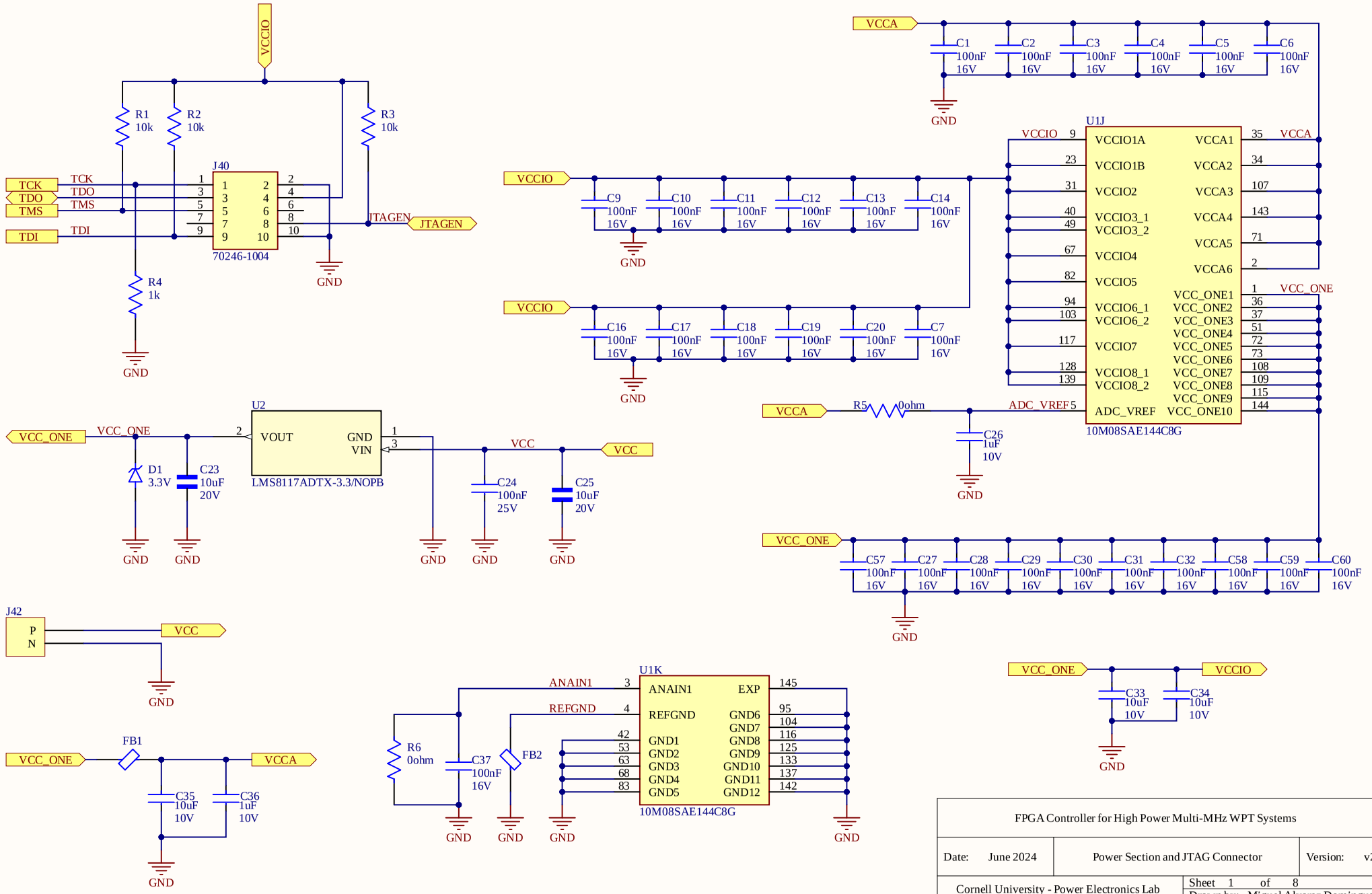
Code 2. Complete FPGA Code

Appendix C

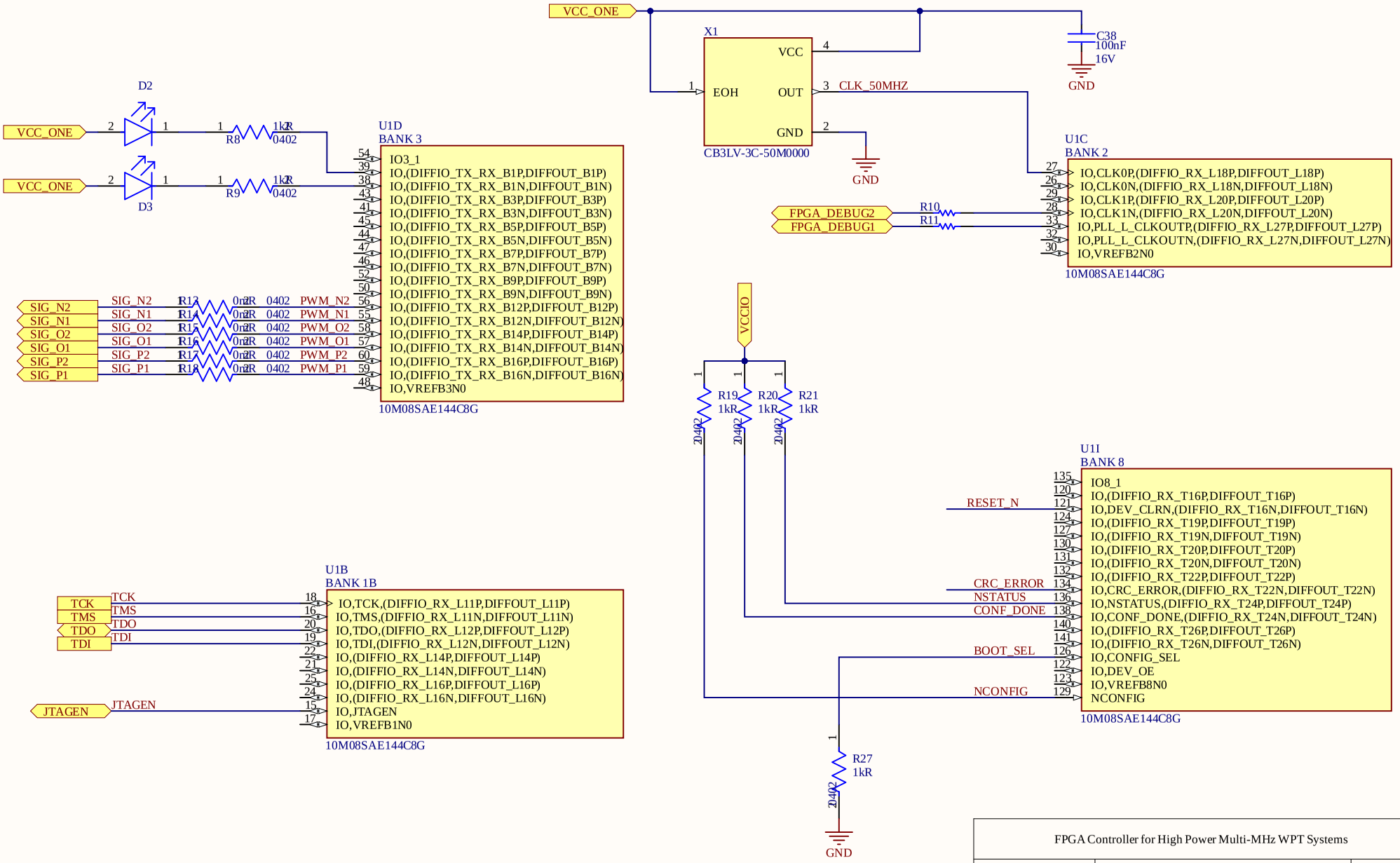
PCB Schematics

THE following pages contain the circuit schematics of the PCB designed in this project. The drawings are divided as follows:

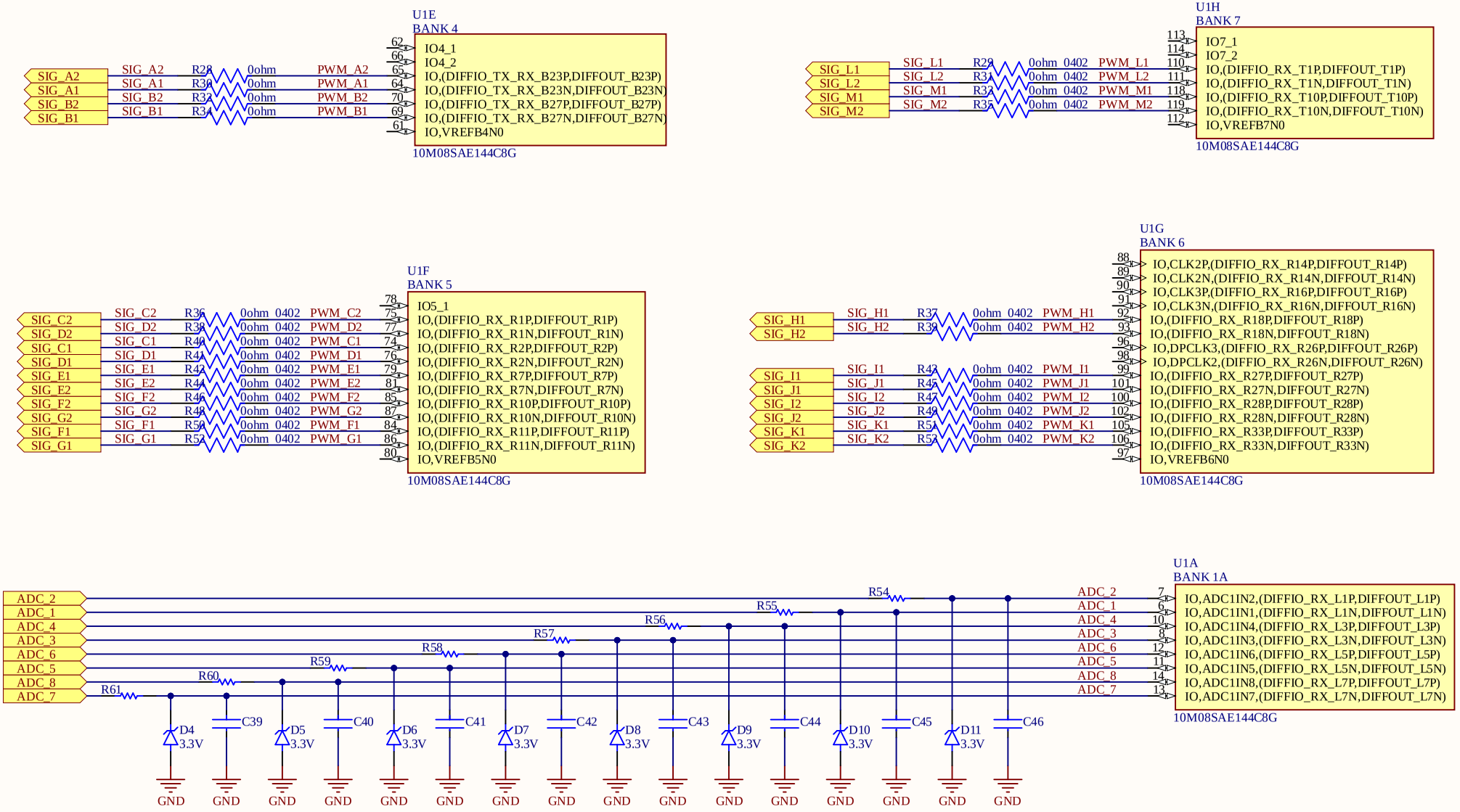
- **Sheet 1:** Contains the JTAG and power connector, the LDO, and all components related to powering the FPGA.
- **Sheet 2:** Contains the clock, the LEDs, some PWM signals, and connections to configure the JTAG protocol.
- **Sheet 3:** Contains most of the PWM signals, as well as the analog signals and their output filter.
- **Sheets 4 to 7:** Contain the buffer gates and the SMA connectors for the PWM signals.
- **Sheet 8:** Contains the buffers, SMA connectors and input filters of the analog signals.



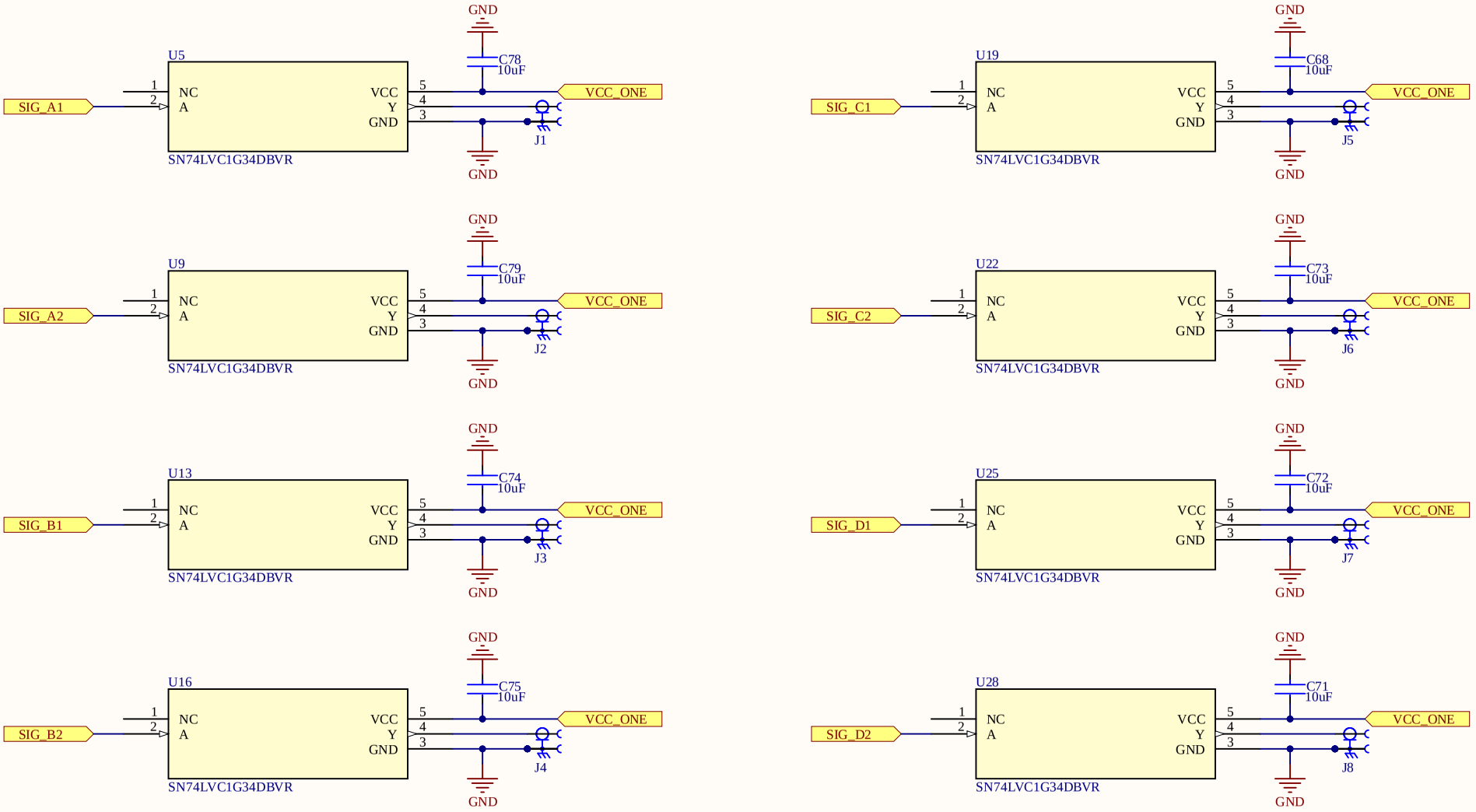
FPGA Controller for High Power Multi-MHz WPT Systems		
Date: June 2024	Power Section and JTAG Connector	Version: v2
Cornell University - Power Electronics Lab	Sheet 1 of 8	Drawn by: Miguel Alvarez Dominguez



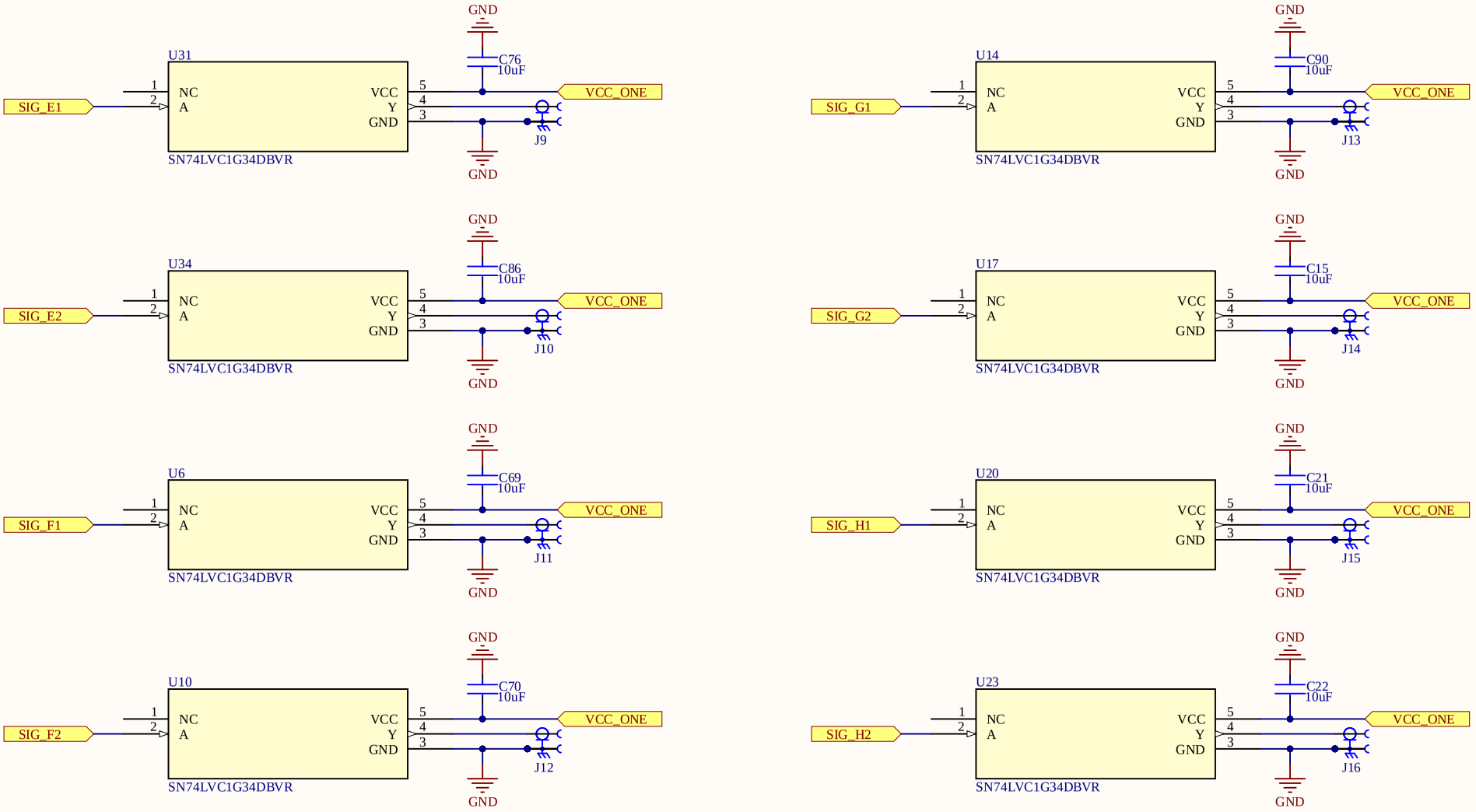
FPGA Controller for High Power Multi-MHz WPT Systems		
Date: June 2024	Oscillator and Configuration Section	Version: v2
Cornell University - Power Electronics Lab	Sheet 2 of 8	
	Drawn by: Miguel Alvarez Dominguez	



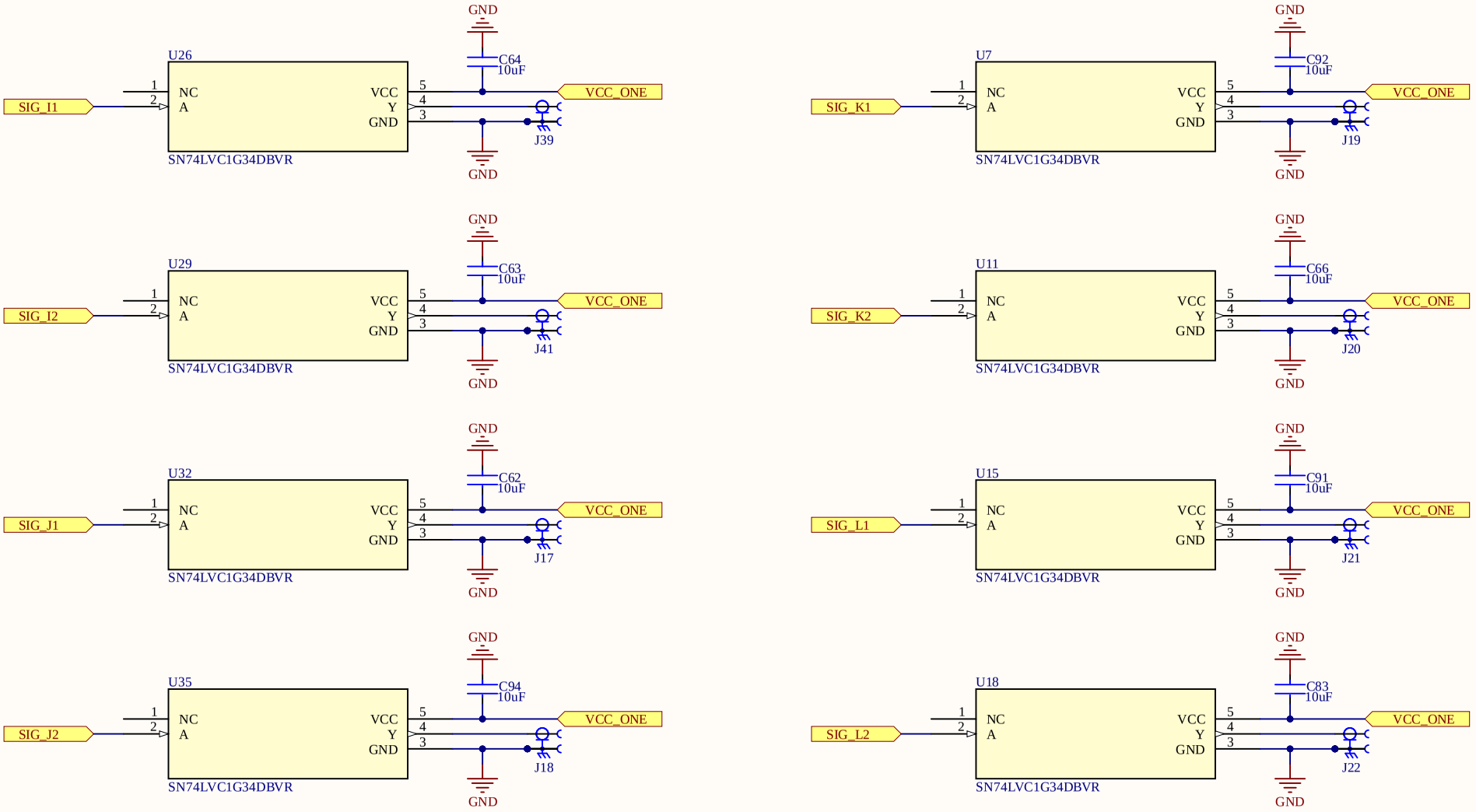
FPGA Controller for High Power Multi-MHz WPT Systems		
Date: June 2024	PWM and Analog Signals	Version: v2
Cornell University - Power Electronics Lab	Sheet 3 of 8	
	Drawn by: Miguel Alvarez Dominguez	



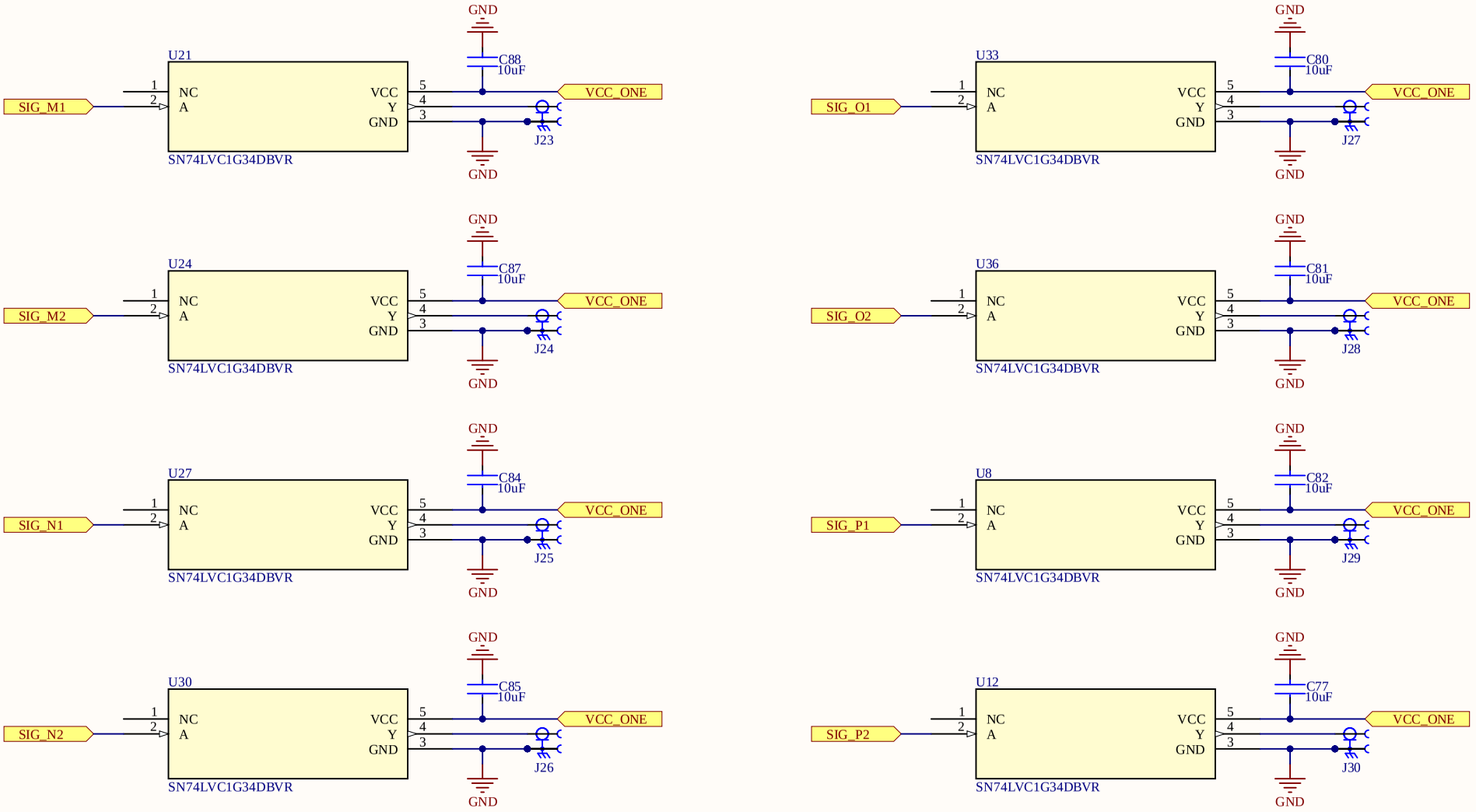
FPGA Controller for High Power Multi-MHz WPT Systems		
Date: June 2024	Buffer Gates and SMA Connectors (A)	Version: v2
Cornell University - Power Electronics Lab	Sheet 4 of 8	
	Drawn by: Miguel Alvarez Dominguez	



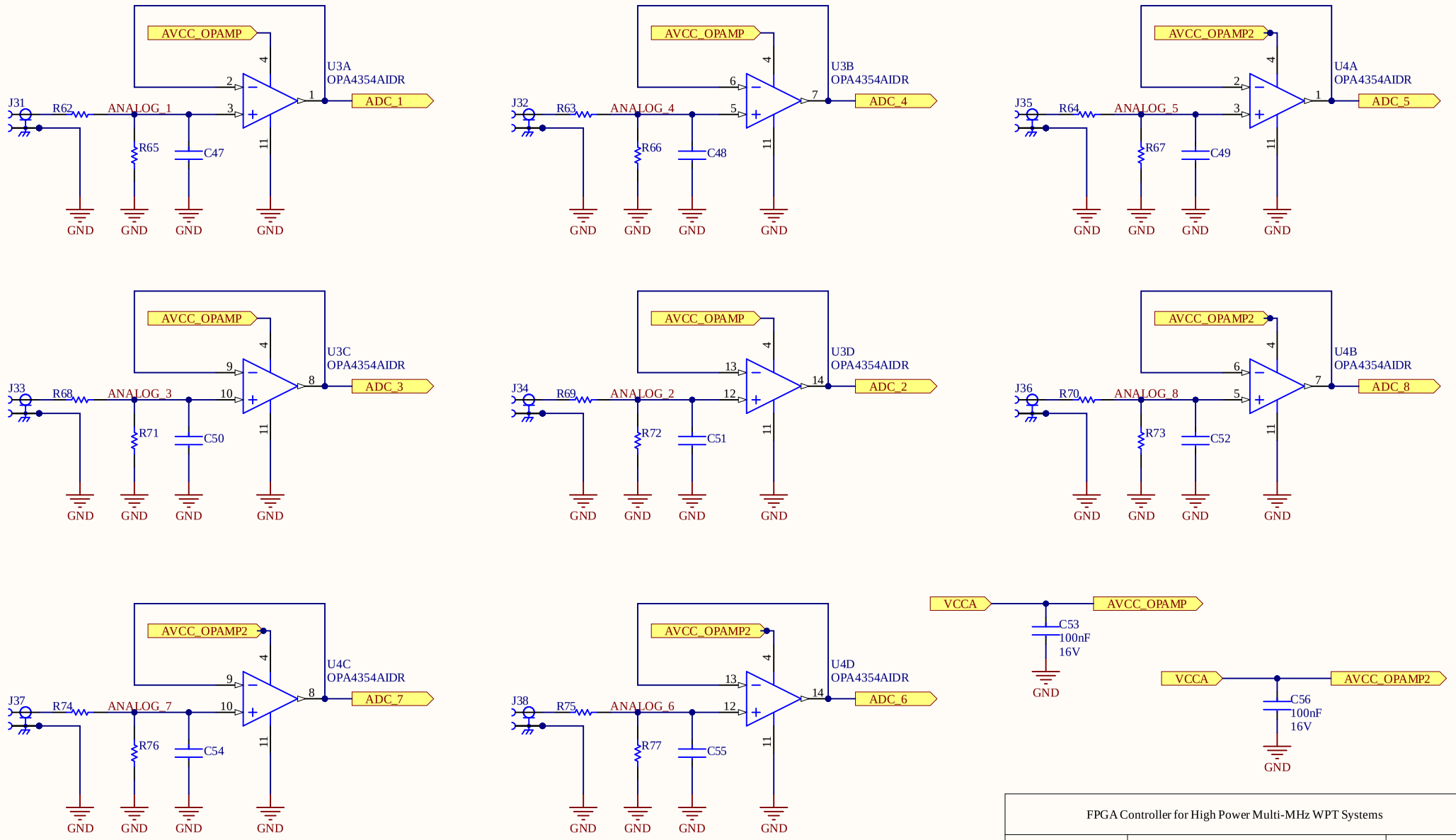
FPGA Controller for High Power Multi-MHz WPT Systems		
Date: June 2024	Buffer Gates and SMA Connectors (B)	Version: v2
Cornell University - Power Electronics Lab	Sheet 5 of 8	
	Drawn by: Miguel Alvarez Dominguez	



FPGA Controller for High Power Multi-MHz WPT Systems		
Date: June 2024	Buffer Gates and SMA Connectors (C)	Version: v2
Cornell University - Power Electronics Lab	Sheet 6 of 8	
	Drawn by: Miguel Alvarez Dominguez	



FPGA Controller for High Power Multi-MHz WPT Systems		
Date: June 2024	Buffer Gates and SMA Connectors (D)	Version: v2
Cornell University - Power Electronics Lab	Sheet 7 of 8	
	Drawn by: Miguel Alvarez Dominguez	



FPGA Controller for High Power Multi-MHz WPT Systems		
Date: June 2024	Analog Section Buffers	Version: v2
Cornell University - Power Electronics Lab	Sheet 8 of 8	
	Drawn by: Miguel Alvarez Dominguez	

Appendix D

PCB Layers Design

D.1. Top Layer

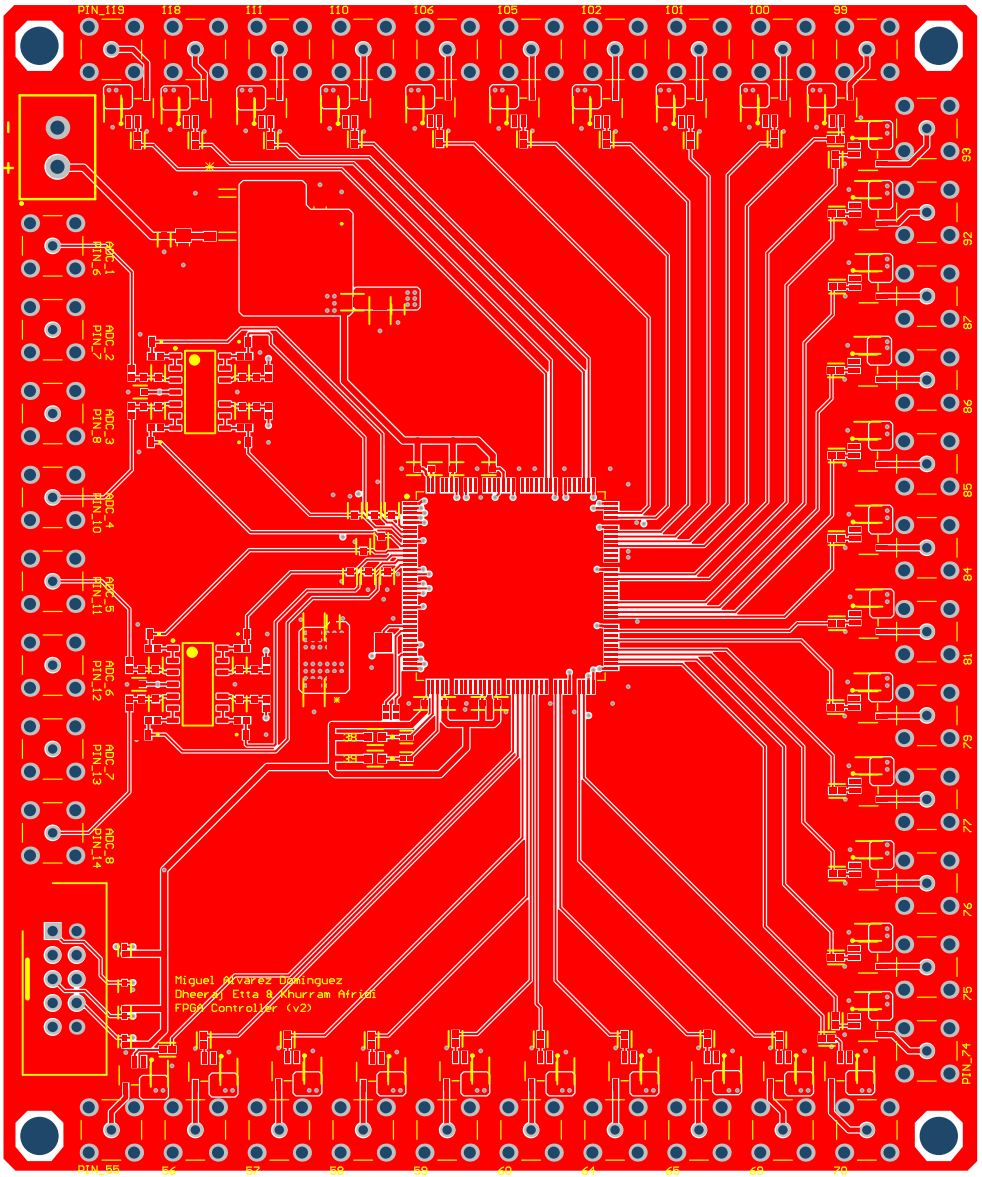


Figure 35. Top Layer of the PCB.

D.2. Second Layer

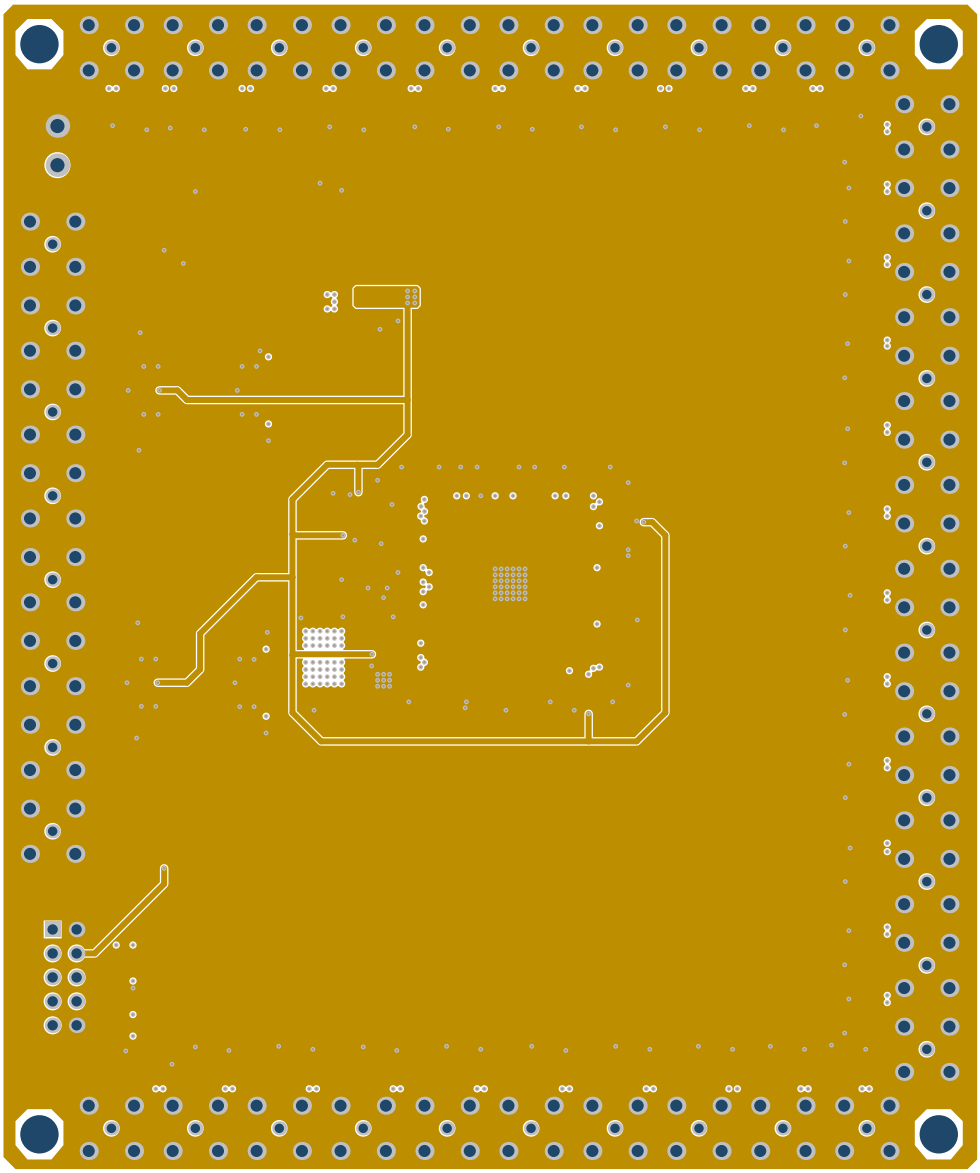


Figure 36. Second Layer of the PCB.

D.3. Third Layer

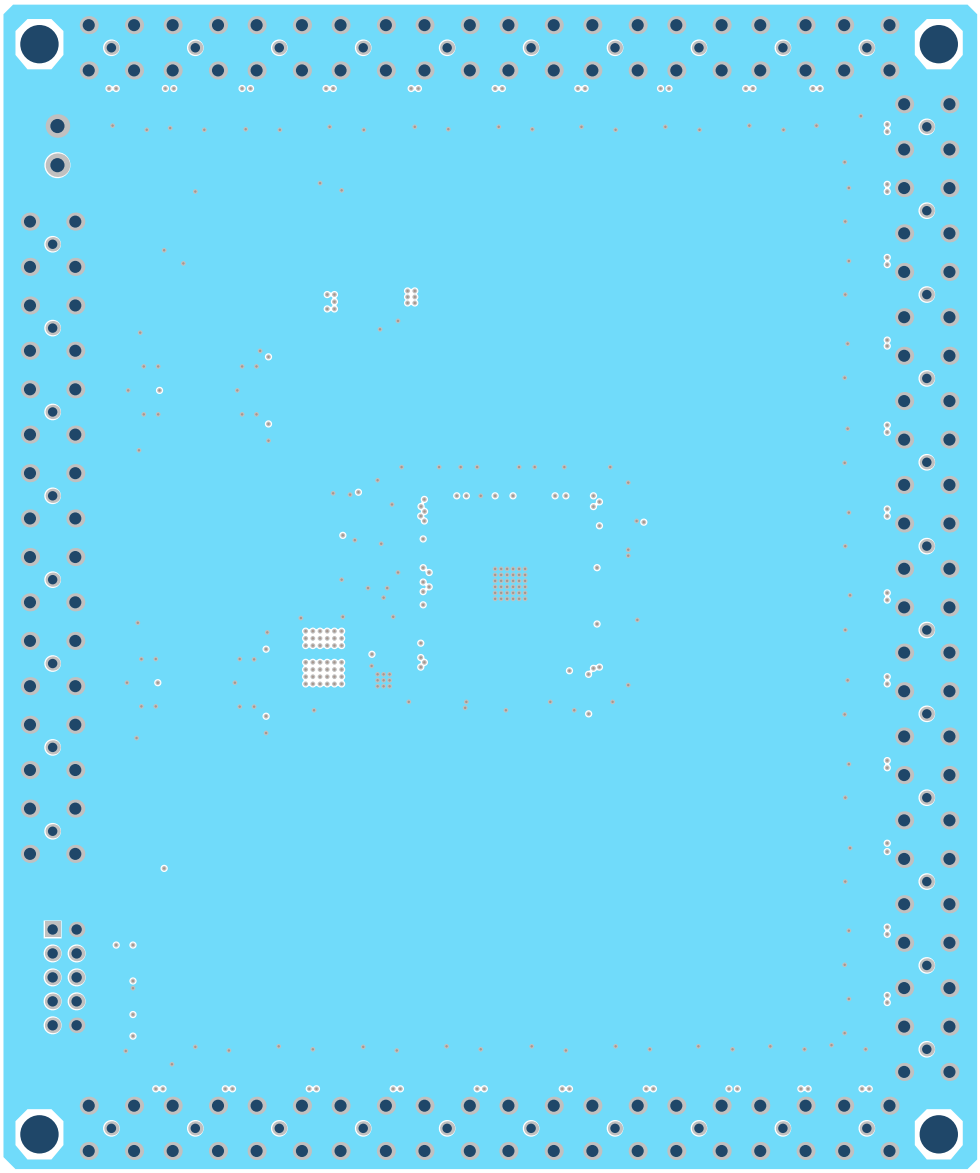


Figure 37. Third Layer of the PCB.

D.4. Bottom Layer

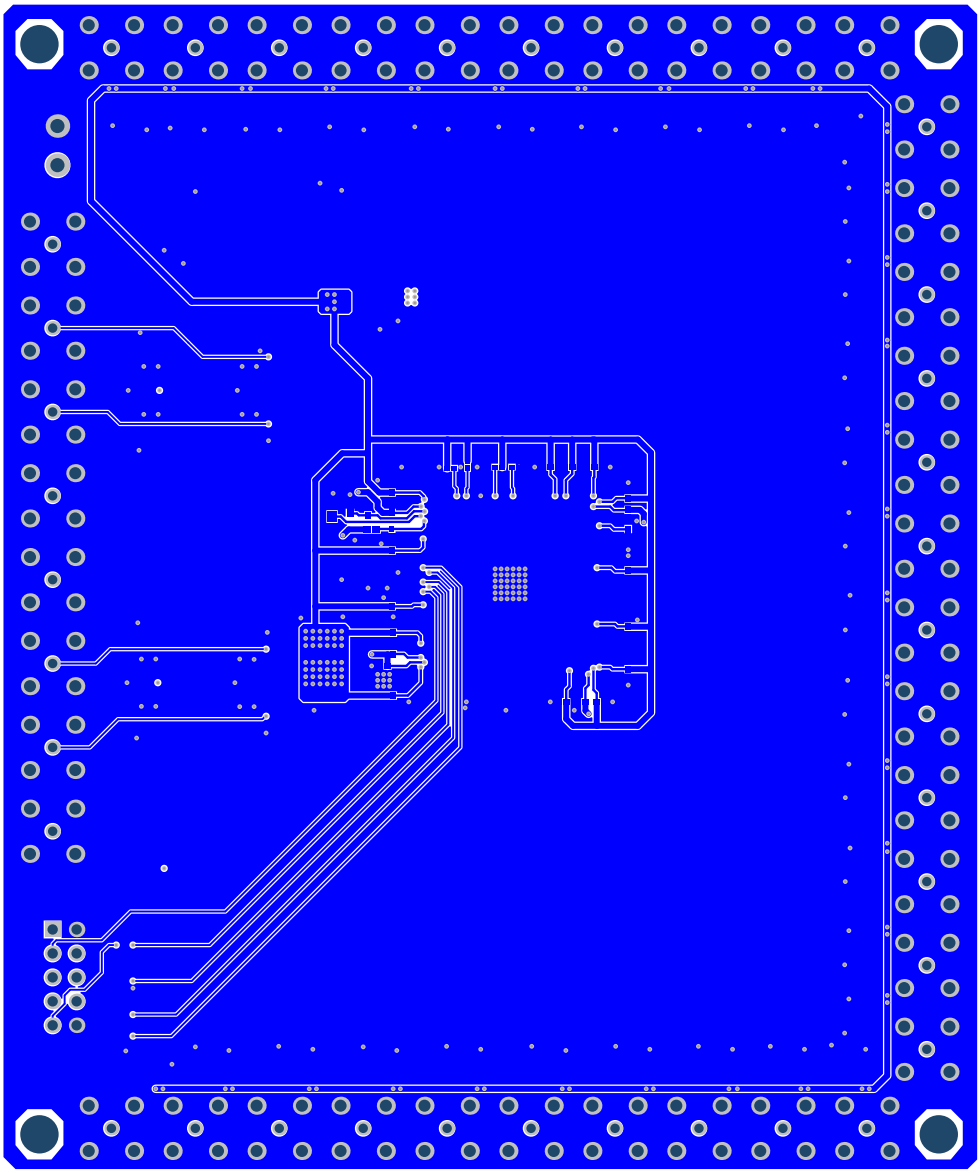


Figure 38. Bottom Layer of the PCB.