Detailed analysis and experimental results of the control system of a UPFC

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Abstract: The decoupled control of the power flow through a transmission line using a PWM-based Unified Power Flow Controller (UPFC) is explained. A dynamic model of a UPFC has been developed using the space-vector representation of instantaneous three-phase variables. The Park's transformation and the reference frame selected reduce the control of the real- and reactive-power flows to the control of the d- and q-axis currents, respectively. The proposed control scheme produces fast and decoupled response of the real- and the reactive-power flow through a transmission line. It also achieves tight control of the DC-link capacitor voltage through careful coordination between the control of the series and shunt compensators of the UPFC. A prototype has been built to illustrate the main contributions. The prototype includes a UPFC with 750 Hz switching frequency applied to a reduced model of a transmission line. Experimental results agree closely with the theoretical analysis.

1 Introduction

The Unified Power Flow Controller (UPFC) is the most comprehensive tool for real-time control of AC transmission systems. It can be used to control the transmitted real- and reactive-power flows through a transmission line thus optimising the power flow, improving the transient stability margins, damping power oscillations and providing voltage support. Previous research efforts have focused mainly on steady-state performance and the description of several applications [1]. Also, some details of the required control loops are explained in [2] and [3]. However, experimental results show cross-couplings between the real- and the reactive-power control systems. Furthermore, during transients the voltage of the DC-link capacitor varies significantly. This paper focuses on the detailed analysis of the implementation of the controller of the UPFC, based on the control system already proposed in [4] and [5].

First of all, the paper describes the dynamic model of a UPFC applied to a transmission line. Secondly, the implementation of the control algorithms is explained in detail. Thirdly, a laboratory prototype is described. The prototype includes a hardware model of a transmission line with per-unit values of its parameters similar to those of a 400 kV and 1500 MVA rating existing line. The switching frequency of the power electronic converters has been limited to 750 Hz to obtain a realistic prototype for high-power applications. Finally, the experimental results illustrate the behaviour of the control system.

2 Configuration and modelling of a UPFC

Fig. 1*a* depicts a UPFC applied to a transmission line. It consists of a series voltage-source inverter (I2), a shunt voltage-source inverter (I1), two transformers (T2 and T1) and the connection filter. Note that the two inverters share the same DC-link capacitor. Fig. 1*b* depicts a simplified model of the system. The series compensator (series inverter plus series transformer) has been modelled as a fully-controllable voltage source (e) and it controls the real and the reactive power flow through the transmission line. The shunt compensator (shunt inverter, shunt transformer and connection filter) has been modelled as a fully controllable voltage source (eP) with a connection impedance (L_p and r_p) including the leakage of the shunt transformer. The shunt

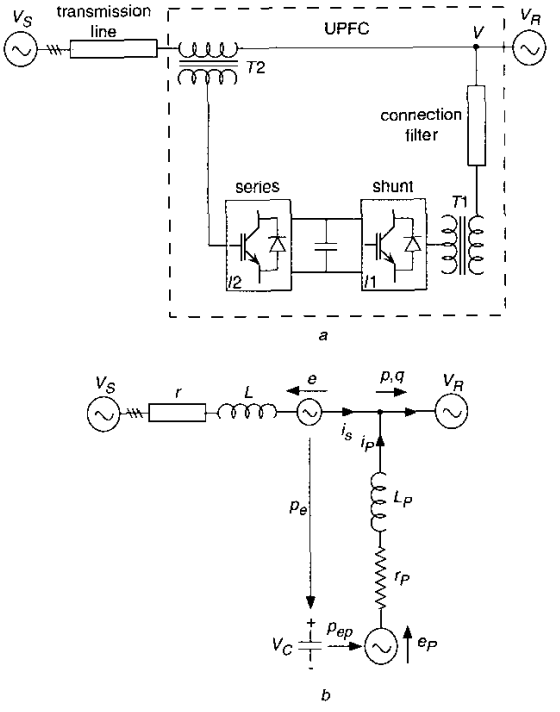

Fig. 1 *a Configuration of a UPFC, b Simplified model*

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compensator exchanges real power with the power system in order to maintain the energy stored in the DC-link capacitor. The shunt compensator may also exchange reactive power with the power system [6] but this is not explored here. Finally, voltages V_S and V_R model the sending-end and the receiving-end voltages respectively, and L and r model the transmission line including the leakage of the series transformer.

The instantaneous three-phase variables of the UPFC can be described by dq-components using Park's transformation [7] as follows:

$$\frac{d}{dt}\begin{bmatrix} i_{Sd} \\ i_{Sq} \end{bmatrix} = \begin{bmatrix} -\frac{r}{L} & \omega \\ -\omega & -\frac{r}{L} \end{bmatrix} \begin{bmatrix} i_{Sd} \\ i_{Sq} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} V_{Sd} - e_d - V_{Rd} \\ V_{Sq} - e_q \end{bmatrix} \quad (1)$$

$$\frac{d}{dt}\begin{bmatrix} i_{Pd} \\ i_{Pq} \end{bmatrix} = \begin{bmatrix} -\frac{r_p}{L_p} & \omega \\ -\omega & -\frac{r_p}{L_p} \end{bmatrix} \begin{bmatrix} i_{Pd} \\ i_{Pq} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_p} & 0 \\ 0 & \frac{1}{L_p} \end{bmatrix} \begin{bmatrix} e_{Pd} - V_{Rd} \\ e_{Pq} \end{bmatrix} \quad (2)$$

where ω is the angular speed of the reference frame used. All pairs in dq-axes are complex numbers or space vectors. Equations (1) and (2) model the series and shunt compensators respectively.

The Park's transformation selected here keeps invariant the instantaneous power expression and the d-axis lays on the space vector of the receiving-end voltage. Hence, $\mathbf{V}_{Rdq} = V_{Rd} + jV_{Rq} = V_{Rd}$. Using the definition of instantaneous reactive power [8] the real power (p) and instantaneous reactive power (q) transmitted to the receiving end are:

$$p = V_{Rd}i_{Sd} + V_{Rq}i_{Sq} = V_{Rd}i_{Sd} \quad (3)$$

$$q = -V_{Rd}i_{Sq} + V_{Rq}i_{Sd} = -V_{Rd}i_{Sq} \quad (4)$$

Hence, the p and q flows in the transmission line are proportional to i_{Sd} and i_{Sq} respectively, and the control of p and q reduce to the control of d- and q-axes currents.

The model of the DC-link capacitor may be derived from the equation of the energy stored in a capacitor ($e_C = 1/2Cv_C^2$). Hence:

$$\frac{d(v_C^2)}{dt} = \frac{2}{C}(p_e - p_{ep}) \quad (5)$$

where:

$$p_e = e_d i_{Sd} + e_q i_{Sq} \quad (6)$$

$$p_{ep} = e_{Pd} i_{Pd} + e_{Pq} i_{Pq} \quad (7)$$

and where p_e is the real power absorbed from the AC system by the series voltage source (e) and p_{ep} is the real power injected by the shunt voltage source into the AC system. Therefore, if $p_e > p_{ep}$, v_C increases, and if $p_e < p_{ep}$, v_C decreases. Equation (5) is good for control purposes because it is a linear model of the DC-link capacitor, where p_e and p_{ep} are the inputs and v_C^2 is the state variable.

Finally, if the shunt compensator does not exchange reactive power and neglecting losses (7) may be simplified as follows [6]:

$$P_{ep} \cong V_{Rd} i_{Pd} \quad (8)$$

and the control of p_{ep} reduces to the control of i_{Pd}. Typically, the shunt voltage is significantly greater than the series voltage. Therefore, the current of the shunt compensator is negligible compared with the current of the series compensator.

3 Design and implementation of digital controllers for the UPFC

Fig. 2 depicts the control system of the UPFC based on (1), (2) and (5) (see [4]). The main loop is the control of the series compensator. It controls i_{Sd} and i_{Sq} (control of the receiving-end power) and all the other loops are subordinated to it. The series voltage source may absorb real power (p_e) from the electric system. The shunt compensator supplies this power to the electric system, so that v_C remains constant.

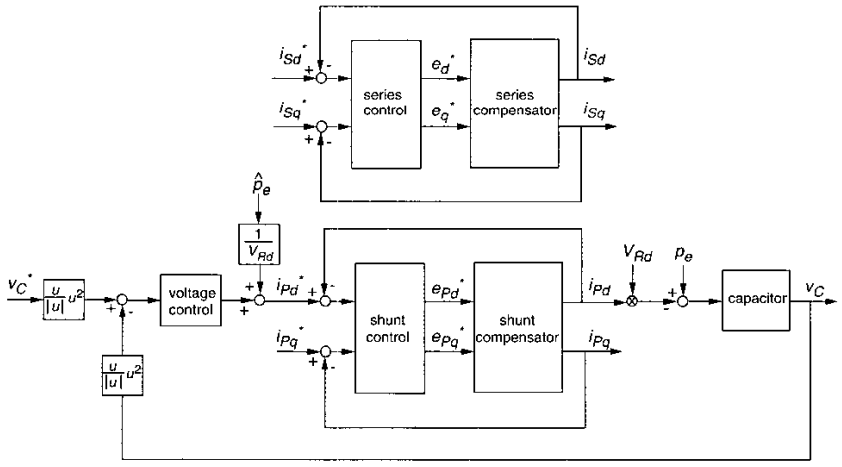

Fig. 2 *UPFC control system. Superscript * means reference value and $\hat{p}_e$ is the estimation of p_e.*

3.1 Series compensator

The receiving-end system frequency (ω) can be considered to be constant and the dynamic system in (1) is linear. Therefore, an exact discrete-time model can be obtained in order to consider the digital implementation of the control algorithms. The UPFC must control i_{Sd} and i_{Sq} independently but the dynamics of the two axes are coupled in (1). It is shown in [4] that further coupling terms appear in the system discrete-time model and that decoupled control is

still possible using state feedback. Details of the digital-controller design of the series compensator are given in [5]. Here, a self-contained summary is presented.

Assuming that inputs are set through a zero-order hold, the discrete-time incremental model of (1) can be written as:

$$\underbrace{\begin{bmatrix} i_{Sd}(k+1) \\ i_{Sq}(k+1) \end{bmatrix}}_{\mathbf{i}_{Sdq}(k+1)} = \underbrace{\begin{bmatrix} \phi_1 & \phi_2 \\ -\phi_2 & \phi_1 \end{bmatrix}}_{\boldsymbol{\Phi}} \underbrace{\begin{bmatrix} i_{Sd}(k) \\ i_{Sq}(k) \end{bmatrix}}_{\mathbf{i}_{Sdq}(k)} + \underbrace{\begin{bmatrix} \gamma_1 & \gamma_2 \\ -\gamma_2 & \gamma_1 \end{bmatrix}}_{\boldsymbol{\Gamma}} \underbrace{\begin{bmatrix} e_d(k) \\ e_q(k) \end{bmatrix}}_{\mathbf{e}_{dq}(k)} \tag{9}$$

and, with [9]:

$$\boldsymbol{\Phi} = e^{\mathbf{A}t_s} \text{ and } \boldsymbol{\Gamma} = \left(\int_0^{t_s} e^{\mathbf{A}\eta} d_\eta \right) \mathbf{B} \tag{10}$$

where t_s is the sampling interval.

Note that the system inputs in (9) $\mathbf{e}_{dq}(k)$ represent the control action of the series inverter upon the line at time k. The controller should calculate it from measurements at time k (feedback). However, even with modern microprocessors it is conceded that there will be at least a one-sample-interval delay between the time when measurements are taken and the time when the inverter output can be set. This is certainly the case in the prototype (see Section 4). Therefore, the controller output calculated at time k (called $\mathbf{e}^*_{dq}(k)$ in Fig. 2) is the control action applied by the series inverter at time $k+1$ ($\mathbf{e}_{dq}(k+1)$).

$$\begin{bmatrix} i_{Sd}(k+1) \\ i_{Sq}(k+1) \end{bmatrix} = \begin{bmatrix} \phi_1 & \phi_2 \\ -\phi_2 & \phi_1 \end{bmatrix} \begin{bmatrix} i_{Sd}(k) \\ i_{Sq}(k) \end{bmatrix} + \begin{bmatrix} \gamma_1 & \gamma_2 \\ -\gamma_2 & \gamma_1 \end{bmatrix} \begin{bmatrix} e^*_d(k-1) \\ e^*_q(k-1) \end{bmatrix} \tag{11}$$

Equation (11) can be transformed into two independent single-input-single-output control systems:

$$\begin{bmatrix} i_{Sd}(k+1) \\ i_{Sq}(k+1) \end{bmatrix} = \begin{bmatrix} \phi_1 & 0 \\ 0 & \phi_1 \end{bmatrix} \begin{bmatrix} i_{Sd}(k) \\ i_{Sq}(k) \end{bmatrix} + \begin{bmatrix} u_d(k-1) \\ u_q(k-1) \end{bmatrix} \tag{12}$$

with

$$\begin{bmatrix} e^*_d(k) \\ e^*_q(k) \end{bmatrix} = -\boldsymbol{\Gamma}^{-1} \begin{bmatrix} 0 & \phi_2 \\ -\phi_2 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{Sd}(k+1) \\ \hat{i}_{Sq}(k+1) \end{bmatrix} + \boldsymbol{\Gamma}^{-1} \begin{bmatrix} u_d(k) \\ u_q(k) \end{bmatrix} \tag{13}$$

Note that the calculation of the series inverter output voltage done by the controller with (13) requires the use of the values of the state variables in the future ($\hat{i}_{Sd}(k+1)$ and $\hat{i}_{Sq}(k+1)$) and that they have therefore to be estimated. In addition, (12) does not have the standard form of a discrete-time system ($x(k+1) = \Phi\mathbf{x}(k) + \Gamma\mathbf{u}(k)$). The second problem can be easily solved by adding the delayed system inputs ($u_d(k-1)$, $u_q(k-1)$ in (12) as two new state variables ($x_{Rd}(k)$, $x_{Rq}(k)$) [9]. Hence, for the d-axis system in (12), it is possible to write:

$$\begin{bmatrix} i_{Sd}(k+1) \\ x_{Rd}(k+1) \end{bmatrix} = \begin{bmatrix} \phi_1 & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_{Sd}(k) \\ x_{Rd}(k) \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} u_d(k) \tag{14}$$

and similarly for the q-axis.

The estimation of $\hat{i}_{Sd}(k+1)$ and $\hat{i}_{Sq}(k+1)$ can be carried out in three different ways. First, one can assume that $\hat{i}_{Sd}(k+1) = i_{Sd}(k)$ and $\hat{i}_{Sq}(k+1) = i_{Sq}(k)$. This will have no computational cost but it will not achieve perfect decoupling. The results will be acceptable if the sampling interval is small compared to the closed-loop system time constants. Second, the estimation can be done using a simulator with (14) and its companion for the q-axis. The simulator will only use the system inputs ($u_d(k)$ and $u_q(k)$) to calculate the estimated state variables recursively. Finally, the estimation can be done using (14) and its companion for the q-axis as a predictor for $k+1$ based on the inputs and measured state variables in k [10]. The second and the latter solutions have a similar computational cost but the latter is preferable if the noise when measuring the state variables is not very significant. The latter solution has been used to obtain the results discussed later.

A proportional state-feedback controller can be easily designed for (14) to place the closed-loop system poles [9]. Most Computer-Aided-Design programs for control system design include several algorithms for pole placement (see [11], for example).

3.2 Design of a decoupled proportional+integral controller

The controllers should use the integral of the error to guarantee zero error in steady state for the state variables. The discrete-time integral of the error in the d-axis (real power) can be written as [9]:

$$x_{Id}(k+1) = x_{Id}(k) + i^*_{Sd}(k) - i_{Sd}(k) \tag{15}$$

where i^*_{Sd} is the reference value for the d-axis current (real power).

A new state variable x_{Id} can be included in (14) yielding:

$$\begin{bmatrix} i_{Sd}(k+1) \\ x_{Id}(k+1) \\ x_{Rd}(k+1) \end{bmatrix} = \begin{bmatrix} \phi_1 & 0 & 1 \\ -1 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{Sd}(k) \\ x_{Id}(k) \\ x_{Rd}(k) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} u_d(k) + \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} i^*_{Sd}(k) \tag{16}$$

Similarly, one can use the q-axis state-variable system.

Clearly, a proportional state-feedback controller for the system in (16) gives a **P+I** controller for the d-axis:

$$u_d(k) = -\underbrace{\begin{bmatrix} k_d & k_{Id} & k_{Rd} \end{bmatrix}}_{\mathbf{K}_d} \begin{bmatrix} i_{Sd}(k) \\ x_{Id}(k) \\ x_{Rd}(k) \end{bmatrix} \tag{17}$$

A similar approach can be used for the q-axis.

Note that d- and q-axes have been treated independently thanks to the decoupling structure proposed for the controller. Summarising:

$$\begin{bmatrix} e^*_d(k) \\ e^*_q(k) \end{bmatrix} = \underbrace{-\boldsymbol{\Gamma}^{-1} \begin{bmatrix} k_d & 0 & k_{Id} & k_{Rd} & 0 & \phi_2 & 0 & 0 \\ 0 & -\phi_2 & 0 & 0 & k_d & 0 & k_{Iq} & k_{Rq} \end{bmatrix}}_{\mathbf{K}_s} \times \begin{bmatrix} i_{Sd}(k) \\ \hat{i}_{Sd}(k+1) \\ x_{Id}(k) \\ x_{Rd}(k) \\ i_{Sq}(k) \\ \hat{i}_{Sq}(k+1) \\ x_{Iq}(k) \\ x_{Rq}(k) \end{bmatrix} \tag{18}$$

3.3 Shunt-compensator controller

The analysis of the shunt-compensator controller is similar to the analysis of the series-compensator controller. Therefore, the final result is presented directly:

$$\begin{bmatrix} e^*_{Pd}(k) \\ e^*_{Pq}(k) \end{bmatrix} = \underbrace{-\Gamma_P^{-1}\begin{bmatrix} k_{Pd} & 0 & k_{Pid} & k_{PRd} & 0 & \phi_{P2} & 0 & 0 \\ 0 & -\phi_{P2} & 0 & 0 & k_{Pd} & 0 & k_{Piq} & k_{PRq} \end{bmatrix}}_{\mathbf{K}_p} \times \begin{bmatrix} i_{Pd}(k) \\ \hat{i}_{Pd}(k+1) \\ x_{Pid}(k) \\ x_{PRd}(k) \\ i_{Pq}(k) \\ \hat{i}_{Pq}(k+1) \\ x_{Piq}(k) \\ x_{PRq}(k) \end{bmatrix} \quad (19)$$

Equations (18) and (19) show the exact implementation of the digital controllers for the d- and q-axis in the prototype.

In steady state, $p_e = p_{ep}$ and v_C remains constant (see (5)). However, during transients, p_e varies. The feed-forward term of the capacitor voltage controller ($\hat{p}_e$ in Fig. 2) modifies the reference of the real power for the shunt compensator to restore the equilibrium between p_e and p_{ep}. To implement the feed-forward it is necessary to estimate p_e. Due to the harmonic contents of the series voltage source ($\mathbf{e}_{dq}$), p_e is better estimated using the reference voltage ($\mathbf{e}^*_{dq}$) and the measurement of $\mathbf{i}_{Sdq}$.

$$\hat{p}_e(k) = i_{Sd}(k)e^*_d(k-1) + i_{Sq}(k)e^*_q(k-1) \quad (20)$$

Finally, the feedback of v_C (see Fig. 2) eliminates the DC voltage variations due to the errors in the estimation, errors in the compensation of the shunt compensator delay, losses in the connection impedance and switching inverter losses.

4 Prototype details

A laboratory prototype has been built to illustrate the performance of the UPFC control system. An overview of the prototype is shown in Fig. 3 and details of the control hardware are depicted in Fig. 4. The parameters of the prototype are in Table 1 and its main characteristics are:

- The prototype includes a hardware model of a transmission line with per-unit parameter values similar to those of a 400 kV and 1500 MVA rating transmission line. The hardware model base voltage is 380 V and the base power is 15 kVA.

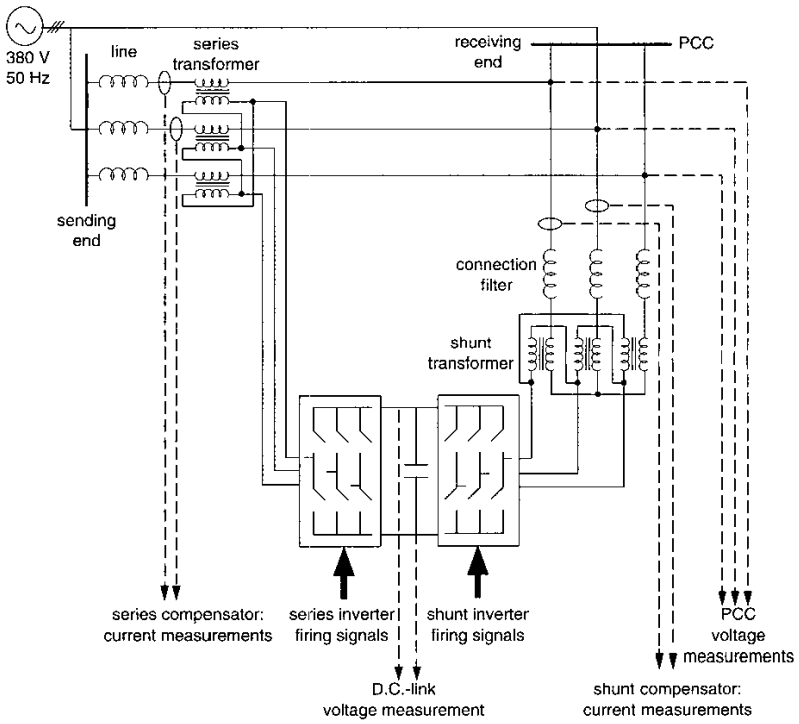

Fig. 3 *Overview of the UPFC hardware prototype*

3.4 Capacitor-voltage controller

The capacitor-voltage control is important for the UPFC control system. If the capacitor voltage variations are bounded the UPFC voltage sources are independent of the capacitor voltage. This can be achieved, by increasing the value of the capacitor, but it is expensive. The best alternative is to achieve good transient performance of this controller.

- The receiving-end and the sending-end were physically the same point in the prototype (called PCC in Fig. 3). Therefore, there is no power flow between them when the UPFC is at rest.
- The system frequency is 50 Hz.
- The series transformer of the UPFC has been built with three single-phase transformers (380/35 V each). The

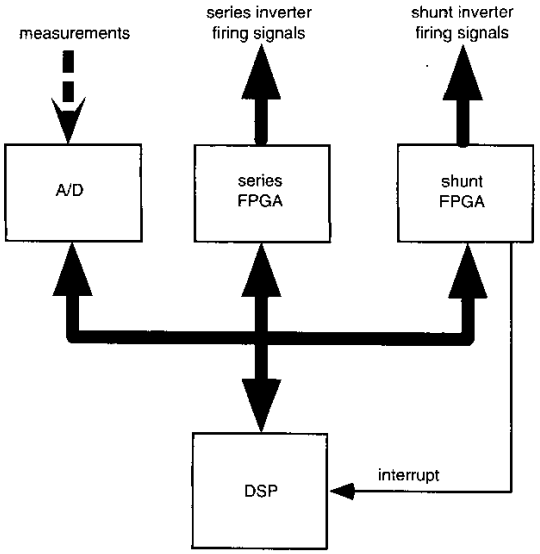

Fig. 4 *Details of the control hardware for the UPFC prototype*

Table 1: Characteristic of the prototype

Parameter	Base	Nominal value	Per-unit value
S	15 kVA	15 kVA	1 p.u.
V_S	380 V	380 V	1 p.u.
V_R	380 V	380 V	1 p.u.
L	9.6267 Ω	4.2 mHr ($X = 1.3195\,\Omega$)	0.4363 ms ($X_P = 0.1371$ p.u.)
r	9.6267 Ω	0.13195 Ω	0.01371 p.u.
L_p	9.6267 Ω	39 mHr ($X_P = 12.2522\,\Omega$)	4.05125 ms ($X_P = 1.2727$ p.u.)
r_p	9.6267 Ω	1.22522 Ω	0.12727 p.u.
V_C (d.c. side)	620 V	620 V	1 p.u.
C (d.c. side)	$0.03902\,\Omega^{-1}$	2.15 mF	55.0973 ms

primary is delta connected to the series inverter and the secondary is series connected to the transmission line.

- The series inverter was built with 1200 V, 100 A IGBT's.
- The shunt transformer has been built with three single-phase transformers (380/220 V each). The primary is delta

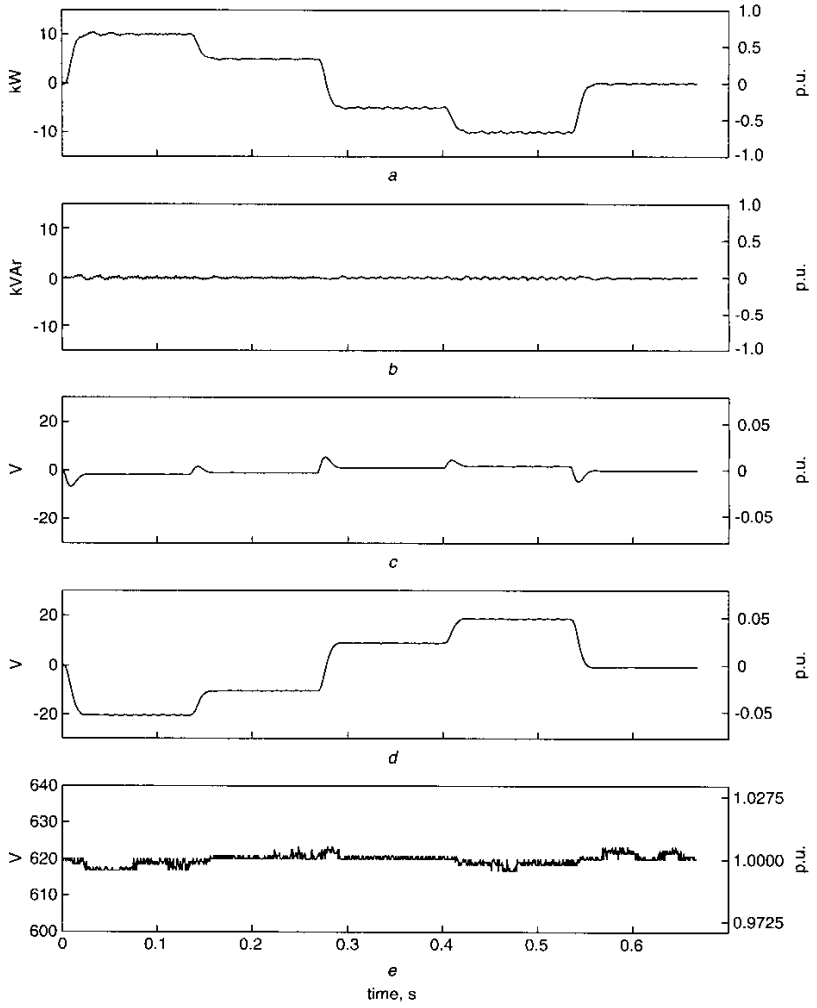

Fig. 5 *Step changes in the reference for p (10 kW, 5 kW, −5 kW, −10 kW and 0 kW) with constant references for q (0 kVAr) and v_C (620 V). From top to bottom: (a)p, (b)q, (c)e_d, (d)e_q and (e)v_C*

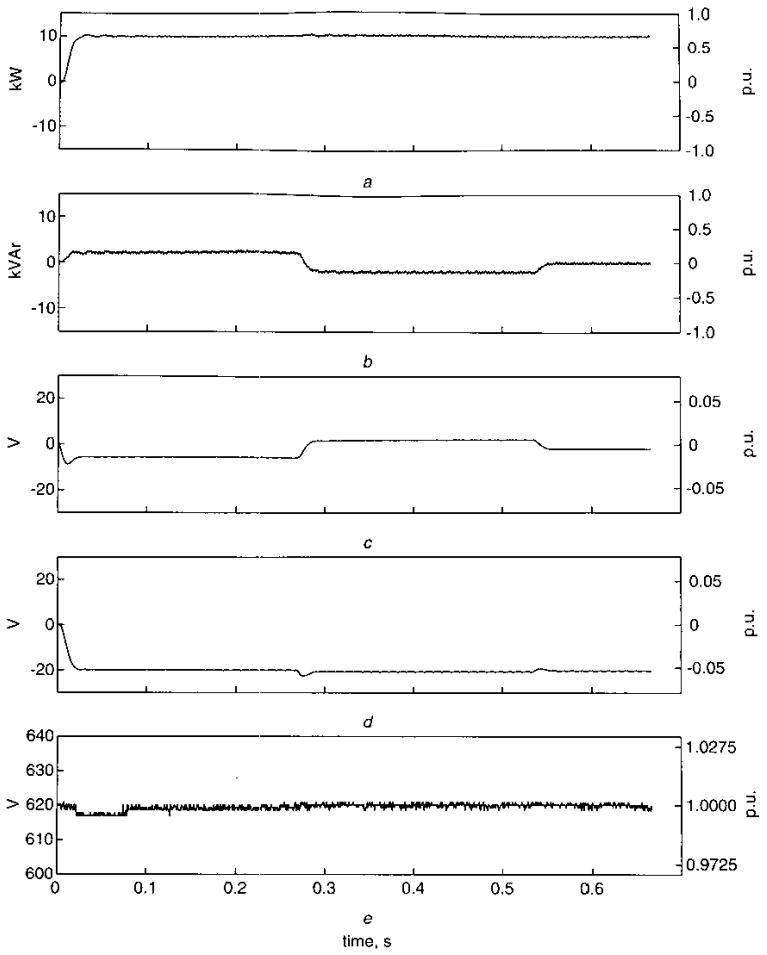

Fig. 6 *Response with step changes in the reference for q (2 kVAr, −2 kVAr and 0 kVAr) with constant references for p (10 kW) and v_C (620 V). From top to bottom: (a)p, (b)q, (c)e_d, (d)e_q and (e)v_C*

connected to the shunt inverter and the secondary is star connected to the electric system through a filter.

- A 15 kVA SEMIKRON inverter assembly was used for the shunt inverter.
- Space-Vector Modulation [12] with 750 Hz switching frequency has been used to control the voltage of each inverter. This is a realistic value for high-power applications.
- A TMS320C30 DSP placed on a commercial board from LSI (UK) has been used to implement the controller with 1.5 kHz sampling frequency.
- The controller implementation has been carried out with a commercial real-time operating system (SIMULINK real-time workshop RTW [13]). Appropriate software drivers had to be developed to handle all the control hardware (DSP board, A/D board, inverter-control board) from SIMULINK RTW.
- Current feedback has been done using hall-effect probes. Voltage feedback has been done using differential probes. The receiving-end voltage has to be measured to carry out Park's transformation. The capacitor voltage is measured for feedback control.

The heart of the controller is a 32-bit floating-point DSP. Feedback signals are measured using a 32-input-channel acquisition card with 12-bit analog-to-digital (A/D) converters. All the calculations, including the inverter switching times, are done by the DSP. The actual firing signals for the inverter switches are generated with a FPGA (Field Programmable Gate Array) for the series inverter and another one for the shunt inverter. The former contains three timers, each one controlling the switching time of a different inverter leg. The latter contains four timers. Three of these control the inverter and the other determines the sampling period for the system control algorithm.

The hardware described above works as follows. The shunt FPGA interrupts the DSP when the control sampling period finishes. This is the signal for the DSP to sample the necessary variables through the A/D card but it also re-starts the count of all timers in the FPGAs. Therefore, the numbers representing the required inverter switching times must be written on the FPGA before the end of the previous sampling period. After reading the feedback values, the DSP performs all the calculations of the control algorithm, including the space-vector PWM. Eventually, the DSP writes on the FPGAs the new switching times for the inverter legs to be used during the next sampling period and waits until the shunt FPGA marks the end of the present sampling period. Note that in an inverter leg, one of the switches (and only one) is 'on'. When a leg timer finishes the count, it forces the inverter driver to change the inverter leg state. This action does not perturb the DSP calculations. When writing the switching times the DSP does not perturb the FPGA either.

Clearly, the control action is applied with one-sampling-period delay with respect to the moment when

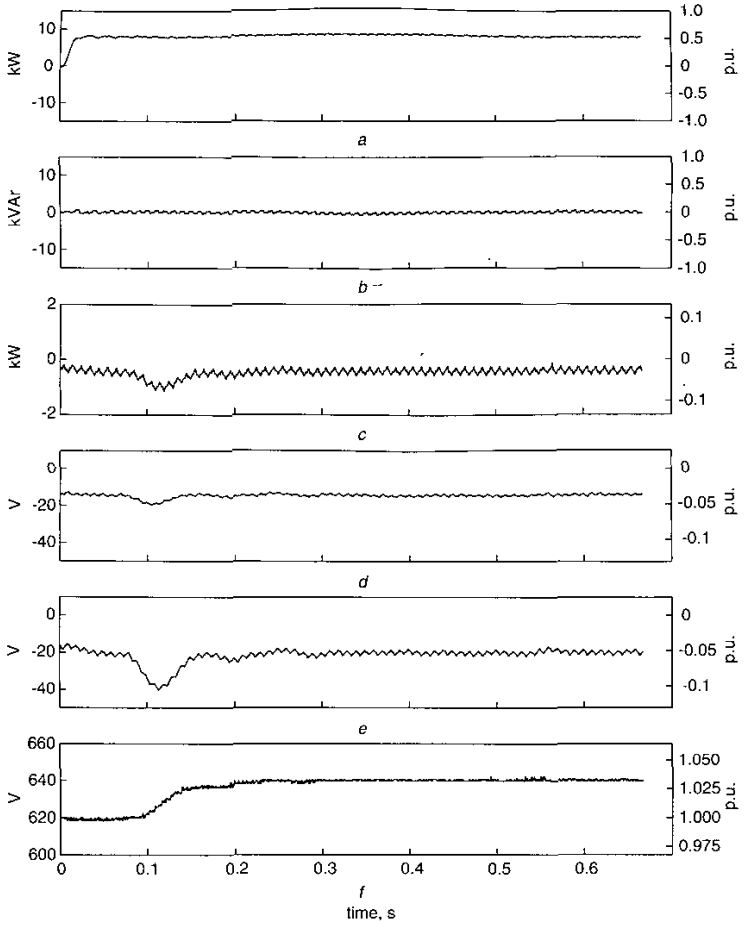

Fig. 7 *Response with a step change in the reference for v_c(620 V to 640 V) with constant references for p(7.5 kW) and q(0 kVAr). From top to bottom: (a)p, (b)q, (c)p_{cp}, (d)e_{pd}, (e)e_{pq} and (f)v_C*

measurements are taken. The implications of this for the control algorithm are explained above in Section 3.1.

5 Experimental results

The experimental results show the performance of the UPFC control system. All figures in this Section have been drawn using data (voltages and currents) sampled with an oscilloscope. Real and reactive power have been calculated from current and voltage measurements at the receiving-end while the capacitor voltage has been measured directly. For simplicity, the inverter voltages (d and q) calculated by the controllers have been plotted instead of the actual applied voltages. Note that the inverters achieve those voltages closely, and that any errors are corrected by the closed-loop control.

Fig. 5 shows the response with step changes in the reference for p and constant references for q and v_C. The real power (p) follows its reference closely with no cross-coupling with the instantaneous reactive power (q). The 5% settling time is less than 25 ms. The capacitor voltage variation is less than 0.5% and is in the order of the variations due to the switching frequency. Similar results are obtained when testing step changes in the reference for q (see Fig. 6)

Finally, Fig. 7 shows the response with step change in the reference for v_C and constant references for p and q. The 5% settling time is less than 150 ms and during the transient p and q remain constants. Therefore, it is possible to change v_C with no cross-coupling with p and q. A choice of the best operating point for the inverters is thus allowed.

6 Conclusions

This paper has shown that fast and decoupled control of the real- and the reactive-power flow through a transmission line is possible using a UPFC with reasonably low inverter switching frequency. Real- and instantaneous reactive-power control is equivalent to d- and q-axis current control using a Park's transformation based on a referenced frame fixed to the receiving-end voltage. The controller design must take into account the discrete-time implementation in a microprocessor if perfect decoupling is required. A one-step-ahead estimator may be necessary to maintain decoupling when there is a significant delay in calculating the control actions. For design purposes, the controller can be seen as a proportional state-feedback control law even when integral actions are required to ensure zero error in steady state. Furthermore, the control of the DC-link capacitor voltage ensures constant voltage during p and q transients. This is very important when capacitor size is a key issue in the design of the UPFC.

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