ESCUELA TÉCNICA SUPERIOR DE INGENIERÍA (ICAI)

Grado en Ingeniería en Tecnologías Industriales

Development of a VSC-based low voltage STATCOM system

Autor
Emilio Pérez del Río

Dirigido por
Jorge Suárez Porras

Madrid
Agosto 2023

Declaro, bajo mi responsabilidad, que el Proyecto presentado con el título

Development of a VSC-based low voltage

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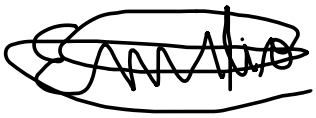

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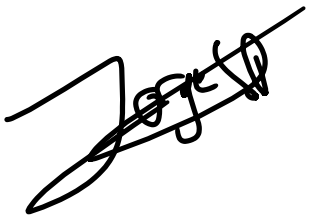

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DESARROLLO DE UN SISTEMA STATCOM DE BAJA TENSIÓN BASADO EN CONVERTIDOR CC-CA

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Entidad Colaboradora: ICAI – Universidad Pontificia Comillas

RESUMEN DEL PROYECTO

En este proyecto se ha utilizado un convertidor trifásico de corriente continua a corriente alterna conectado a la red eléctrica para corregir su factor de potencia.

Palabras clave: STATCOM, VSC, control de potencia reactiva, corrección del factor de potencia, integración con la red.

1. Introducción

La creciente cuota del mercado energético ocupada por las energías renovables está desplazando a las centrales eléctricas tradicionales y a los grandes generadores síncronos que emplean [1]. Una de las funciones realizadas por estos generadores es corregir el factor de potencia de la red, función que ahora tendrán que realizar conversores CC-CA, entre otros dispositivos [2]. Este documento resume el proceso de diseño y desarrollo de un sistema de compensador síncrono estático (STATCOM, del inglés *STATic synchronous COMPensator*) basado en un sistema convertidor de fuente de tensión trifásico (VSC, del inglés *Voltage Source Converter*) para proporcionar corrección del factor de potencia a una red, proporcionando una respuesta rápida y una inyección de armónicos mínima. En este resumen, primero se presenta el diseño de los elementos hardware y software. Después de eso, se muestra el diseño del sistema de control. Por último, se discuten los resultados de las simulaciones por ordenador y las pruebas del prototipo físico.

2. Definición del proyecto

El objetivo de este proyecto es diseñar un sistema STATCOM utilizando un convertidor de fuente de tensión trifásico que pueda responder a cambios en la demanda de potencia reactiva de la red eléctrica con la mayor velocidad posible, y evitando introducir un alto novel de armónicos en las corrientes de salida. Primero se simulará utilizando Matlab y Simulink, y después se construirá un prototipo en el laboratorio.

3. Descripción del sistema

La Ilustración 1 muestra el diagrama eléctrico del sistema, y en la Ilustración 2 se observa cómo este se desarrolló en forma de prototipo en el laboratorio. El convertidor carga su condensador del lado de continua utilizando la energía que le proporciona la red. Mediante una actuación apropiada sobre los transistores utilizando PWM, se pueden generar tensiones a la salida del convertidor que no estén en fase con las de la red, lo cual permite controlar las potencias activa y reactiva absorbidas por el aparato. Entre el convertidor y la red hay un filtro con inductancias (*L filter*) para reducir los armónicos en las corrientes de salida, una resistencia de precarga (*Startup resistance*)

y un transformador para adaptarse a la tensión de la red. Entre el transformador y la resistencia de precarga, se puede introducir una carga para que el convertidor compense su reactiva, o simplemente se puede demandar una generación de reactiva prescindiendo de la carga.

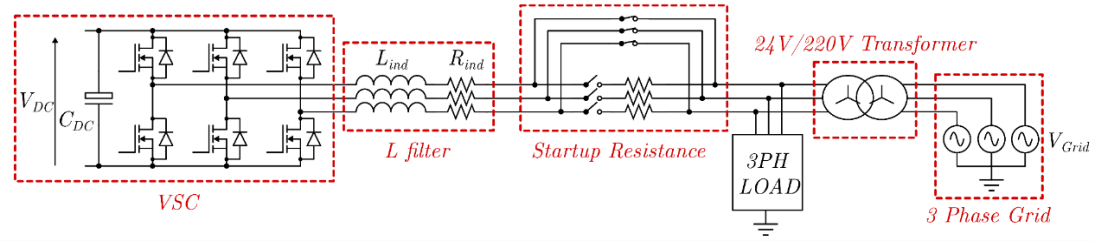

Ilustración 1 - Diagrama eléctrico del sistema.

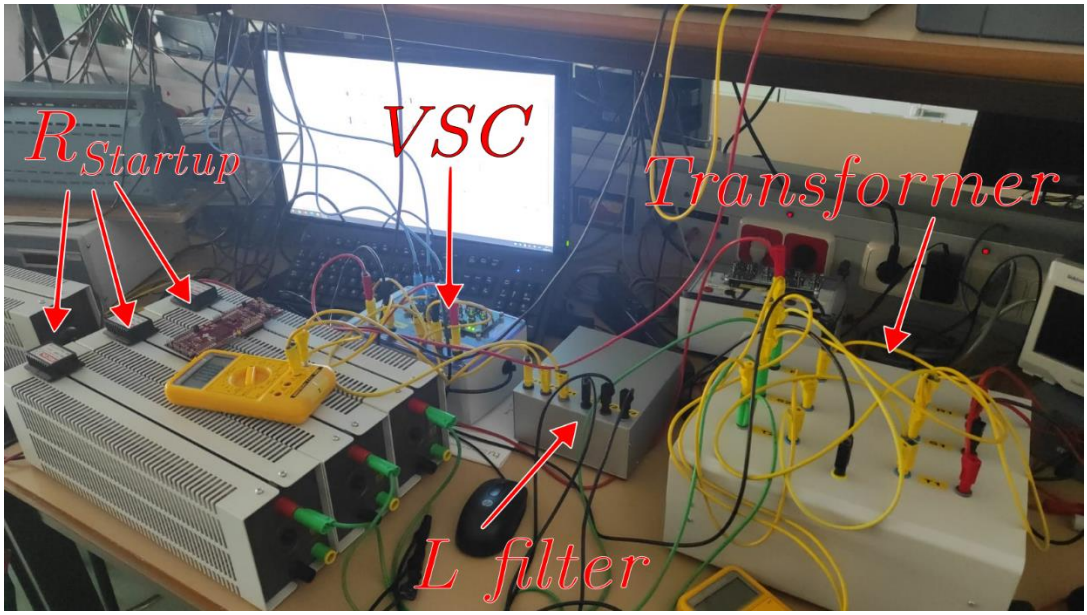

Ilustración 2 – Implementación del prototipo en el laboratorio.

En la Ilustración 3 se puede ver un diagrama general del sistema de control del dispositivo. El control de las potencias se lleva a cabo controlando las corrientes de salida del convertidor, las cuales a su vez dependen de la tensión de salida. Las señales trifásicas senoidales de tensión y corriente de la red se miden en el lado de baja tensión del transformador, y se cambian al sistema de referencia dq0 mediante la transformada de Park. La mayor ventaja de esta transformación matricial es que, en ausencia de armónicos, permite representar las señales senoidales trifásicas como valores constantes en dos ejes ortogonales, d y q [3], lo cual simplifica su control.

En primer lugar, un sistema PLL (*Phase-Locked Loop*) modifica el ángulo utilizado por los bloques de transformada de Park hasta que la transformación de las señales de tensión de la red se represente solo en el eje d, con el valor en el eje q valiendo 0. A partir de este momento, las corrientes en eje d, es decir, alineadas con la tensión de la red, transportarán potencia activa, mientras que las corrientes en eje q serán responsables de la reactiva [4].

El sistema debe absorber potencia activa de la red durante su funcionamiento para mantener la tensión del condensador en el lado de continua, que se reduce constantemente debido a las pérdidas durante el funcionamiento. Para ello, un controlador PI monitoriza

esta magnitud y establece una referencia de corriente en eje d, la cual se garantiza con otro controlador PI, como se ve en la Ilustración 4. Para controlar la variable de mayor interés del sistema, la potencia reactiva generada, otro controlador establece la referencia de corriente en eje q necesaria. Finalmente, la salida de los controles de corriente se vuelve a convertir al sistema de referencia senoidal y se implementa mediante PWM.

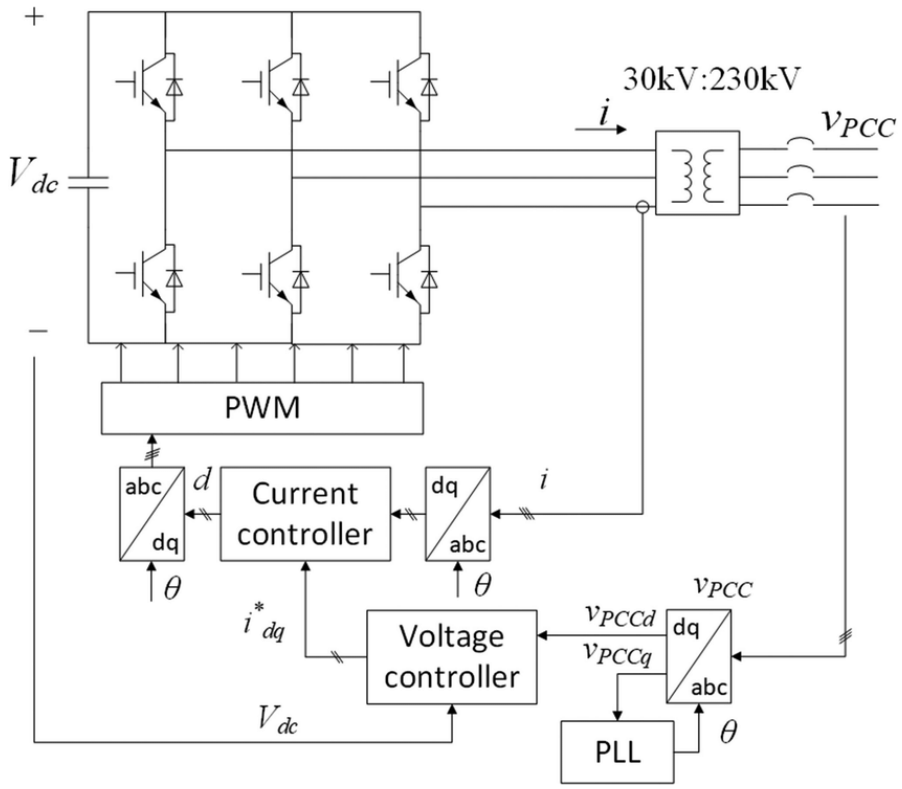

Ilustración 3 - Diagrama general del sistema de control [5]

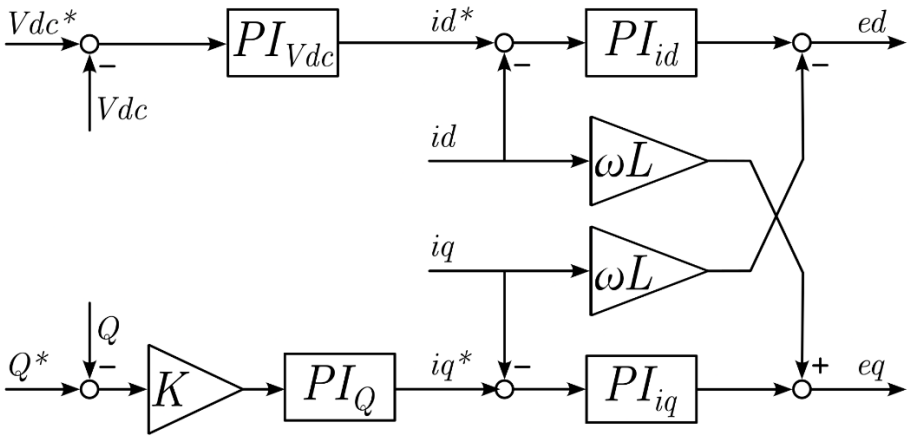

Ilustración 4 - Detalle de la relación entre los controles

4. Resultados

Los resultados de las simulaciones se muestran en la Ilustraciones 5 y 6. La Ilustración 5 muestra la compensación del consumo de una carga de 80 var comenzando alrededor de los 0.4 segundos. Se puede observar que la reactiva proporcionada por

la red se cancela muy rápidamente y sin sobrepaso, y que la potencia activa proporcionada por la red también aumenta para compensar las pérdidas del sistema durante su funcionamiento. El pico de potencia activa entregada en torno a los 0.3 segundos se corresponde con la carga inicial del condensador hasta que alcanza su tensión nominal.

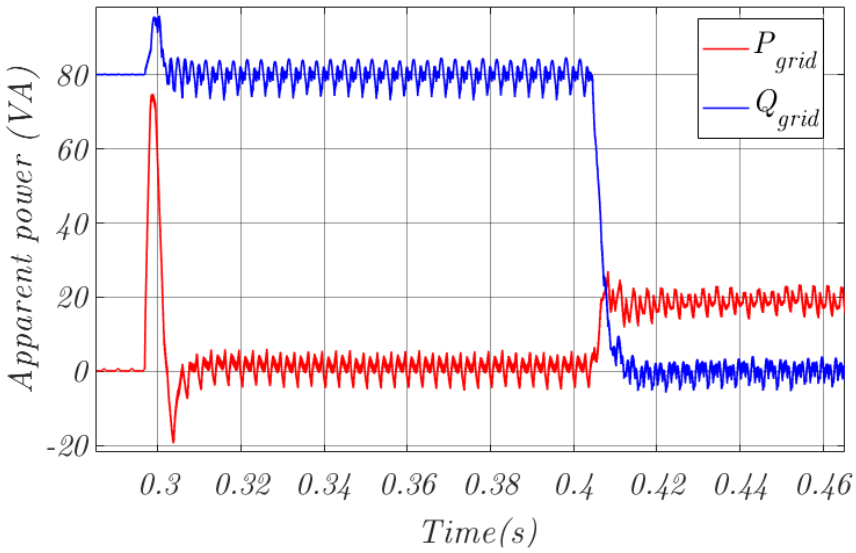

Ilustración 5 - Potencia aparente entregada por la red durante un ensayo con carga inductiva de 80 var.

La Ilustración 6 muestra la disminución notable en la magnitud de las corrientes entregadas por la red en el gráfico superior, así como su adelanto de fase al pasar a proporcionar exclusivamente potencia activa.

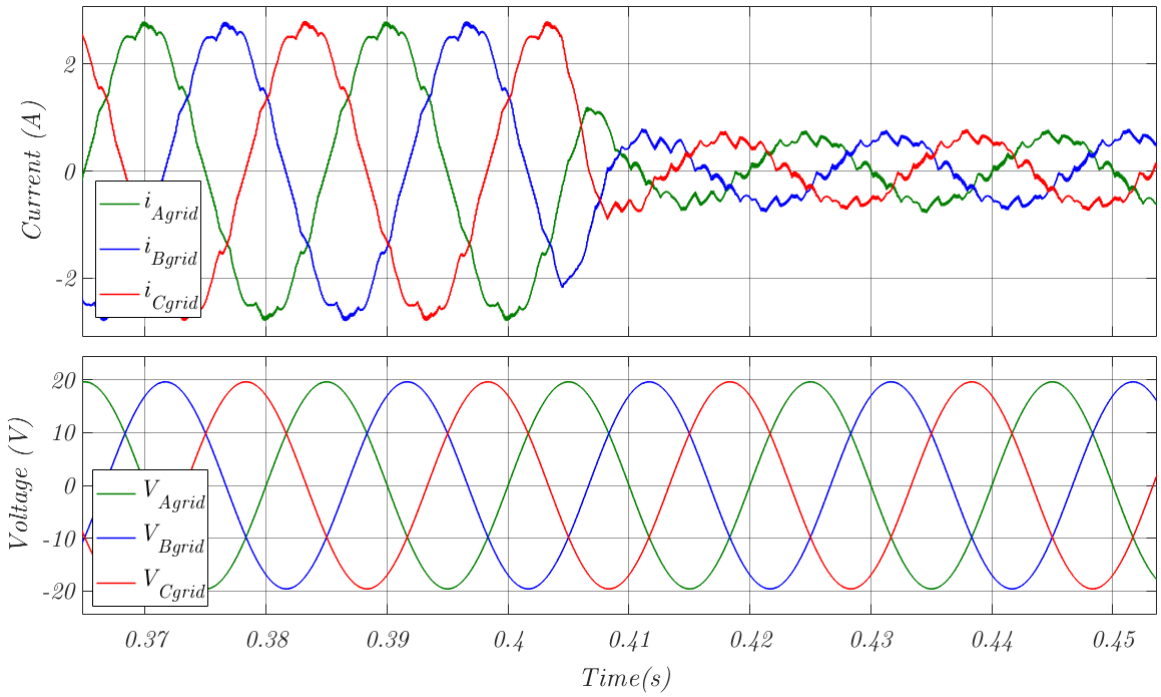

Ilustración 6 - Corrientes y tensiones de la red durante un ensayo con carga inductiva de 80 var.

Lamentablemente, los ensayos con el prototipo del laboratorio no dieron los resultados esperados.

5. Conclusiones

El desarrollo de este proyecto ha generado un sistema con el cual es posible entender los detalles de la operación de un STATCOM implementado con un convertidor CC-CA, y facilitar su implementación en un prototipo físico.

6. Referencias

[1] International Energy Agency, “Renewable energy market update - June 2023.” IEA, Paris, 2023. License: CC BY 4.0.

[2] J. Ali, S. Massucco, and F. Silvestro, “Aggregation strategy for reactive power compensation techniques—validation,” Energies, vol. 12, no. 11, 2019.

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DEVELOPMENT OF A VSC-BASED LOW VOLTAGE STATCOM SYSTEM

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Collaborating Entity: ICAI – Universidad Pontificia Comillas

ABSTRACT

In this project, a three-phase voltage source converter connected to the electrical grid was used to provide power factor correction.

Keywords: STATCOM, VSC, reactive power control, power factor correction, grid integration.

1. Introduction

The increasing share of the energy market held by renewable sources is displacing traditional power plants and large synchronous generators [1]. One of the functions traditionally performed by these generators is power factor correction within the grid, a role that will now be undertaken by DC-AC converters, among other devices [2]. This paper outlines the design and development process of a Static Synchronous Compensator (STATCOM) system based on a three-phase Voltage Source Converter (VSC) to provide power factor correction to a grid, offering rapid response and minimal harmonic injection. In this summary, we first present the hardware and software element designs. Subsequently, the control system design is detailed. Finally, the outcomes of computer simulations and physical prototype testing are discussed.

2. Project definition

The objective of this project is to design a STATCOM system using a three-phase Voltage Source Converter that can rapidly respond to changes in the reactive power demand of the electrical grid while avoiding the introduction of a high level of harmonics in the output currents. Initially, the system will be simulated using Matlab and Simulink, followed by the construction of a laboratory prototype.

3. System description

Figure 1 presents the system’s electrical diagram, and Figure 2 shows its implementation in the prototype developed in the laboratory. The converter charges its DC-side capacitor using energy sourced from the grid. Through appropriate transistor manipulation using Pulse Width Modulation (PWM), output voltages from the converter can be generated that are not in phase with the grid's, enabling control over the active and reactive powers absorbed by the device. Positioned between the converter and the grid there is an L filter to diminish harmonics in the output currents, a startup resistance for preloading, and a transformer for voltage adaptation to the grid. Between the transformer and the startup resistance, a load can be introduced for its reactive power to be compensated by the converter, or alternatively, a reactive power generation reference can be set directly.

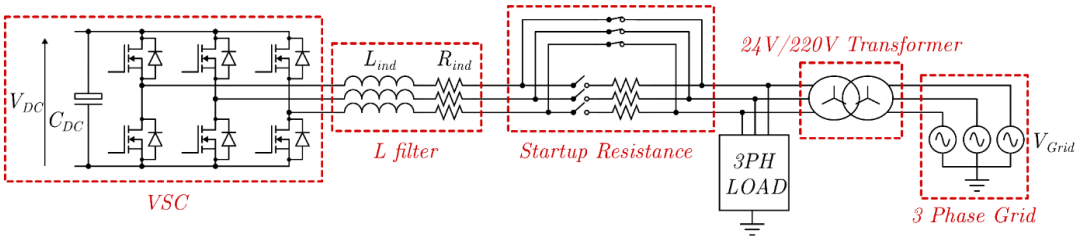

Figure 1 – General electrical diagram of the system.

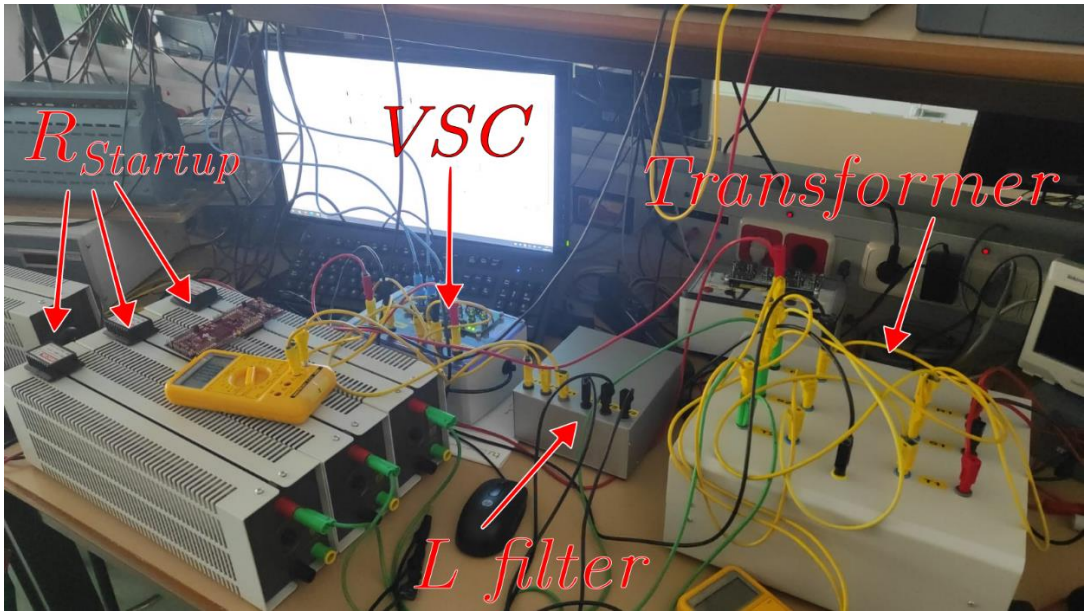

Figure 2 – Laboratory setup.

Figure 3 presents a comprehensive diagram of the control system for the device. Active and reactive power control is achieved by managing the output currents of the converter, which depend upon its output voltage. Sinusoidal three-phase voltage and current signals from the grid are measured at the low-voltage side of the transformer and are transformed into the dq0 reference frame using the Park transformation. The principal advantage of this matrix transformation is that, in the absence of harmonics, it permits the representation of sinusoidal three-phase signals as constant values along two orthogonal axes, d and q [3], thereby simplifying their control.

Initially, a Phase-Locked Loop (PLL) system adjusts the angle employed by the Park transformation blocks until the transformation of the grid's voltage signals is exclusively represented along the d-axis, with the value along the q-axis being 0. After this stage, currents along the d-axis, aligned with the grid's voltage, will convey active power, while currents along the q-axis will govern the reactive power [4].

The system must absorb active power from the grid during its operation to maintain the voltage of the DC-side capacitor, which experiences continuous reduction due to losses during operation. To achieve this, a PI controller monitors this magnitude and establishes a current reference along the d-axis, which is ensured through another PI controller, as depicted in Figure 4. In order to manage the most critical variable of the system, the generated reactive power, yet another controller sets the required current reference along

the q-axis. Finally, the output of the current controllers is transformed back into the sinusoidal reference frame and is implemented using PWM.

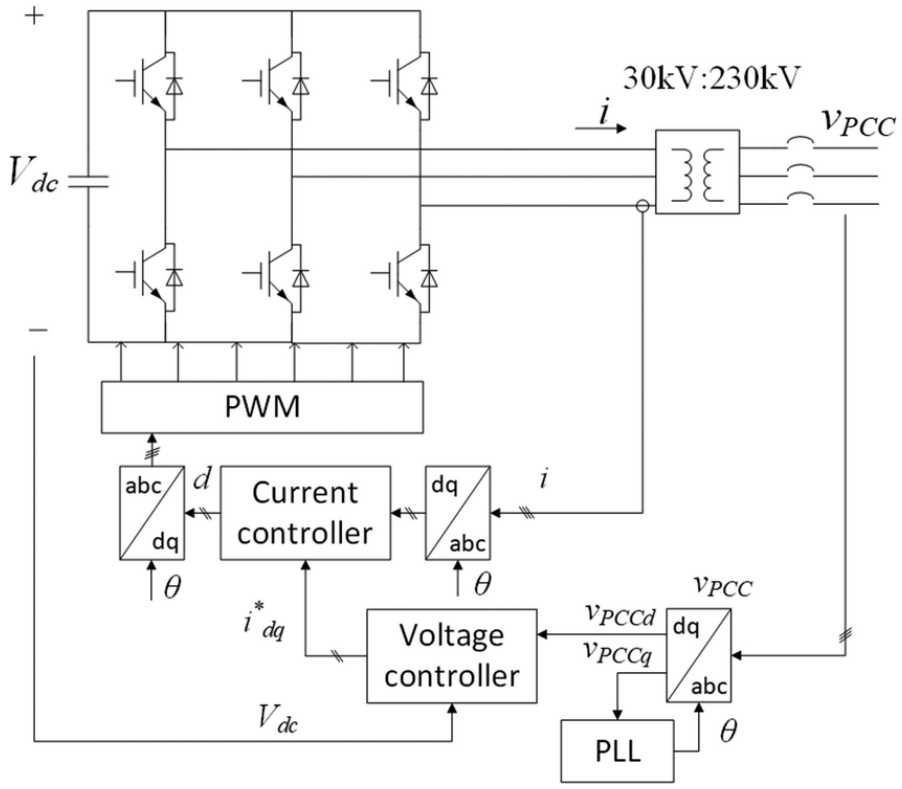

Figure 3 – General diagram of the control system [5].

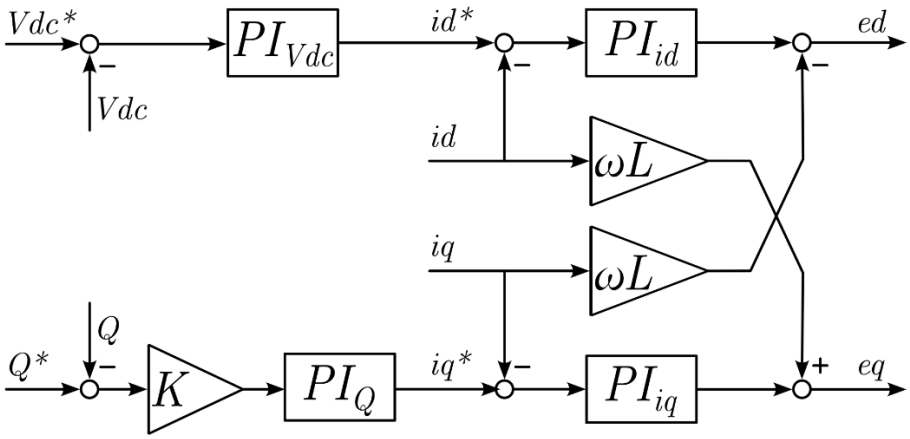

Figure 4 – Detailed diagram of the relationship between controllers.

4. Results

The simulation results are presented in Figures 5 and 6. Figure 5 illustrates the reactive power compensation for an 80 var load commencing around 0.4 seconds. It can be observed that reactive power supplied by the grid is swiftly cancelled without overshoot, and the active power provided by the grid also rises to compensate for system losses during operation. The peak of active power delivered around 0.3

seconds corresponds to the initial capacitor charging phase until it reaches its nominal voltage.

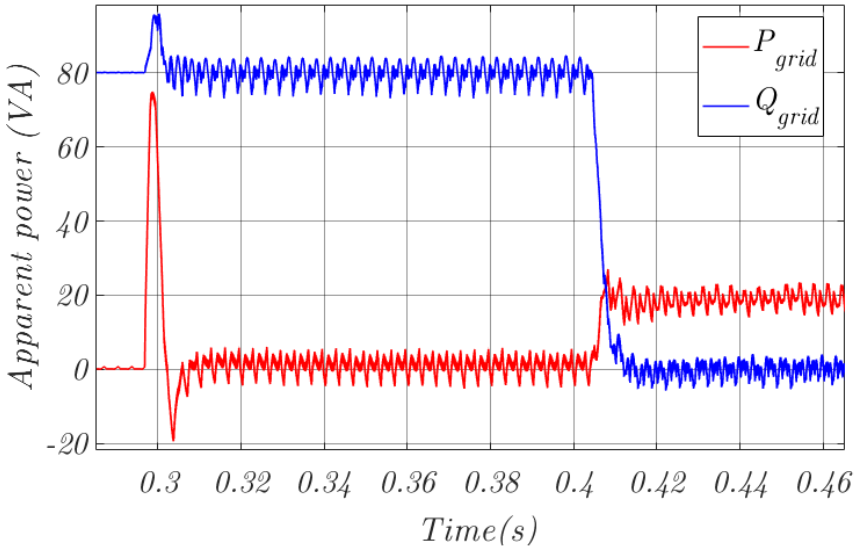

Figure 5 – Apparent power delivered by the grid during a test with an 80 var inductive load.

Figure 6 depicts the noticeable reduction in the magnitude of currents supplied by the grid in the upper graph, as well as their phase advancement as they shift to exclusively delivering active power.

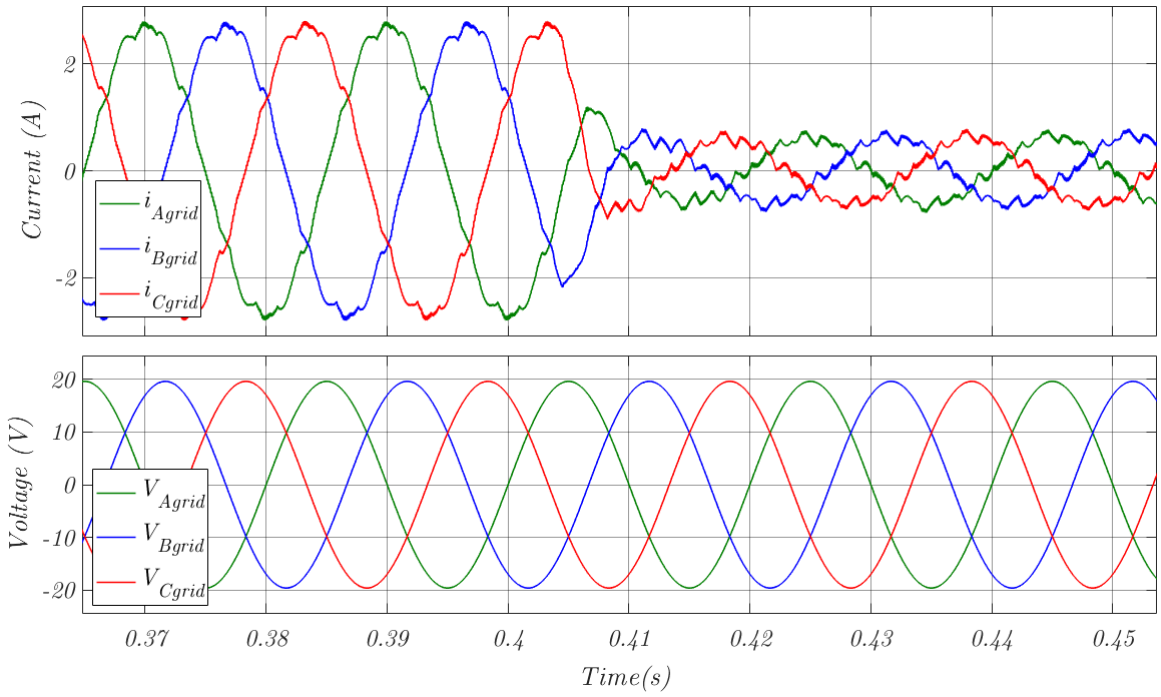

Figure 6 – Grid currents and voltages during a test with an 80 var inductive load.

Unfortunately, the laboratory prototype tests did not yield the expected outcomes.

5. Conclusion

The completion of this project has resulted in a system that allows for a comprehensive understanding of the operational intricacies of a STATCOM implemented using a DC-AC converter, thereby facilitating its realization in a physical prototype.

6. References

[1] International Energy Agency, “Renewable energy market update - June 2023.” IEA, Paris, 2023. License: CC BY 4.0.

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Contents

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Chapter 1

Introduction

This document summarises the design and development process of a STATic synchronous COMPensator (STATCOM) device prototype based on a three-phase voltage source converter (VSC). The complete setup includes the converter, an L filter for improved current waveforms, and a transformer to adapt the voltage to that of the three-phase grid. The purpose of this device is to absorb or inject a specified amount of reactive power from and into a three-phase grid, with the ultimate aim of improving the grid power factor, while minimizing active power consumption. This type of device excels at environments where a fast response to a change in reactive power demand is required, but should work alongside other devices with a higher energy efficiency for steady state reactive power compensation [6]. This document is structured as follows. First, the state of the art of power factor correction technologies is reviewed. Then, the modeling of the different elements is introduced. After that, the design and simulation process of the control algorithms is explained. Finally, the implementation of these algorithms in a physical prototype, as well as an analysis of the results, is presented.

1.1 Project motivation

The rise of renewable energy technologies in modern electrical networks is displacing traditional power plants, which use large synchronous generators, with more inverter-based resources (IBR) [7]. The increasing use of renewable energy sources in modern electrical networks is leading to the replacement of power plants that relied on large synchronous generators (SGs) with more inverter-based resources (IBR). These SGs are very effective at reactive power compensation, and their disappearance in certain parts of networks requires the creation of plants that can emulate that role. An example of this scenario can be found in the case of the Holly STATCOM in Texas [8]. In the coming years, more of this SGs will be phased out,

making the development of efficient and effective reactive power compensators a top priority for the electric power industry.

1.2 Objectives

The main objective of this project is to develop a device that can output a specified amount of reactive power set by the user. Additionally, it must be as quick as possible in reacting to a change in demand, and avoid introducing excessive harmonics into the grid.

Chapter 2

Review of power factor correction technologies

Power factor correction involves compensating the reactive power generated in a grid. The compensation of this reactive power provides several benefits, among them:

1. Reduced current magnitudes for a given active power load, which saves energy during transmission by reducing resistive losses ($i^2 \cdot R_{line}$), as well as freeing current capacity from the grid, which can be used to deliver active power.

2. Provides a way to regulate the voltage of nodes in the grid, which helps keep them within the specified margin required by consumers. An extended explanation for this can be found in section 4.2.

Many systems have been developed to solve the power factor correction, ranging from those consisting of purely passive elements to higher complexity ones. Historically, capacitor banks have been used to passively compensate reactive power where its demand was anticipated, with the synchronous generators in thermal and hydropower plants providing a dynamic response to reactive power demand [6]. The gradual replacement of traditional power plants and their synchronous generators by renewable energy alternatives, as well as the increasing prevalence of microgrids, have led to the development of innovative methods of power factor correction.

2.1 Power electronics technologies

2.1.1 Capacitor banks

Capacitor banks are the simplest solution to the problem of reactive power compensation. Current through a pure capacitor connected to an AC grid is always leading the voltage by ninety degrees, which means that the capacitor always generates reactive power. This is a limitation when compared to other technologies which can both generate and absorb reactive power from the grid, but given that most loads are usually inductive, reactive power generation is usually what is required. Additionally, the amount generated depends solely on grid voltage and bank capacitance, and cannot be controlled without using additional components. This kind of solution is valued for its low cost and its simplicity and can be used to compensate the baseline reactive power expected from induction motors used in industrial plants.

2.1.2 Static Var Compensators

Static Var Compensators, or SVCs, are the next step towards controlling the reactive power output required by the grid, coming from simple capacitor banks. These systems employ capacitors and reactors which can be individually connected or disconnected from the grid through the switching of thyristors [1]. This provides fine and variable control over the output, although it is limited to discrete steps.

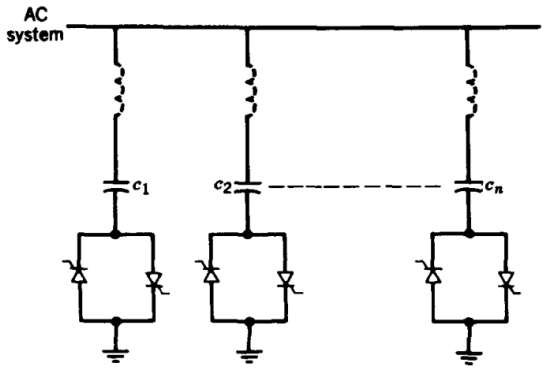

Figure 2.1: Thyristor switched capacitor arrangement [1]

2.1.3 Static synchronous compensator technologies

STATCOM technologies provide continuous and precise control over the desired reactive power output, as well as high speed. The most basic design, like the

one explored in this project, involved using an inverter with two levels (high and low), which, through Pulse Width Modulation (PWM) generates the desired sinusoidal output voltage, and with it, controls the phase and magnitude of the current absorbed by the device, thereby controlling the absorbed reactive power. A detailed explanation of the operation of this device can be found in Chapter 4, and Figure 2.2 shows a basic diagram of it.

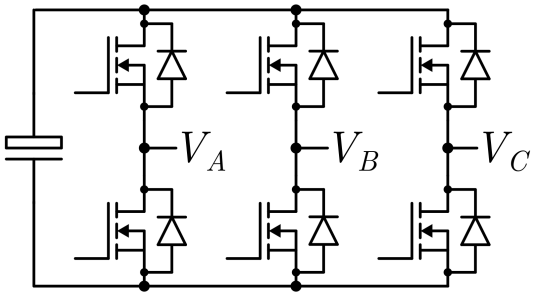

Figure 2.2: Diagram of the VSC topology used in this project.

The generation of sinusoidal waves using PWM and two possible voltage levels generates harmonic distortions in grid currents even after filtering. In order to mitigate these problems, multilevel STATCOM designs have been developed to provide more possible output values, which allows the pre-filtered signal to more closely resemble the desired sinusoidal form, as seen in Figure 2.3.

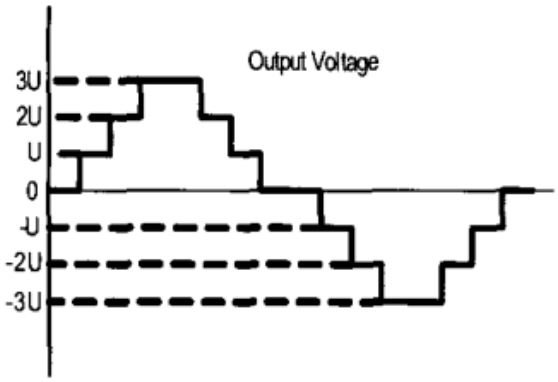

Figure 2.3: Discrete multilevel voltage outputs of a three level cascade converter [2]

This waveform is a result of the three-level topology from Figure 2.4.

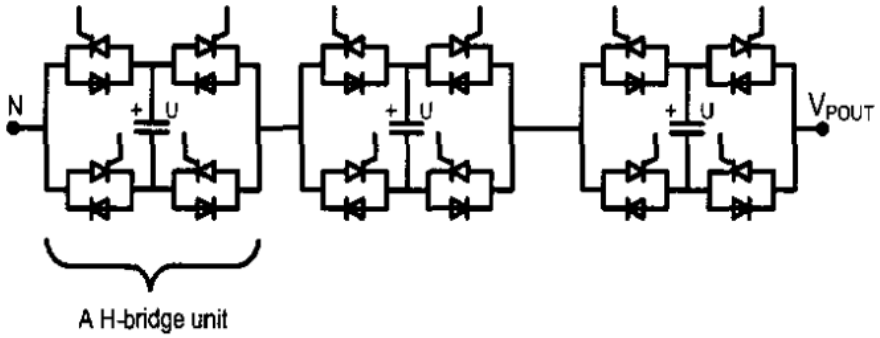

Figure 2.4: Single phase diagram of a cascaded H-bridge topology converter [2]

There are three main types of multilevel converters [9]:

- Diode clamped multilevel converters
- Flying capacitor multilevel converters
- Cascaded H-Bridge multilevel converters

Another aspect to consider when classifying STATCOM toplogies is phase independence. The dq0 reference frame typically used to design the controllers can only operate with the assumption that the three phases are balanced. There are designs and control schemes that act on each phase of the grid independently, which allows the device to correct imbalances between phases in addition to power factor correction. A collection of many of the possible topologies can be found in [10].

2.2 Comparison and aggregation strategies

Every system used presents its own advantages when it comes to costs, efficiency, response speed, and reactive power generation capacity. Due to this , they are commonly used together to optimize the service provided. A practical application can be found in the case of the Holly STATCOM in Texas [8]. In this case, the decommissioning of an old oil-powered thermal plant and its synchronous generators put the local voltage stability at risk. In order to carry out the required voltage control, a specialised facility was developed. As seen in the report, the final design included fixed capacitor banks, as well as an SVC and A Voltage Source Converter STATCOM.

This setup acts to the advantages presented by each of the elements as explained in [6]:

- Capacitor banks take care of the constant reactive power demand. They are highly efficient and cheap, but can get bulky.
- The SVC has a lower efficiency due to the losses in the switching components, but it is still higher than that of the VSC. Its role is to provide reactive power control for a longer time frame.
- The VSC has a very high response speed as its main advantage. When a fault occurs in the grid, it is the first to react. Its efficiency, however, is much lower, which is the reason why it is only used while the slower SVCs adapt to the change in demand.

Chapter 3

Relevant Equations

In this chapter, the foundational equations used throughout the rest of the document to perform design calculations and inform decisions will be presented.

3.1 Park's transform and the dq0 reference frame

Controlling the voltages of a three-phase electrical system made up of three sinusoidal signals 120 degrees apart can be simplified by implementing Park's transform. an algebraic transformation that represents the three balanced AC phase voltages as two DC values, v_d and v_q, which remain constant in time during steady state periods. This is achieved using two subsequent transformations. First, one of the phase voltage phasors is represented as a sum of two perpendicular vectors, d and q. This first transformation is known as Clarke's transform. Then, a rotation at a certain speed ω which matches the grid frequency guarantees that the coordinates of the chosen phasor will remain the same. The combination of Clarke's transform with a rotating reference frame is known as Park's Transform [11]:

$$\begin{pmatrix} v_d \\ v_q \\ v_0 \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{pmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ -\sin(\omega t) & -\sin\left(\omega t - \frac{2\pi}{3}\right) & -\sin\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} \begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} \tag{3.1}$$

The form with these scaling parameters is known as the power-invariant Park transform. Mathematically, it is just a rotation with no scaling [11], which means that dot product relationships like instantaneous power remain constant under the transformation [12], that is,

$$p(t) = v_a(t) \cdot i_a(t) + v_b(t) \cdot i_b(t) + v_c(t) \cdot i_c(t) = v_d(t) \cdot i_d(t) + v_q(t) \cdot i_q(t) + v_0(t) \cdot i_0(t)$$

This is the version used in this project. The resulting equations for active and reactive power are [13]:

$$P = v_d \cdot i_d + v_q \cdot i_q \tag{3.2}$$

$$Q = v_q \cdot i_d - v_d \cdot i_q \tag{3.3}$$

A rigorous derivation of Park's transform, as well as a detailed explanation of its geometric interpretation with illustrative graphics was made by O'Rourke et al. [11].

3.2 Plant modeling equations

In order to be able to design the control system, a model of the controlled plant is needed. Figure 3.2 shows a simplified one phase diagram of the system. All control objectives are achieved by setting a reference current output, but the only variable that can be directly set is the converter voltage, so it is essential to find an equation that relates the two. Using Kirchhoff's voltage law, equation 3.4 can be derived.

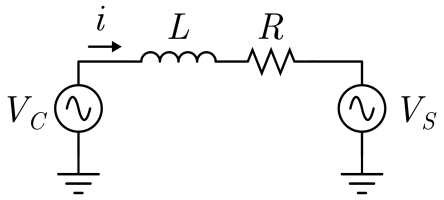

Figure 3.1: Single phase diagram of the system.

$$V_C = V_S + \frac{di}{dt} \cdot L + i \cdot R \rightarrow V_C - V_S = \frac{di}{dt} \cdot L + i \cdot R \tag{3.4}$$

Using matrix notation to represent the three phases of the system, we get:

$$\begin{pmatrix} V_a \\ V_b \\ V_c \end{pmatrix} = R \cdot \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} + L \cdot \frac{d}{dt} \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} \tag{3.5}$$

Now, the sinusoidal variables are substituted for the dq0 reference frame variables, mediated by the inverse Park transform $P = P_{abc \rightarrow dq0}$ seen in equation 3.1:

$$P^{-1} \cdot \begin{pmatrix} v_d \\ v_q \\ v_0 \end{pmatrix} = R \cdot P^{-1} \cdot \begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix} + L \cdot P^{-1} \cdot \frac{d}{dt} \begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix} \tag{3.6}$$

Applying the Park transform to both sides, we obtain equation 3.7.

$$P \cdot P^{-1} \cdot \begin{pmatrix} v_d \\ v_q \\ v_0 \end{pmatrix} = P \cdot R \cdot P^{-1} \cdot \begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix} + P \cdot L \cdot P^{-1} \cdot \frac{d}{dt} \begin{pmatrix} i_d \\ i_q \\ i_0 \end{pmatrix} \tag{3.7}$$

After performing the matrix operations presented in equation 3.7, taking into account the properties of the derivatives of variables in a rotating reference frame, as shown in equation 3.8 [14], and ignoring the zero component, we obtain equations 3.9 and 3.10, which will be used to model the plant. An important insight provided by these equations is that, even in steady state, currents i_d and i_q are not only affected by the corresponding converter v_d and v_q voltages, but also by each other's values. This cross relationship is known as coupling, and its cancellation during the control stage is known as decoupling. Decoupling serves to make the overall control faster by removing the burden of reacting to changes in the other current from each current PI controller.

$$\left(\frac{d\vec{A}}{dt}\right)_{inertial} = \left(\frac{d\vec{A}}{dt}\right)_{rotating} + \vec{\Omega} \times \vec{A} \tag{3.8}$$

$$v_d = R \cdot i_d + L \cdot \frac{di_d}{dt} - \omega \cdot L \cdot i_q \tag{3.9}$$

$$v_q = R \cdot i_q + L \cdot \frac{di_q}{dt} + \omega \cdot L \cdot i_d \tag{3.10}$$

3.3 Base magnitudes

The per-unit system makes it easy to compare magnitude values with their nominal value. The nominal DC voltage for the VSC is 48V[4]. Given that half of this value represents the maximum possible sinusoidal amplitude by the output voltage of the inverter, a base RMS voltage of $\frac{48}{2\sqrt{2}} = 16.97V$ was selected. While the inverter can sustain currents of up to 10A, the inductances used can only sustain a maximum current of 5A. In order to remain far enough from this value, a base current value of 2.5A was selected. The grid and inverter frequencies are 50Hz. With these base

magnitudes, the rest can be calculated as follows:

$$V_{DC} = 48V$$
$$U_b = \frac{V_{DC}}{2\sqrt{2}} = 16.97V$$
$$I_b = 2.5A$$
$$F_b = 50Hz$$
$$\omega_b = 2\pi F_b = 314.2rad/s$$
$$S_b = 3 \cdot U_b \cdot I_b = 126.8VA$$
$$Z_b = \frac{U_b}{I_b} = 6.76\Omega$$
$$L_b = \frac{Z_b}{\omega_b} = 0.0215H$$

Chapter 4

System design and operation

In this chapter, the elements that make up the hardware of the project will be listed, and their individual roles will be explained. Then, the electrical connections in the prototype will be presented, as well as the general operational principles of the complete setup.

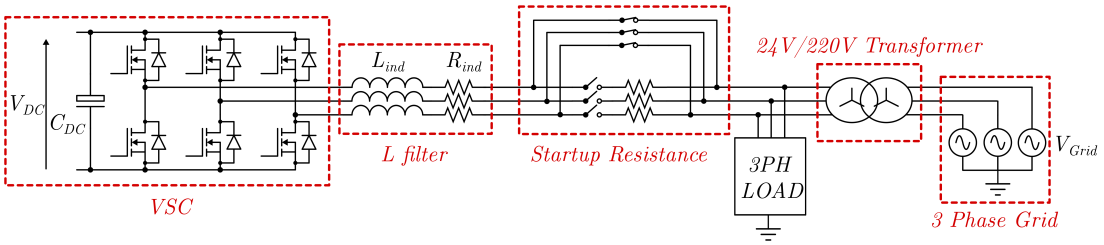

Figure 4.1: General diagram of the system used for simulation.

4.1 Hardware elements

The main hardware elements that make up the prototype are:

1. Three-phase transformer
2. Filter inductance
3. Startup resistance
4. BOOSTXL-3PhGaNInv VSC
5. LAUNCHPADXL - F28379D

4.1.1 Three-phase transformer

The prototype uses a 220/24V shell-type three-phase transformer made up of three individual single-phase transformers in a STAR-STAR configuration. The main role of this component is to step down the three-phase grid voltage to the nominal levels of the available converter. Additionally, it provides electrical insulation from the grid in case of failures.

4.1.2 Filter inductance

A three-phase L filter of 5.88 mH per phase is used to reduce the current harmonics in the output of the inverter.

4.1.3 Startup resistance

A 100 Ω three-phase variable resistance is used to reduce the currents that flow into the DC side of the inverter during the first instants after connecting to the grid, when the DC link capacitor is discharged. Once this initial current surge is over, this resistor would generate significant active power losses. To reduce these conduction losses, the resistors are bypassed once a stable voltage is reached in the DC link capacitor

4.1.4 BOOSTXL-3PhGaNInv VSC

The BOOSTXL-3PhGaNInv by Texas Intruments is the VSC used for this project. The following are its main characteristics [3], [15]:

- Accepted input DC voltages between 12 and 60V, with a nominal operating DC voltage of 48V.
- Features three 80V and 10A gallium nitride half-bridge modules (LMG5200).
- Includes three INA240 differential current sense amplifiers, one for each phase. The original 5 mΩ shunt resistances had been previously substituted for 15 mΩ ones for increased accuracy.
- Includes external connections to Va, Vb, Vc and Vdc, stepped down to a 3.3V scale for measuring purposes.
- Is compatible with C2000 MCU Launchpad Development Kits for control and evaluation purposes.

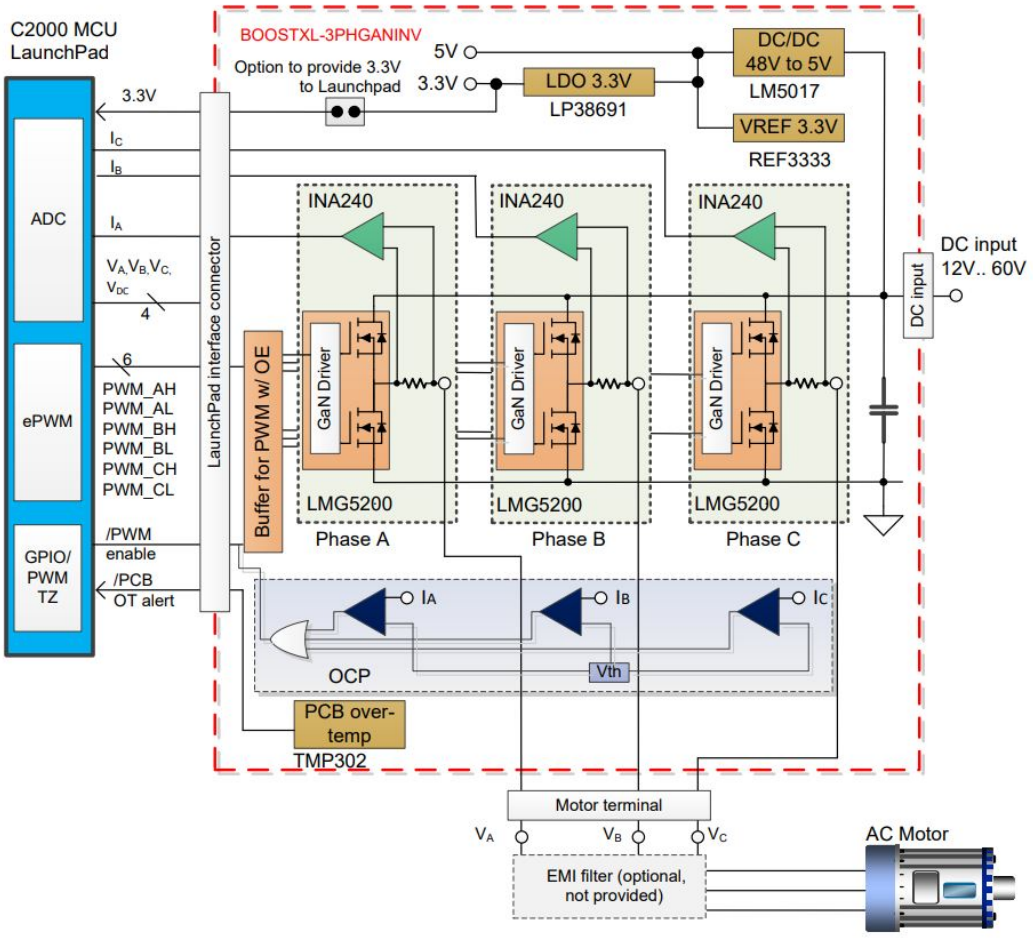

Figure 4.2: Diagram of the BOOSTXL-3PhGaNInv [3].

A complete diagram of the internal elements and the inputs and outputs of the device can be found in Figure 4.2. The pinout is shown in Figure 4.3 and 4.4. It is important to ensure that the inverter and the microcontroller launchpad are lined up properly so that measurements from the VSC can be read through the ADCs and the PWM control signals reach the transistor drivers.

PIN	SIGNAL	I/O (3.3 V)	PIN	SIGNAL	I/O (3.3 V)
J1-1	3.3-V supply (optional)	O or NC (jumper selectable)	J1-2	NC	—
J1-3	NC	—	J1-4	GND	GND
J1-5	NC	—	J1-6	VDC	O (0 to 3.3 V)(1)
J1-7	NC	—	J1-8	VA	O (0 to 3.3 V)(1)
J1-9	NC	—	J1-10	VB	O (0 to 3.3 V)(1)
J1-11	VREF	O (3.3 V, 10 ppm)	J1-12	VC	O (0 V to 3.3 V)(1)
J1-13	NC	—	J1-14	IA	O (0 to 3.3 V)
J1-15	NC	—	J1-16	IB	O (0 to 3.3 V)
J1-17	NC	—	J1-18	IC	O (0 to 3.3 V)
J1-19	NC	—	J1-20	VREF	O (3.3 V, 10 ppm/K)

(1) Overvoltage protection with Schottky diodes ensures output voltage remains below 3.6 V.

Figure 4.3: Table showing the left-side pinout J1 of the BOOSTXL-3PhGaNInv [4].

PIN	SIGNAL	I/O (3.3 V)	PIN	SIGNAL	I/O (3.3 V)
J2-1	PWM A (high-side)	I (10k PD)	J2-2	GND	GND
J2-3	PWM A (low-side)	I (10k PD)	J2-4	NC	—
J2-5	PWM B (high-side)	I (10k PD)	J2-6	NC	—
J2-7	PWM B (low-side)	I (10k PD)	J2-8	NC	—
J2-9	PWM C (high-side)	I (10k PD)	J2-10	NC	—
J2-11	PWM C (low-side)	I (10k PD)	J2-12	NC	—
J2-13	/PCB OT alert	O (open drain, 10k PU)	J2-14	NC	—
J2-15	NC	—	J2-16	/PWM enable (active low)	I (10k PU)
J2-17	NC	—	J2-18	NC	—
J2-19	NC	—	J2-20	NC	—

Figure 4.4: Table showing the right-side pinout J2 of the BOOSTXL-3PhGaNInv [4].

4.1.5 LAUNCHPADXL - F28379D

The LAUNCHPADXL - F28379D, featuring a TMS320F28379D microcontroller, acts as an interface between the computer and the MCU, as well as between the MCU and the VSC. Thus, the most relevant technical information refers to the microcontroller itself.

4.2 Steady state operation

When the voltage across the capacitor on the DC side has reached its reference value after the startup phase, the steady state is achieved. In this state, the device is capable of controlling the power factor of the grid. To illustrate how this works, a simplified system like the one found in Figure 4.5 can be considered. After an analysis is carried out, as in chapter 18 of [1], the resulting equations for active power P and reactive power Q are:

$$P = 3 \cdot \frac{V_c V_s \sin\delta}{X} \tag{4.1}$$

$$Q = 3 \cdot \frac{V_c^2 - V_c V_s \cos\delta}{X} \tag{4.2}$$

where X is the impedance connection between the converter and the source, δ is the angle by which V_c lags behind V_s, which are the phase-to-neutral voltages of the converter and the grid source, respectively, assuming balanced operating conditions. For small values of δ, Q can be considered to be determined exclusively by the magnitude of V_c, while P is determined by δ. The phasor diagram in Figure 4.5 shows the range available for V_c after considering system limitations. It also shows the sign of the active and reactive power generated by the converter as a function of the quadrant occupied by i_S. Since the system is incapable of active power generation in steady state, both left quadrants are only accessible for short periods of time as a part of the regulation process of V_{DC}, as any active power output will drain the DC capacitor.

In general, the device operates in the right quadrants in order to compensate the active power losses that come with regular operation, although i_S will be much closer to the vertical axis than shown in the diagram. This limitation in the stable range of the source current phasor means that jXi_S will only be in the bottom right quadrant, and V_C is constrained by its own maximum value V_{Cmax}, the half circumference of radius jXi_{Smax} with center in V_S, and the minimum voltage attainable V_{Cmin}, corresponding with the value of V_{DC} obtained in rectification. Rectification will be further explained in section 4.3.1.

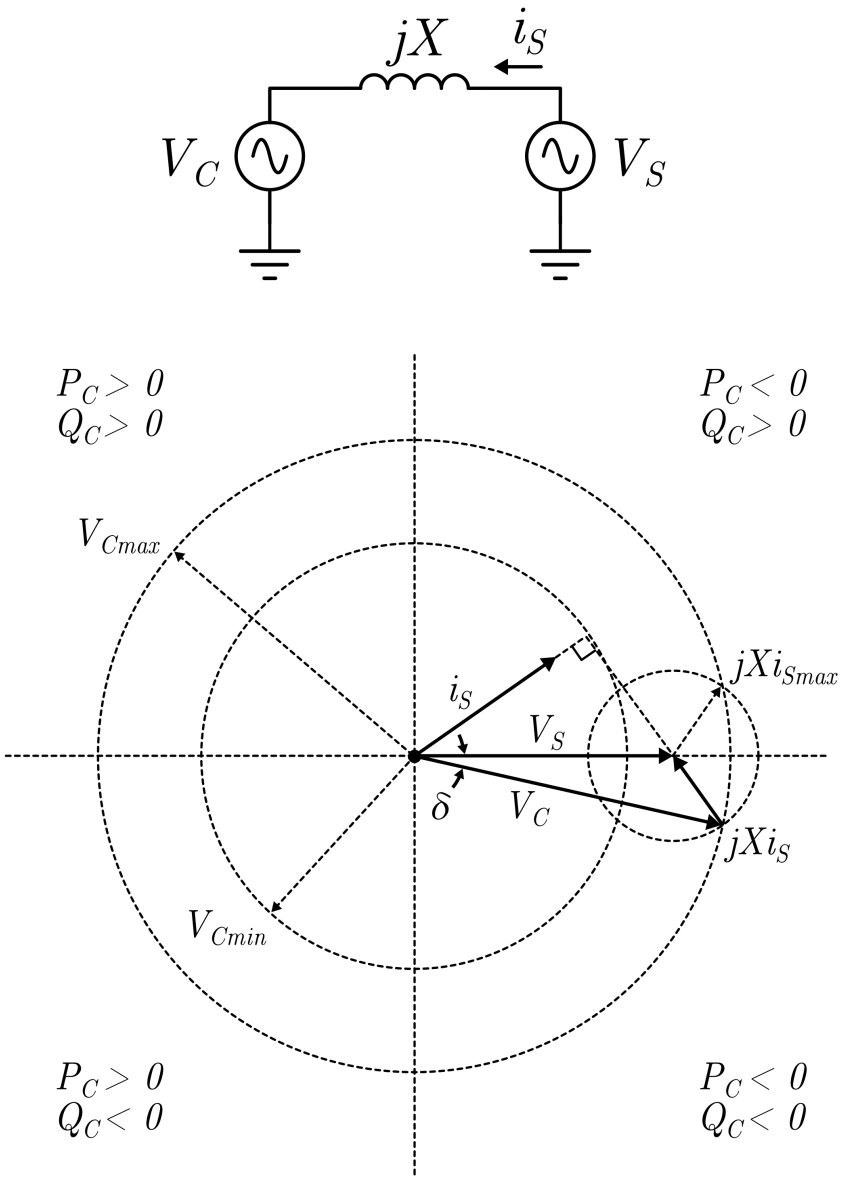

Figure 4.5: Simplified electrical diagram of the system and proportional phasor diagram, along with the areas of operation of the converter in each quadrant as a function of i_S, considering the converter as a generator.

During regular operation, δ will be very close to zero, but it can reach a maximum angle of:

$$\delta_{max} = \tan^{-1}\left(\frac{X \cdot i_{Smax}}{V_{Sph}}\right) = \tan^{-1}\left(\frac{0.00588 \cdot 2\pi \cdot 50 \cdot 2.5}{\frac{24}{\sqrt{3}}}\right) = 18.43° \qquad (4.3)$$

This happens when i_S is aligned with V_S, and the system is absorbing active power from the network while generating no reactive power, resulting in the capacitor charging. This only takes place during the startup phase.

The above explanation is intuitive, but technically complicated to implement. For this reason, the device actually controls i_d, which is proportional to P, and i_q, which controls the output of Q, as shown in chapter 3. One PI controller ensures that V_{DC} reaches and remains at its nominal value by setting the right reference for i_d. Due mainly to resistive losses, this reference will almost always be negative. Another PI controller carries out the main objective of the system: it takes in the measurement of the reactive power supplied by the grid to a load, and acts on i_q to generate or consume that much reactive power, ultimately driving it to zero, reducing the magnitude of the grid currents and saving energy during the transmission phase.

4.3 Startup procedure

The startup phase is the period when the DC capacitor voltage V_{DC} is raised to its nominal value from an assumed 0V, before steady state operation can begin. It can be divided in 3 stages:

1. Startup in rectifier mode
2. PLL synchronization with the grid
3. Active power absorption to reach final V_{DC}

4.3.1 Startup in rectifier mode

The device cannot operate correctly if V_{DC} is close to 0V, so initially the control system in charge of driving it to $V_{DC_{Ref}}$ would be unable to achieve its goals. For this reason, the VSC starts in rectifier mode, with no switching of the transistors and the PI controllers turned off. Eventually, without taking inductances into account, a steady state is reached when [1]:

$$V_{DC_0} = 1.35 V_{S_{LL}} \qquad (4.4)$$

where V_{DC_0} is the average value of V_{DC} and $V_{S_{LL}}$ is the phase-to-phase voltage in the AC side. In practice, inductances make instantaneous commutations in the current impossible, but they remain very small once steady state is reached. This means that, in steady state, the voltages on the three-phase ports of the converter can be considered to be equal to the grid voltages. This will be useful during the PLL stage.

Another important consideration is the overvoltages and overcurrents experienced by components at turn-on. As seen in [1], considering the worst case scenario where the DC-side capacitor is initially fully discharged, the maximum voltage across it could reach $V_{DC_{Max}} = 2\sqrt{2}V_{S_{LL}}$ before settling into its steady state value. For a 24V grid, this would be a peak of 67V. Despite this, startup resistances have been included to avoid these voltage spikes, as well as their corresponding current spikes, to ensure that factors that may not be accounted for in the model don't push the DC voltage higher than the rated voltage of the components in the real prototype. The lowest constraint to this voltage is presented by the GaN transistors, which can sustains a maximum of 80V across them. Once the voltage is closer to the final steady state value, these resistances are bypassed to avoid unnecessary energy losses.

For a 24V grid, the steady state value of V_{DC} would ideally be close to 32.4V.

4.3.2 PLL synchronization with the grid

Once the system has achieved steady state conditions in the rectification mode of operation, the PLL subsystem (Phase Locked Loop) is activated. Its role is to generate the appropriate angle which will be used by all Park transformationblocks. This signal has the following characteristics:

- It is a ramp that goes from 0 to 2π, at which point it resets instantly back to 0.
- This rotating frame is aligned with the grid three-phase voltage in such a way that its $V_{S_q} = 0$

Since i_q and i_d of the converter are the essential controlled variables in the system, this step is essential to ensure correct alignment with the grid voltage. The alignment of V_{S_q} with what will be considered the A phase of the grid is arbitrary, but convenient when reviewing how the equations derived in chapter 3 change as a result:

$$P = v_d \cdot i_d + v_q \cdot i_q \xrightarrow{\text{when } v_q=0} P = v_d \cdot i_d \tag{4.5}$$

$$Q = v_d \cdot i_q - v_q \cdot i_d \xrightarrow{\text{when } v_q=0} Q = v_d \cdot i_q \tag{4.6}$$

With this alignment, the absorbed active power P can be controlled exclusively with i_d, while Q depends solely on i_q. With the current decoupling shown in chapter 3, this means that P and Q can be controlled independently.

The way this PLL subsystem achieves this is using a PI controller that takes the quadrature component of the grid voltage in a dq0 frame, V_{S_q}, as its input, and outputs an angular speed ω, which is then input into an integrator, obtaining an angle θ. This θ is the angle variable used by all other Park transform blocks in the system. It is then fed back into the Park transform block that generated V_{S_q} from the grid voltage readings, eventually driving it to zero at steady state. A diagram of the system can be found in figure 4.6

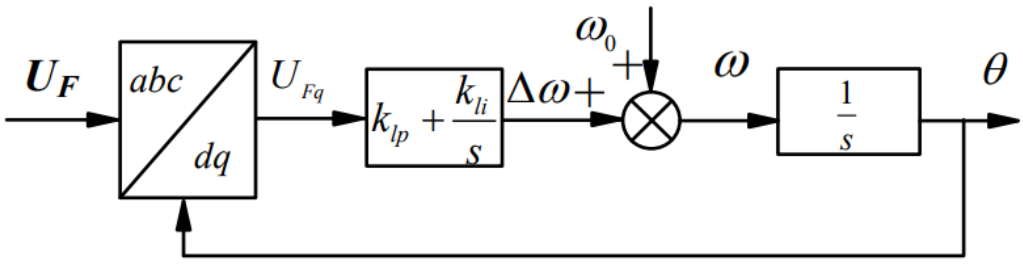

Figure 4.6: Block diagram of the PLL system used [5]. In practice, the integrator resets every time $\theta = 2\pi$

Once V_{S_q} can be considered stable and zero, an internal flag is switched on and control of V_{DC} is enabled.

4.3.3 Active power absorption to reach final V_{DC}

When the PLL subsystem has successfully synchronised with the grid, the PI controller in charge of V_{DC} will sense the difference between it and the specified reference voltage $V_{DC_{Ref}}$, and generate a reference signal $i_{d_{Ref}}$ to absorb the necessary active power. The details of the design of this controller can be found in section 5.4.Once V_{DC} is stable at the desired value, a flag than enables the control of the reactive power output is turned on, and steady state operation of the device begins.

4.4 Modifications for prototype implementation

In practice, due to the hardware available at the lab as well as due to a desire to avoid complexity, the built prototype differs from the system that has been

described and simulated in several minor ways.

4.4.1 PLL locking

Ideally, the PLL subsystem should operate at the same time as the rest of the system, in order to adapt to changes in the frequency of the grid and guarantee correct operation. This would require additional voltmeters connected to the grid. To avoid implementing these, the prototype synchronises with the grid while the VSC is operating in rectifier mode and the voltages in each of its phases, which are internally measured and available, are equal to those of the grid, as explained in 4.3.1. Then, the PI controller of the PLL gets disabled and the integrator continues generating the θ output signal without adapting to new potential grid conditions. This makes it essential to feed the integrator with $\omega = 2\pi 50 rad/s$, and trust that the grid frequency is just as likely to go above 50Hz as it is to go below it, and that it never strays either way for long stretches of time thanks to a good frequency control in the grid. This clearly is not a good design for long term operation, since the longer the device is connected the more likely it is that it will desynchronise catastrophically, but it may suffice for short sessions of laboratory testing.

4.4.2 Manual startup resistances

A solid state relay was considered to perform the job of bypassing the startup resistances automatically once they were no longer necessary. This devices can take a small electronic signal, which could be sent from the microcontroller, and open or close as a result, like a mechanical relay would, while being able to sustain large voltages and currents. The main advantage they present over traditional mechanical relays is a shorter actuation time and much lower currents from the control signal, since it is no required to create a strong magnetic field for the switching to take place. However, the high prices of this devices when considering the very limited role they play seems like a waste of money for a testing prototype, so in practice the resistances are gradually reduced to short circuits using sliding levers attached to them.

4.4.3 Three-phase load and Q reference

As mentioned in 4.4.1, there are no voltmeters or ammeters available outside the VSC itself. This means that the process of measuring and calculating the reactive power supplied by the grid to a load and trying to make it zero is not possible. Instead, the physical prototype is directly connected to the grid, and several reactive power references can be given to the PI controller to test how well it can follow

them. In this configuration, the prototype is either a reactive power consumer or generator following reactive power references.

Chapter 5

System Control

5.1 PI controller design

5.1.1 Controller design using open loop frequency response in continuous time

Proportional-Integral (PI) controllers are commonly used in converter designs due to their ability to exactly follow input constant references, unlike P controllers, and being more resistant to the high levels of noise typically found in these systems, which is the main drawback of PID controllers, despite their higher speed. A PI type of controller is designed following the structure shown in figure 5.1. This requires a sufficiently precise model of the plant $P(s)$, in order to generate the appropriate transfer function $C(s)$ to control it. The plant transfer function

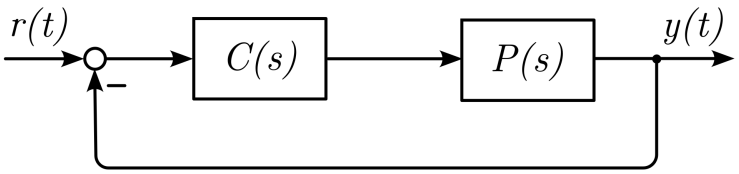

Figure 5.1: Classical controller diagram, where $C(s)$ is the controller transfer function and $P(s)$ is the controlled plant's transfer function.

was obtained from a Simulink model of the three filter inductances, linearized from a state space model. The control transfer function will have the form and

characteristics described by Pagola [16]:

$$C(s) = K_P \frac{1 + Is}{Is} \tag{5.1}$$

Where K_P and I are the tuning parameters proportional and integral control, respectively, and s is the Laplace variable. This control allows independent determination for damping and response speed by setting the desired phase delay φ_C at the selected crossover frequency ω_o. Representing the transfer function as a change in module and a rotation in the complex plane, the relationship between these and the tuning parameters can be obtained:

$$K_P \frac{1 + \omega_o Ij}{\omega_o Ij} = A_C e^{j\varphi_C} \tag{5.2}$$

$$I = \frac{-1}{\tan(\varphi_C)\omega_o} \tag{5.3}$$

$$K_P = A_C \cos\varphi_C \tag{5.4}$$

In order to determine the necessary phase shift to be provided by the control transfer function in order to guarantee the desired total phase margin of the open loop, as well as to ensure that the crossover frequency is the desired ω_o, the influence of the plant must also be taken into account. The final equation used to determine the values of the tuning parameters for a selected total phase margin M_f and a crossover frequency ω_o are:

$$\varphi_C = -180 + M_f - \angle P(j\omega_o) \tag{5.5}$$

$$A_C = \frac{1}{|P(j\omega_o)|} \tag{5.6}$$

Substituting these values into equations (5.3) and (5.4) yields the final value of the tuning parameters.

5.1.2 Discretization of a continuous-time controller

The analysis and design method presented in the previous section only applies to analog systems. However, this project is implemented in a digital microcontroller. This mainly introduces a delay in the feedback path, which will reduce the damping of the system response. To evaluate this effect, the Digital Control notes available to students of this university provide three different case scenarios depending on controller speed, defined by the crossover frequency, and sample time T_s. As mentioned previously in this document, $T_s = 3T_{PWM}$, and the value of ω_o considered

here is 500 rad/s for the reactive power controller and 1500 rad/s for the current controllers. Using the highest of the to, we obtain a value of $\omega_{oi}T_s = 0.45rad$, which results in a loss of $\frac{\omega_{oQ}T_s}{2}\frac{180}{\pi} = 12.89°$ of phase margin. This indicates a medium sample time, which requires using the modified version of the analog controller shown in Figure 5.2

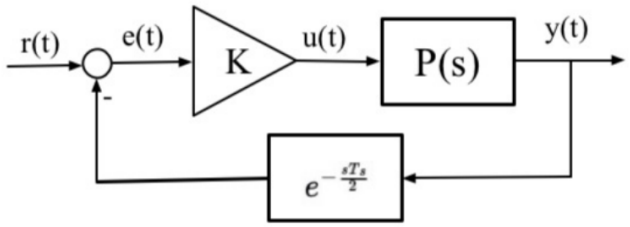

Figure 5.2: Modified analog system for discrete-time controller design

5.1.3 STATCOM PI control loops design

The main controlled variables of the system are V_{dc} and the reactive power output Q. The references for these two controllers are set by the user, and the two controllers in charge of the currents i_d and i_q take their output as their own reference, as seen in Figure 5.3. As shown in chapter 3, V_dc is controlled by increasing the absorbed active power by increasing i_d, while Q depends mostly on the value of i_q if the system is properly synchronised with the grid.

Given the nested nature of the controls and the higher overall relevance of the Q controller, it is the first to be tuned. The current controllers will have to adapt to the requirements of this controller, as will be shown in the next sections. The V_{dc} controller only acts on step inputs during the startup phase, and only keeps the output close to the reference during regular operation, so the requirements for its behavior are not very strict and can be considered after the other three controllers are tuned.

5.2 Reactive power controller

The main point to consider when tuning the controllers is their role in a given electrical grid. A reactive-power-controlling STATCOM, like the one designed in this project, is often used close to industrial sites to compensate for the reactive power consumed by machinery [17]. One of the fastest changes in reactive power usually experienced in these sites happens during the startup of induction motors.

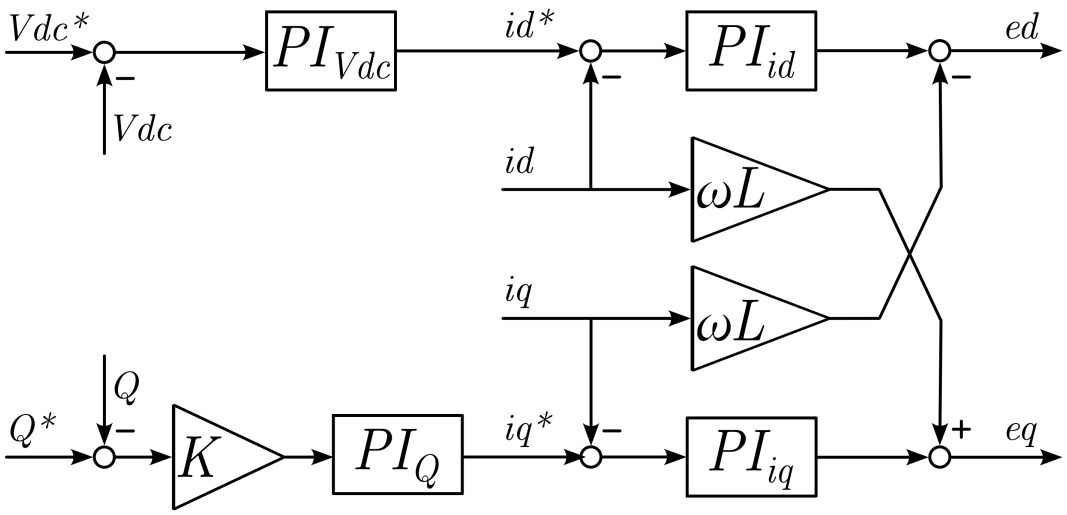

Figure 5.3: Diagram of the four PI controllers and how they feed into each other.

For example, as shown by Garg in [18], a given 400 kW motor was calculated to take 0.3008 seconds to start with no load and 1.474 seconds with a certain torque load. The fastest starting time for one of these motors is still in the hundreds of milliseconds range, while the designed controller comfortably acts in tens of milliseconds, with the final values chosen to allow a settling time of 4.55 milliseconds within 5% of the final value. Even if the controller was used to regulate the voltage of a certain node within a 50 Hz grid, this response time would allow corrections within one quarter of a voltage cycle, significantly faster than even typical fault response devices, which range in the tens of cycles [19].

There are other relevant factors to take into account during design besides speed, e.g., peak response and damping. These would depend on the requirements imposed by the load. Low damping was observed to be associated with stability, with the peak response of most stable configurations not exceeding the steady-state value. The open loop frequency response of the current and reactive power controllers represented in a Nichols chart becomes close to horizontal as the phase approaches -180º, which led to some configurations with ample phase margins becoming unstable due to low gain margins. Pagola [16] recommends a minimum gain margin of 6 dB, but some configurations exceeding this were still unstable. As can be seen in Figure 5.7 and 5.6, the phase margin M_f is the most relevant factor to adjust the gain margin.

Figure 5.6 shows that the three central phase margins have a superior gain margin than those in the lowest and highest extremes. Figure **??** shows a great

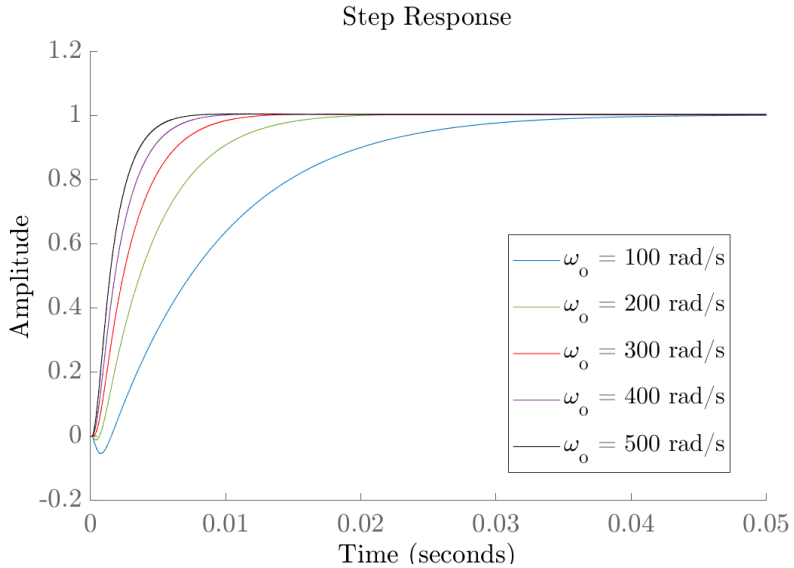

Figure 5.4: Plot of system step responses of the reactive power PI controller for a fixed Mf = 80^{o} using a current controller with a phase margin of 80^{o} and $\omega_{o_i} = 1500 rad/s$

degree of system independence from the selected crossover frequency ω for a given phase margin, a consequence of how close to horizontal the system becomes in a Nichols chart for high values of ω .

This suggests that the highest speed should be chosen, but in practice, the highest speed led to great oscillations in the output. Figures 5.4 and 5.5 were useful when selecting the right values for MF and ω_o, looking to avoid overshooting while obtaining a high speed.

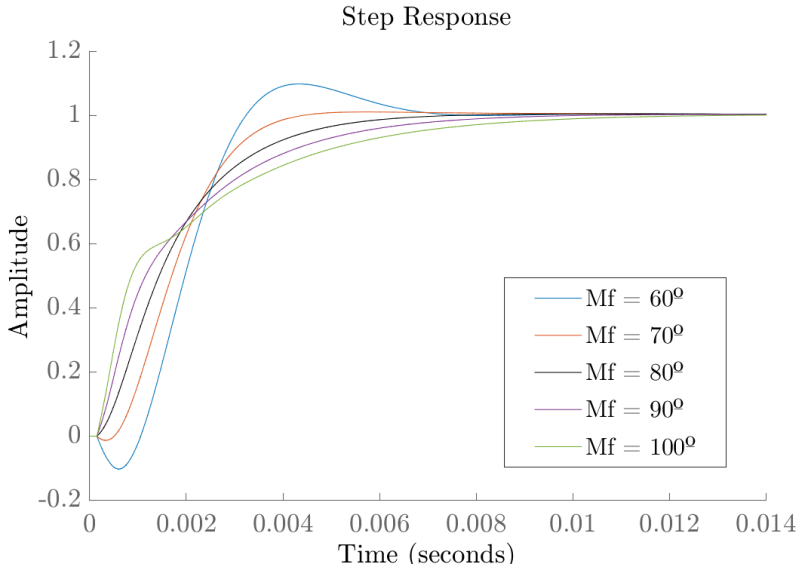

Figure 5.5: Plot of system step responses of the reactive power PI controller for a fixed $\omega_{oQ} = 500 rad/s$ using a current controller with a phase margin of 80º and $\omega_{oi} = 1500 rad/s$

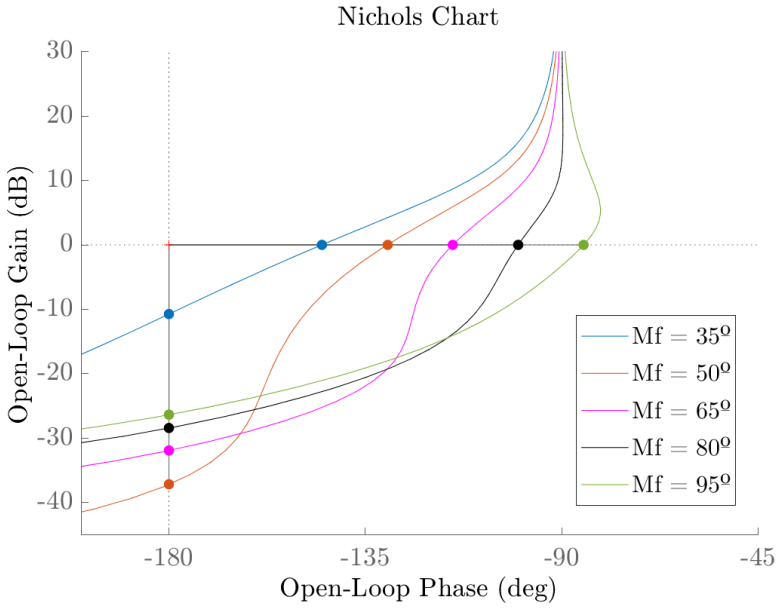

Figure 5.6: Nichols chart of the open loop of the reactive power controller for a fixed $\omega_{oQ} = 500 rad/s$ using a current controller with a phase margin of 80º and $\omega_{oi} = 1500 rad/s$

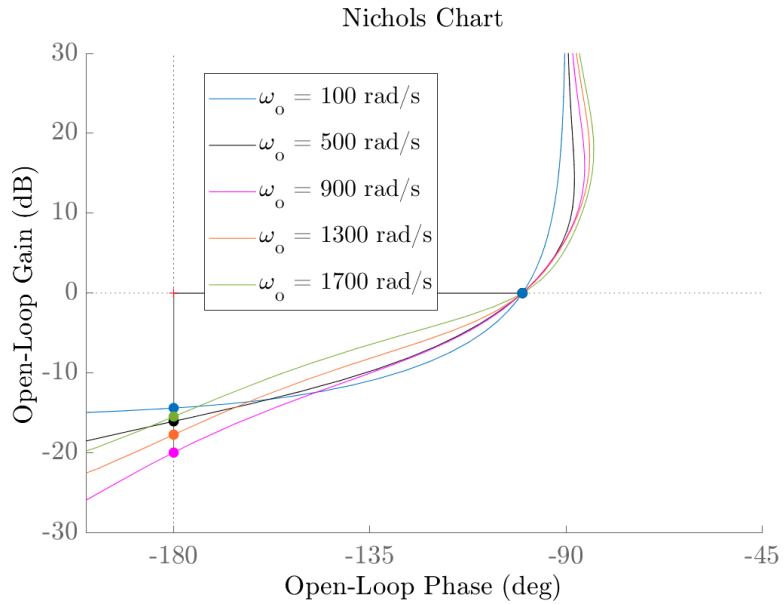

Figure 5.7: Nichols chart of the open loop of the reactive power controller for a fixed Mf $= 80^{\text{o}}$ using a current controller with a phase margin of 80^{o} and $\omega_{o_i} = 1500 rad/s$

5.3 Current controller

The goals for this control are to achieve speed and be as stable as possible in order to guarantee minimal oscillations in the reactive power control loop. These oscillations are related to the overshoot of the step response of the current controller, which is itself related to the system phase margin. The selected value of 80^{o} achieves this, as seen in Figure 5.8.

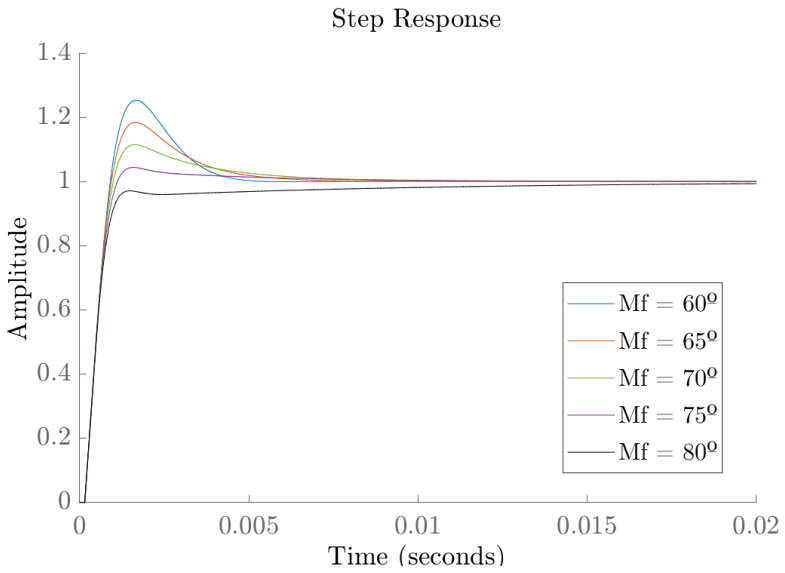

Figure 5.8: Plot of system step responses of the current PI controller for a fixed $\omega_{o_i} = 1500 rad/s$

Figures 5.9 and Figure 5.10 show that the gain margin is mostly dependent on the value of ω_o, decreasing as response speed increases. The selected value of $\omega_o = 1500 rad/s$ guarantees a sufficient gain margin.

This selected speed is compared with those in Figure 5.11 to guarantee there is no overshoot in the step response.

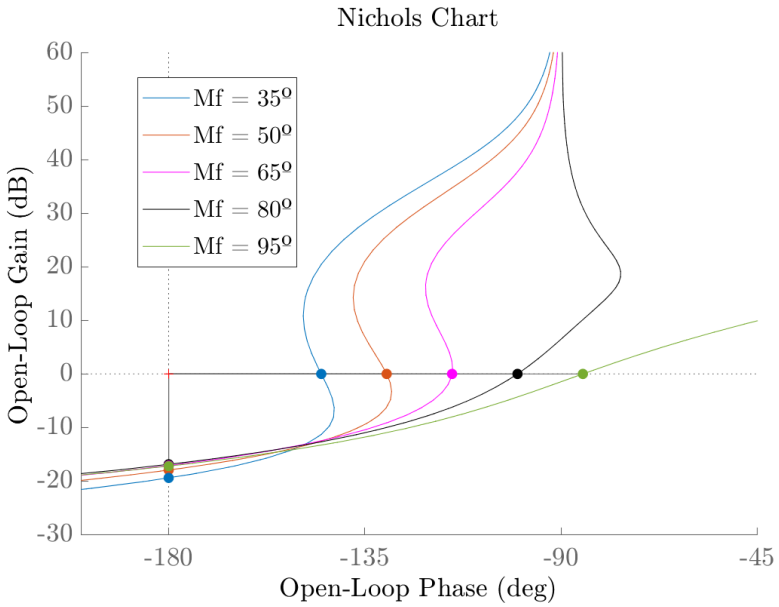

Figure 5.9: Nichols chart of the open loop of the reactive power controller for a fixed $\omega_{o_i} = 1500 rad/s$

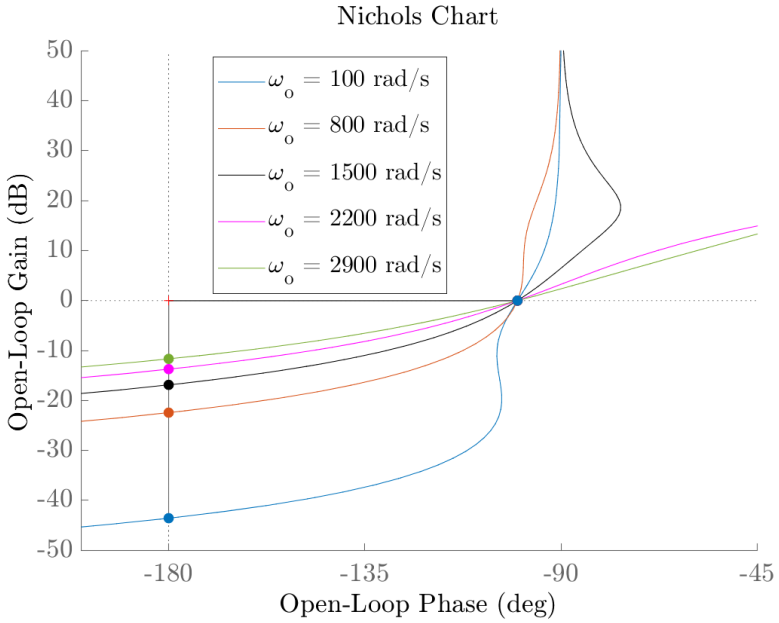

Figure 5.10: Nichols chart of the open loop of the current controller for a fixed Mf = 80º

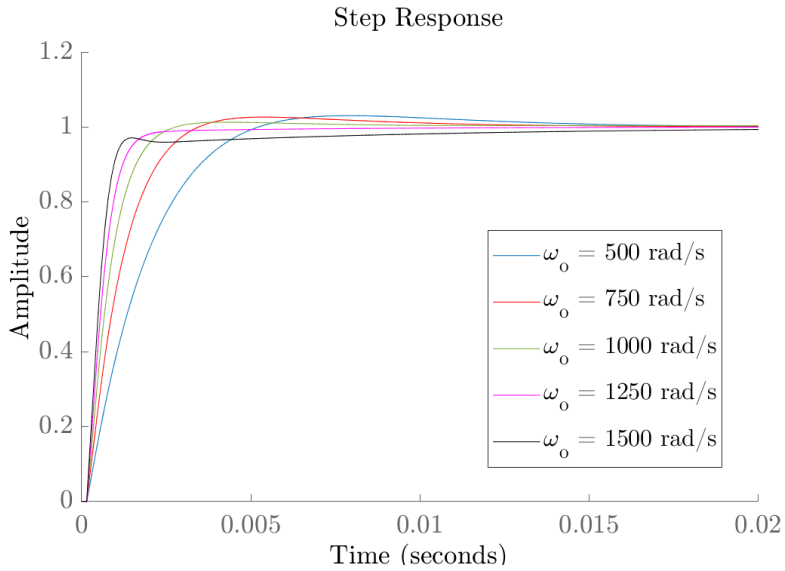

Figure 5.11: Plot of system step responses of the current PI controller for a fixed Mf = 80^o

5.4 DC voltage controller

This controller was the hardest to tune, as it was hard to model due to the non linear relationship between the control variable i_d and the controlled variable, V_{DC}.This relationship can be obtained by equating the active power of the DC side with that of the AC side of the converter after a power invariant Park transformation [20]:

$$V_{DC}^2 = \frac{v_{invd}i_{invd} + v_{invq}i_{invq}}{sC_{DC}} \tag{5.7}$$

Even ignoring that V_{DC} is squared in order to model at least the integration behavior in the transfer function feedback, the resulting model will not be useful. This is because a transfer function with an integrator in its feedback loop can only reach a steady state if the system output, in this case i_d, is zero, which cannot happen in the real model due to the active power losses taking place in the converter. A state space representation of the system could more accurately model this, but given that the only major step input this controller is subject to take place during system startup and steady state being held relatively easily with a wide range of tuning parameter values, it was more practical to test different values in simulation. The starting point of the parameter tuning process where the values obtained for the Q controller, since both of these controllers act before the current controllers and work in a range between one and zero.

The following table shows the final values of the specified and calculated parameters:

Controller	**Mf(º)**	ω_o **(rad/s)**	$\mathbf{K_P}$	**I**
V_{DC}	-	-	5	0.05
i	80	1500	1.31	0.009
Q	80	500	0.0889	$1.69e^{-4}$

Chapter 6

Experimental results

6.1 Simulations

Simulations in the Simulink environment were the main method of testing used to develop the system. All simulation wre carried out using the Runge-Kutta method with a fixed step size of 10 µs, which was found to be a good compromise between precision and simulation speed. Given the complexity of the model, the speed of the simulation could be very slow with smaller step sizes, making the iterative testing process necessary to test several subsystems and situations also unnecessarily slow.

The first test aimed to determine the response of the DC voltage controller, as well as the difference in performance when avoiding the use of the startup resistance. Figure 6.1 shows the capacitor charging process when using the startup resistance. In this test, the system connects to the grid with a 100Ωseries resistance connected in series in each phase.

When 27V is reached, a comparator signal activates a switch that bypasses those resistances. This can be observed in the small step at around 0.16s, when the capacitor reaches the expected steady state value for the rectifier mode, which according to (4.4) is 32.4V for a 24V grid. After this, a comparator subsystem compares the value of V_{DC} with a delayed version of the V_{DC} signal, allowing a margin of 0.1V. When this condition is met, a signal is fed to an integrator module with a specific gain to ensure that the voltage value is truly stable. This prevents unwanted connections like the ones that could happen if the system response had some overshoot, which is not the case here. Once a value of 1 is reached by the integrator, a flag is set on a set-reset flip-flop and another subsystem activates. These flags act as the change of state signals. The flip-flop prevents the flag from turning on and off, as would have happened with the V_{DC} flag right as it triggered had the final flip-flops not been utilized. Once the voltage of the DC capacitor

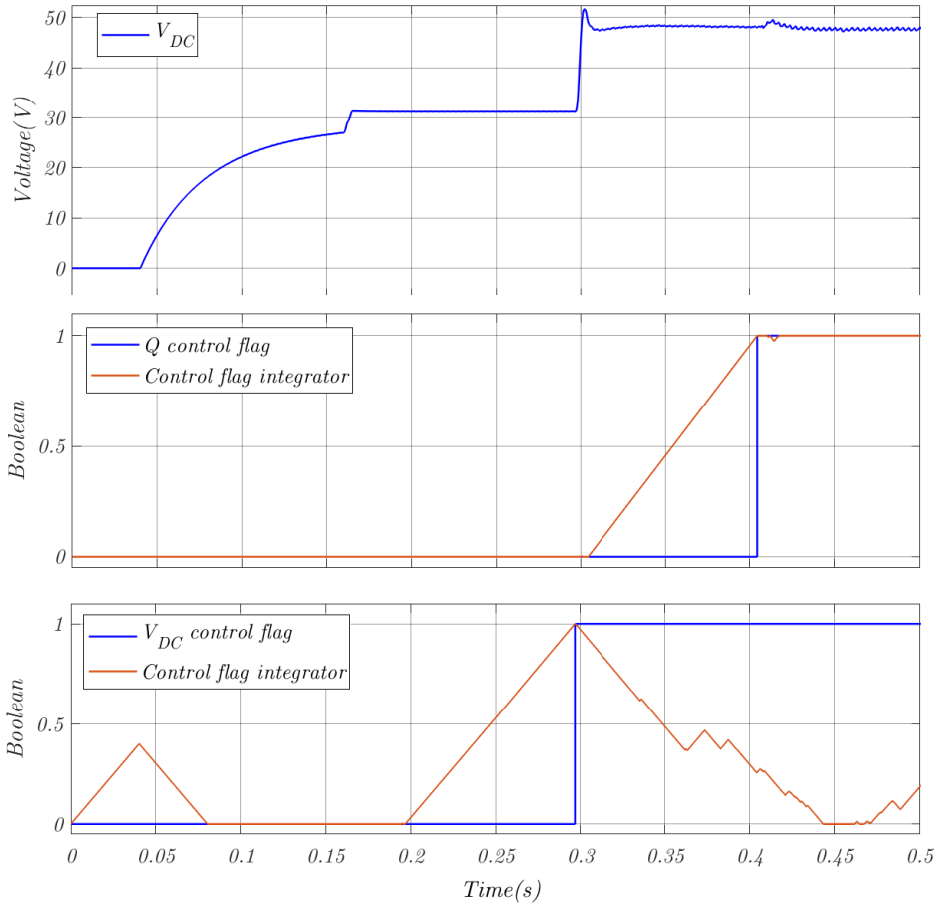

Figure 6.1: Charging process of the DC side capacitor during startup, using the startup resistance during the first stage. The middle and lower subplots show the triggering of the control flags.

is considered stable, the V_{DC} flag goes up and the DC voltage controller drives the the voltage to the specified reference, in this case 48V. Once the 48V has been reached and is stable, the Q control flag goes up and the systems start to compensate for reactive power from the network, or alternatively output a specified commanded reactive power. This second flag only causes a minor disturbance in the DC voltage.

Figure 6.2 shows the evolution of the DC voltage when no startup resistance is used. There is a clear peak in voltage that was prevented by the resistances, as well as a current spike associated with it. However, according to the simulation, this peak remains well within the 80V maximum supported voltage, and even below the desired 48V at steady state. The process of reaching steady state is also longer, but that is a result of the integrator subsystems not being calibrated for this scenario, and they could be tuned to optimize the response.

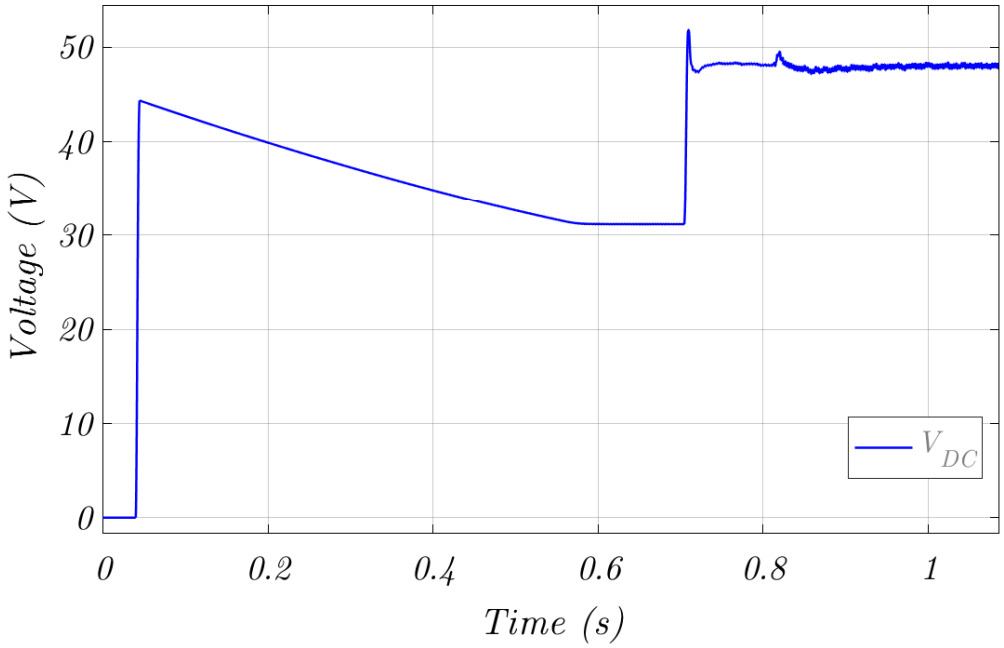

Figure 6.2: Charging process of the DC side capacitor during startup, without the startup resistance.

The next two figures, Figure 6.3 and Figure 6.4, present the system response when tasked with compensating 80VA of reactive power consumption by a load. Figure 6.3 shows the initial active power spike supplied by the grid at the 0.3s mark, when the DC voltage controller is driving the DC voltage to the desired value. More interestingly, it shows the very fast response of the system to compensate the loads reactive power, as well as a raise in active power consumption by the VSC necessary to achieve this. This increase in active power consumption is very important to determine whether power factor correction using this system is worth the investment if the aim is to save energy during transmission. Using this particular load as an example and taking into account the reduction in the

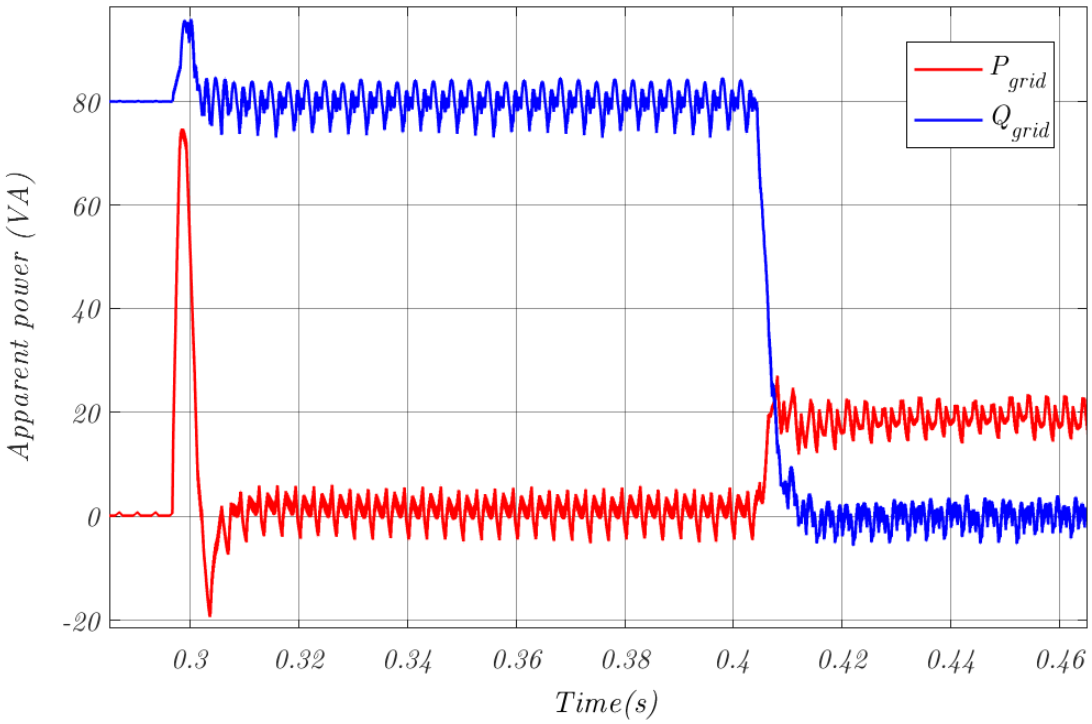

Figure 6.3: Active and reactive power supplied by the grid with an 80 VA inductive load.

magnitude of the currents observed in Figure 6.4, as well as the data provided in [21], an approximation of the minimum length of the transmission lines needed for the system to have a positive impact in energy efficiency can be calculated. 13 gauge copper wire can support a maximum current of 7.4A, and has 6.57Ω/km of resistance. Considering that the system reduced the peak current drawn from 2.8A to 0.8A, the minimum resistance needed is

$$\frac{20W}{\frac{2.8^2}{2} - \frac{0.8^2}{2}} \cdot \frac{1}{3} = 1.85\Omega/phase$$

This means the minimum distance required is $\frac{1.85}{6.57} = 282m$ from the available distribution point. For loads with a significant active power component, the reduction in current becomes much smaller, and more distance is required. Additionally, these calculations assume that the step-down transformer is located at the farthest point from the system, connected directly in the intersection with the grid. If the transmission to the point where the VSC is located is carried out at higher voltages, the transmission currents are minimal, and much longer distances are

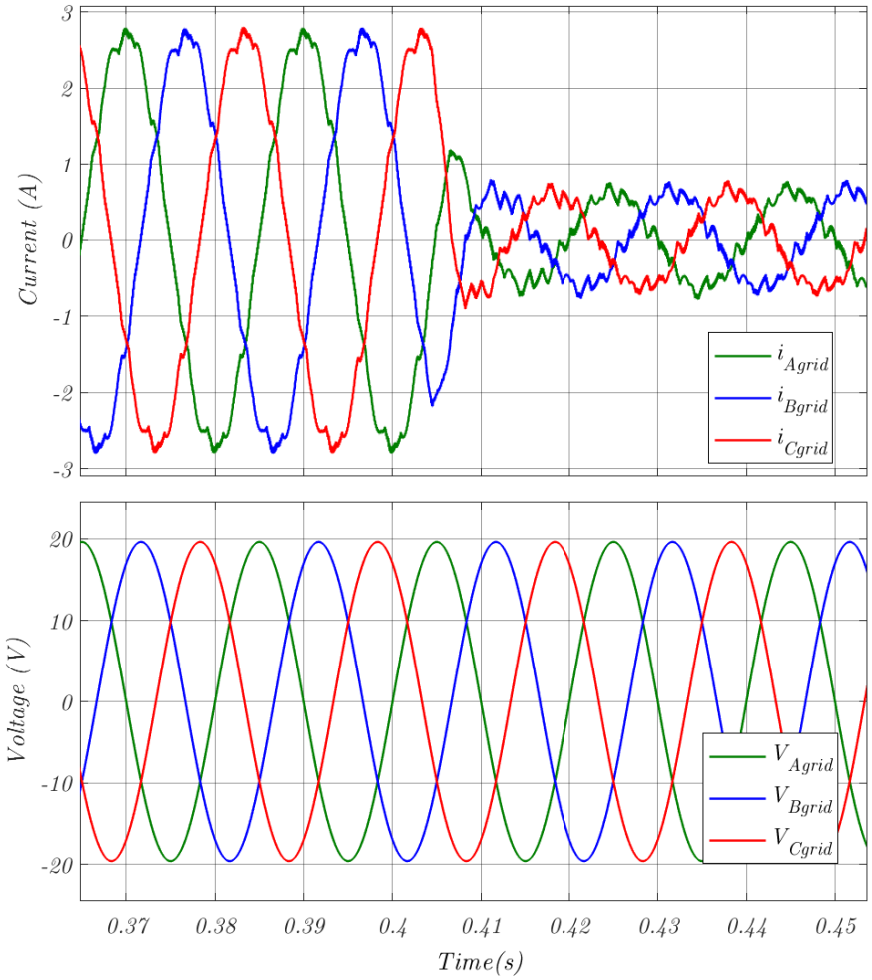

Figure 6.4: Grid voltage and current with an 80 VA inductive load.

needed. This shows that such a system has to operate at the available grid voltage and avoid using a transformer in order to increase energy savings.

For the last test, step inputs in the DC voltage and reactive power references to observe the system response to them. Figure 6.5 shows that the DC voltage controller can follow a 5V variation in its reference very fast and with minimal overshoot, being, in fact, more sensitive to changes in the reactive power reference.

Figure 6.6 shows the effective system response to the step in grid reactive power reference. This reactive power is referred to as the grid, so a positive reference requires a control signal i_q with the opposite value. Given that the converter is considered in generator mode in this reference frame, a positive Q reference requires the grid to absorb reactive power, so the converter must

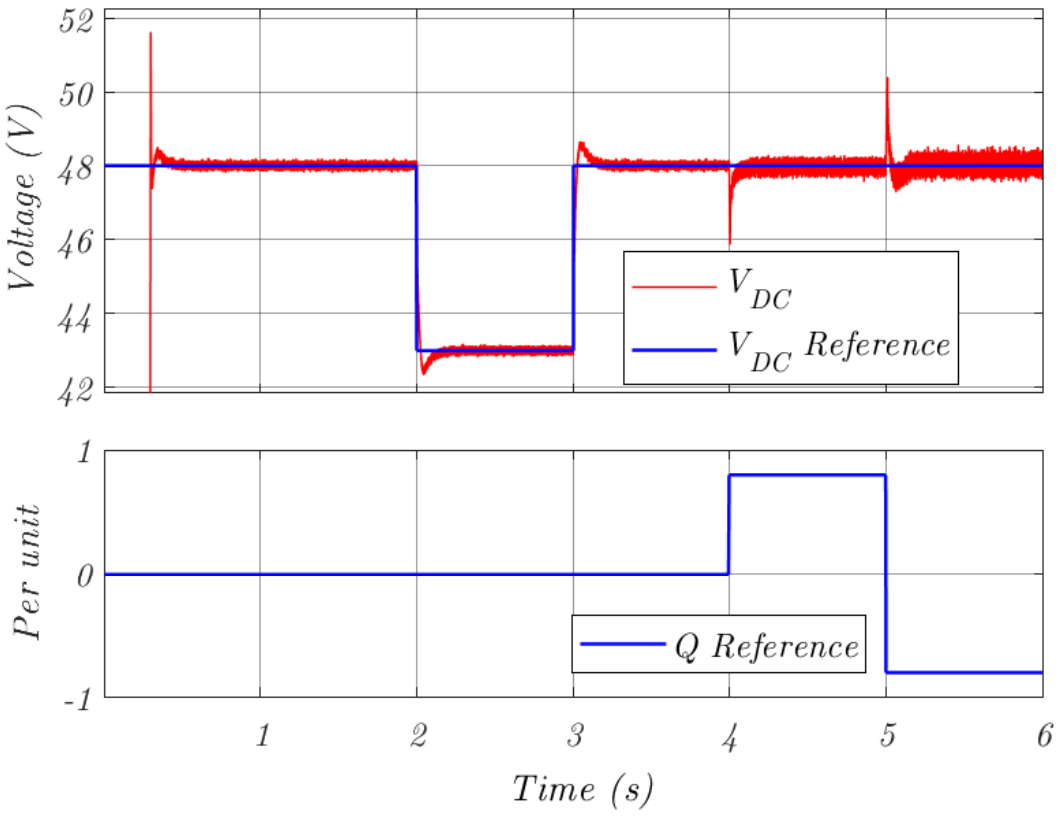

Figure 6.5: DC voltage response to steps in DC voltage reference and reactive power reference.

Finally, Figure 6.7 shows the response of the q-axis component of the current to the step given by the Q controller in the previous test.

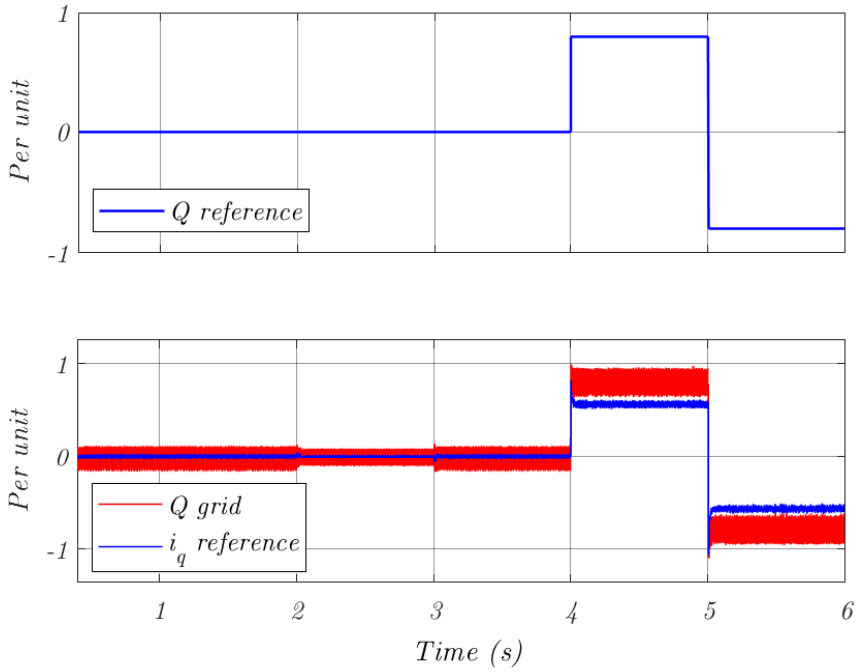

Figure 6.6: Grid reactive power response to steps in DC voltage reference and reactive power reference.

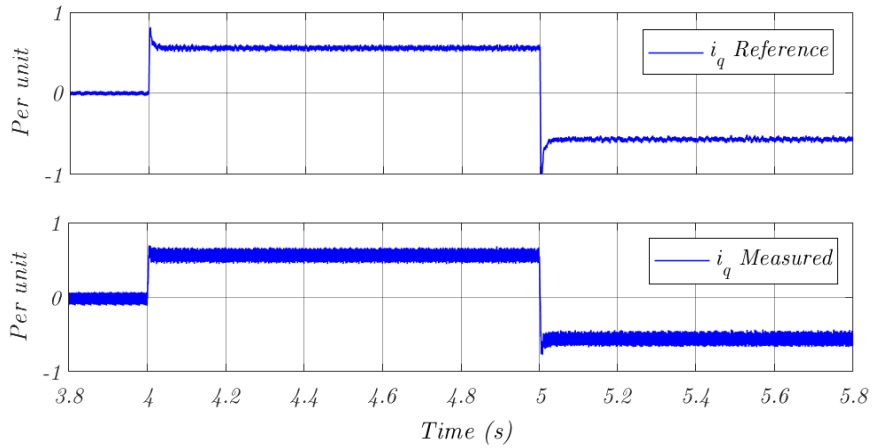

Figure 6.7: q-axis current output response to a step in current reference.

6.2 Prototype testing

Figure 6.8 shows the setup used for testing in the laboratory. The transformer placed to step down the three-phase voltage is composed of three independent single-phase 220/24V transformers. To achieve a three-phase line to line 220 V/24 V, a STAR-STAR configuration was utilized. The first test involved measuring the

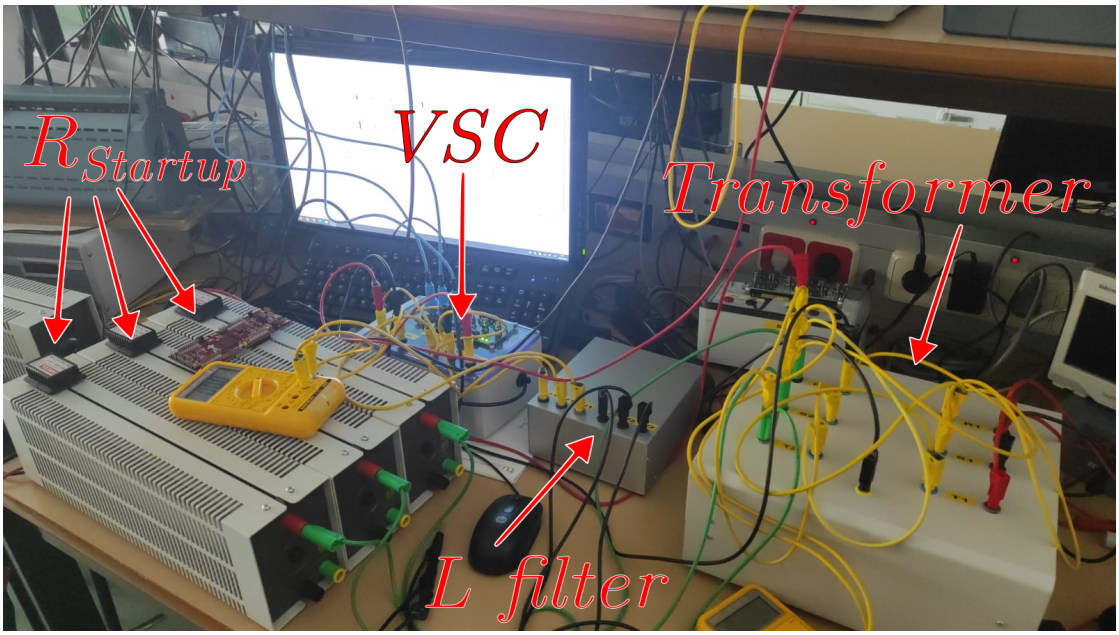

Figure 6.8: Prototype setup used for laboratory tests.

three-phase grid voltages to ensure the stability of the network, on which the stability of every other element depends. As expected, it was found to be satisfactory most of the time, but some distortion appeared occasionally in the oscilloscope. Figure 6.9 shows one such incident. The origin of these distortions is beyond the scope of this project and they were ignored. The next test aimed to observe the effect of the startup resistance in the charging of the DC-side capacitor. This is because, during simulation, it was observed that not using a startup resistance would result in a peak in the response which would be higher than steady state, but still well within the range of voltage supported by the capacitor. Not using the startup resistances would simplify the startup process and improve power efficiency. For the 24V present at the secondary of the transformer during these tests, a DC voltage $V_{DC} = 1.35 \cdot 12 = 32.4V$ was expected according to the analysis presented by Mohan [1]. According to the same author and as explained in section 4.3, the worst case scenario for the peak voltage would be $V_{DC} = 2 \cdot \sqrt{2} \cdot 12 = 67.9V$, still

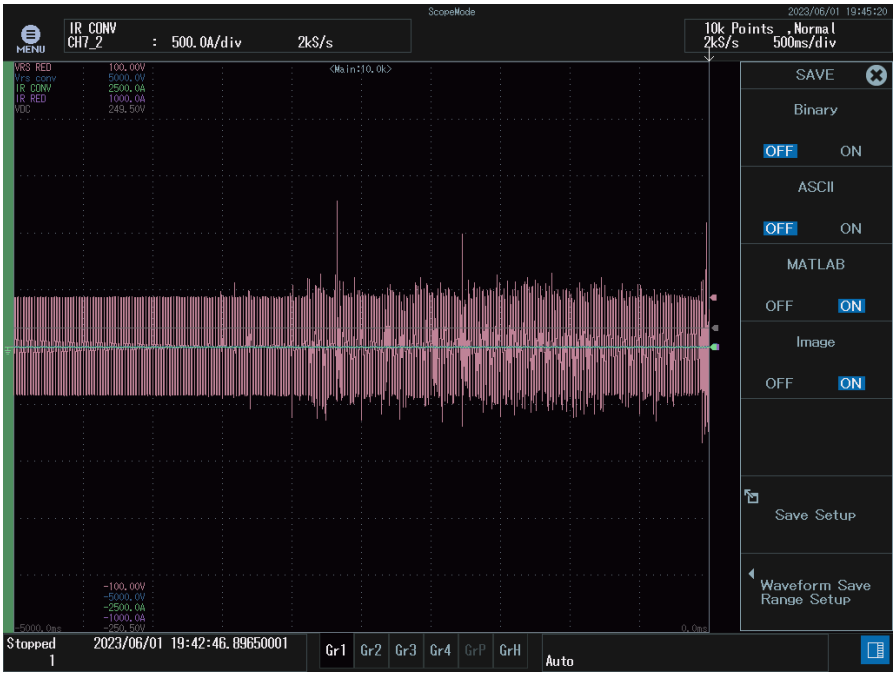

Figure 6.9: Oscilloscope capture of the three-phase grid displaying anomalous waveforms.

within the 80V maximum. Figure 6.10 shows the DC voltage response with no startup resistances. In this case, the peak was much smaller than the theoretical maximum, and the steady state was achieved at 15.15V. Figure 6.11 shows the damped response using the startup resistance, with a steady state DC voltage of 14.71V. The currents during steady state are small, but they still generate voltage drops the average voltage in the steady state, resulting in a lower voltage than the one observed when no startup resistance was used. These values are far from the ones predicted, due to the fact that the converter was not actually working in rectifier mode. In any case, the difference in the shape on the signal caused by the presence of the startup resistance can still be observed.

In the next action taken in the laboratory, a connection with the startup resistances at their maximum value was attempted, but the value of V_{DC} reached was just 5V. Moving the sliders to reduce the resistance did not seem to increase the DC voltage. When the sliders reached the end of the track and the resistance was close to 0Ω, a large voltage spike that reached 48V was observed. The converter showed an anomalous behavior, and all signals, including the other test signals that can be observed in Figure 6.12, moved to zero values.

The unresponsiveness to the lowering of the series resistance, as well as the converter tripping at a voltage much lower than the maximum rate, suggest that

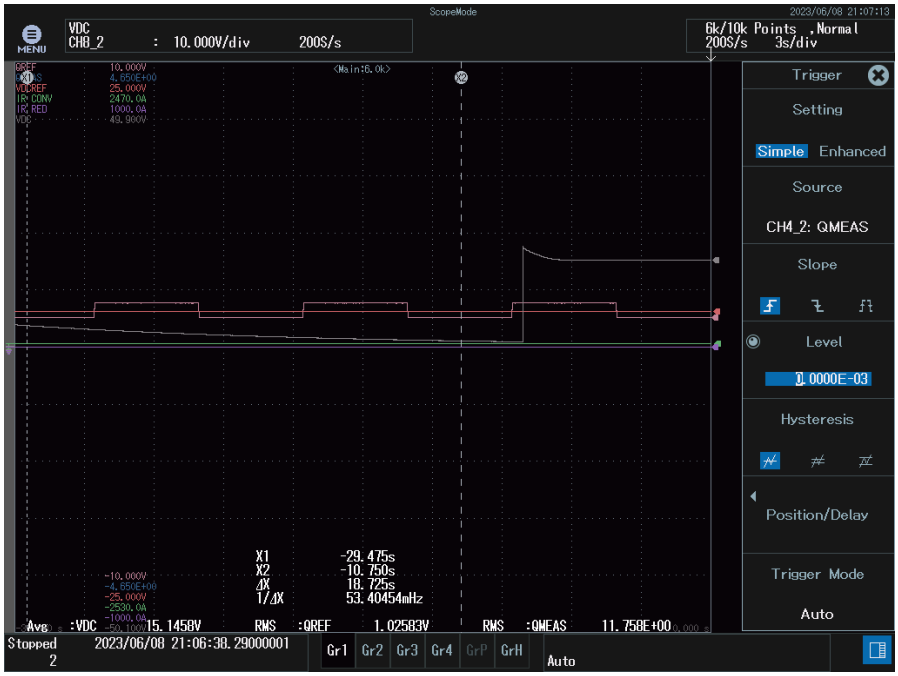

Figure 6.10: Oscilloscope capture of DC capacitor charging when connecting to the grid and without the startup resistance (grey trace).

some internal circuit must have been preventing the charge of the capacitor. All attempts to fix this problem failed, even with other VSCs so no more tests could be carried out.

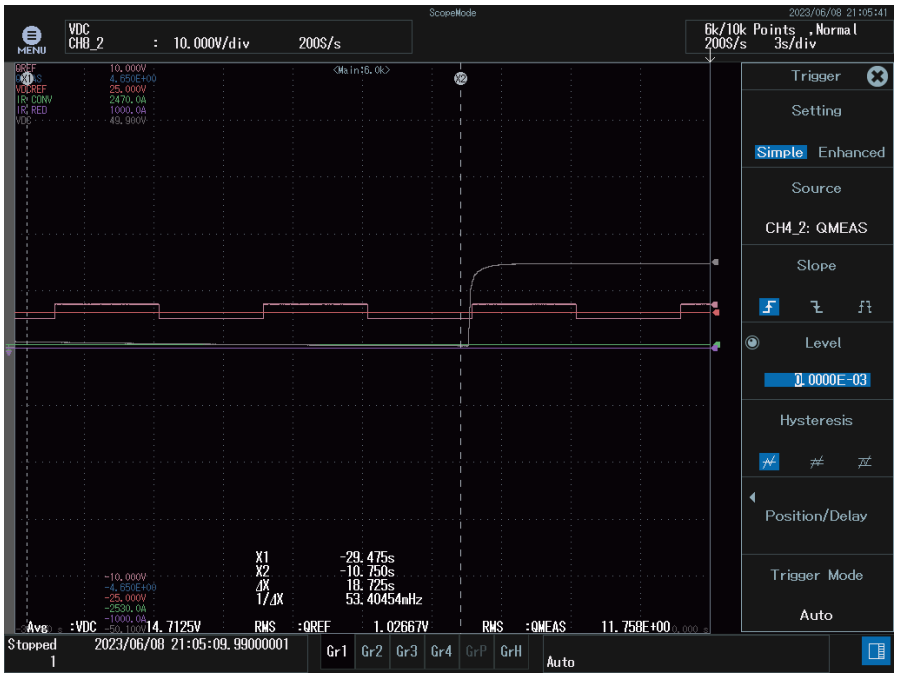

Figure 6.11: Oscilloscope capture of DC capacitor charging when connecting to the grid and with a startup resistance of 100Ω(grey trace).

Figure 6.12: Oscilloscope capture of the incident in which a VSC tripped.

Appendix A

Alignment with UN Sustainable Development Goals

The technology used for the development of this project is playing a key role in the worldwide transition to clean energy sources, and this role is only likely to increase in the future. This makes the project particularly aligned with goal 7, which aims to ensure affordable, sustainable, reliable and modern energy for all. The transition to renewable energy sources is also tied to goal 13, related to actions that contribute to stop climate change.

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