COMILLAS
UNIVERSIDAD PONTIFICIA
ICAI ICADE CIHS

Syllabus
2025 - 2026

GENERAL INFORMATION

Data of the subject	
Subject name	Digital Electronics
Subject code	DEA-GITI-341
Mainprogram	Bachelor's Degree in Engineering for Industrial Technologies
Involved programs	Grado en Ingeniería en Tecnologías Industriales [Third year]
Level	Reglada Grado Europeo
Quarter	Semestral
Credits	6,0 ECTS
Type	Obligatoria (Grado)
Department	Department of Electronics, Control and Communications
Coordinator	Fermín Zabalegui Sanz
Office hours	Upon request

Teacher Information	
Teacher	
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DESCRIPTION OF THE SUBJECT

Contextualization of the subject

Prerequisites

A basic knowledge of analog electronics circuits is needed for this course

Course contents

Contents

Theory

Introduction to Digital Techniques

- Bits and logic levels
- Digital circuits technologies
- Digital design levels

Boolean Algebra

- Boolean algebra's definitions and theorems
- Non-primary logical functions
- Normal form of a Boolean function
- Simplifying Boolean functions using Karnaugh maps (K-maps)

Numeral Systems and Codes

- Positional numeral systems
- Base conversion
- Ranks and representation
- Hexadecimal and octal systems

Mathematical operations with binary numbers

- Representing whole numbers
- Ranks and representation of signed numbers
- Mathematical operations with signed numbers
- Other binary codes

Introduction to Hardware Description Languages. VHDL

- Design flow
- File structure
- Examples
- Data types, constants and operators
- Concurrent statements

Arithmetic Circuits

- One-bit adder
- N-bit adder
- N-bit subtractor
- N-bit adder-subtractor
- Multipliers
- BCD adder

Combinational Logic Design

- Multiplexers
- Demultiplexers
- Encoders
- Decoders
- Comparators

Sequential Circuits Fundamentals

- Introduction to sequential logic
- Basic concepts
- Bistables

Digital Circuits Timing

- Introduction
- Timing hazards
- Synchronous design
- Technical parameters of bistables
- Synchronous design and clock period
- Clock skew and distribution
- Asynchronous input synchronization

Finite-State Machines

- Definitions – Mealy and Moore machines
- Design of finite-state machines
- VHDL definition
- Sequence detector
- Sequence detector with edge detectors

Registers

- Introduction
- Parallel registers
- Shift registers

Counters

- Binary up counter
- Binary down counter
- Up / down counters
- Counters with enable
- Mod M counters
- Cascaded counters
- Counters with load input
- Arbitrary sequence counter

Complex Digital Design: Datapath + Control Unit

- Introduction
- Parking barrier control
- Binary to BCD converter
- SPI connections

Memories

- Introduction
- Static RAMs

- Dynamic RAMs
- ROMs
- Examples

Laboratory
Laboratory practice units
P1. Introduction to digital gates and digital oscilloscope. P2. Introduction to designing with schematics and compilation. P3. Introduction to simulation and physical design. P4. Combinational digital circuits with VHDL. P5. Arithmetic circuits. 5 bits adder. P6. Arithmetic circuits. 5 bits multiplier. P7. Arithmetic circuits. 5 bits ALU. P8. Introduction to latches and flip-flops. P9. Digital design. The electronic lock. P10. Digital design. The parking control. P11. Digital design. Microwave timer.

EVALUATION AND CRITERIA

The use of AI to produce full assignments or substantial parts thereof, without proper citation of the source or tool used, or without explicit permission in the assignment instructions, will be considered plagiarism and therefore subject to the University's General Regulations.

Evaluation activities	Evaluation criteria	Weight
Theoretical exams: • Final exam • Midterm exam	• Knowledge of concepts. • Resolution of practical problems. • Analysis and interpretation of the results. • Presentation and written communication.	54
Class tests • Two class tests during the semester	• Knowledge of concepts. • Resolution of practical problems. • Analysis and interpretation of the results.	6
Laboratory practices: • 11 units of digital electronics laboratory practices Practical exam	• Application of concepts to the resolution of practical problems. • Realization of practices in the laboratory. • Analysis and interpretation of the results obtained in laboratory practices. • Work in groups. • Presentation and written communication.	40

Grading

Theoretical (ordinary period)

The normal period evaluation/grading is composed by:

- Two class tests (30 minutes maximum). The average mark of both exams is ***nc***.
- One midterm exam: ***ni***.
- One theoretical final exam: ***ne***.

The theoretical final grade ***nt*** is:

nt = 0,7 • ***ne*** + 0,2 • ***ni*** + 0,1 • ***nca***

A minimum mark of 4/10 is needed in the final exam (***ne***), otherwise ***nt*** will be the lowest mark between ***ne*** and the calculated mark ***nt***.

Practical (ordinary period)

The normal period evaluation/grading is composed by:

- Final practical exam: ***nex***.
- Laboratory practices, which include previous work, circuit designing and implementation and final documentation. The average mark of the 11 practices is ***np***.

nlab = 0,5 • ***nex*** + 0,5 • ***np***

A minimum mark of 4/10 is needed in the final exam (***nex***), otherwise ***nlab*** will be the lowest mark between ***nex*** and the calculated mark ***nlab***.

In order to pass the course, attendance to laboratory sessions is compulsory.

Final grading (ordinary period)

In order to pass the course, both ***nt*** and ***nlab*** marks must be greater or equal to 5/10. If this condition is met, the final mark is:

nfinal = 0,6 • ***nt*** + 0,4 • ***nlab***

Otherwise, the final mark will be the lowest between ***nt*** and ***nlab***.

Extraordinary (re-sit) exam

In the case the theoretical or practical (laboratory) part has not been passed in the normal period, a re-sit theoretical exam and/or practical exam will be required.

If the theoretical part is failed, there will be a re-sit theoretical exam: ***njt.*** The mark for the theoretical part will be:

nt = 0,8 • ***njt*** + 0,1 • ***ni*** + 0,1 • ***nc***

(***ni***: midterm mark, ***nc***: average class tests mark)

A minimum mark of 4/10 is needed in the exam (***njt***), otherwise ***nt*** will be the lowest mark between ***njt*** and the calculated mark ***nt***.

If the practical part is failed, there will be a re-sit practical exam: ***njl.*** The mark for the practical part will be:

nlab = 0,8 • ***njl*** + 0,2 • ***np***

(***np:*** average mark of the laboratory practices)

A minimum mark of 4/10 is needed in the exam (***njl***), otherwise ***nlab*** will be the lowest mark between ***njl*** and the calculated mark ***nlab***.

In order to pass the course, both ***nt*** and ***nlab*** marks must be greater or equal to 5/10. If this condition is met, the final mark is:

nfinal = 0,6 • ***nt*** + 0,4 • ***nlab***

Otherwise, the final mark will be the lowest between ***nt*** and ***nlab***.

Attendance rules

Class attendance is mandatory, according to the Academic Regulations of the Higher Technical School of Engineering (ICAI). The requirements of attendance will be applied independently for theory and laboratory sessions:

- In the case of theory sessions, failure to comply with this rule may prevent them from taking the exam in the ordinary period.
- In the case of laboratory sessions, failure to comply with this rule may prevent you from taking the exam both in the normal and re-sit period.
- In any case, unjustified absences from laboratory sessions will be penalized in the evaluation.

AI Usage Regulations

- **Midterm Tests and Theory and Laboratory Examinations.** The use of generative artificial intelligence models or programming assistants is strictly prohibited during any assessment activity, whether in-person or remote. These activities must exclusively reflect the student's individual knowledge and work.
- **Laboratory Practices and Projects.** The use of AI-based programming assistants and generative language models is permitted under the following conditions:
  - They may be used as support to understand technical concepts, obtain suggestions on how to approach proposed exercises, and generate code fragments or initial drafts of reports.
  - The use of these tools must be complementary and never substitute individual work. Presenting automatically generated content as one's own without having understood, reviewed, and properly adapted it is not permitted.
  - Any relevant content generated wholly or partially through these tools must be explicitly cited, clearly indicating which part has been obtained by this means and in which tool it was generated. The sequence of queries (prompts) used shall be included as an appendix at the end of reports.
  - Professors reserve the right to ask oral questions about content generated with AI assistance. The inability to explain or justify such content may negatively impact the activity grade.
- The responsible use of these tools as support for individual study is encouraged —for example, to clarify concepts, generate new exercises, or receive corrections—. However, it is reminded that **responses generated by AI models may contain errors**, and it is the student's responsibility to analyze them critically.

WORK PLAN AND SCHEDULE

Activities	Date of realization	Delivery date
Understanding the theoretical contents in the textbook	After theoretical classes	

Solving the proposed exercises	Weekly	
Studying and preparation for the class tests that will be carried out during the term	Weeks 6 and 10 (3rd week after midterm exams)	
Preparation of the final theoretical exam	Weekly and class session in April	
Writing of the laboratory reports for each practice unit	Weekly	A week after the laboratory practice

BIBLIOGRAPHY AND RESOURCES

Basic References

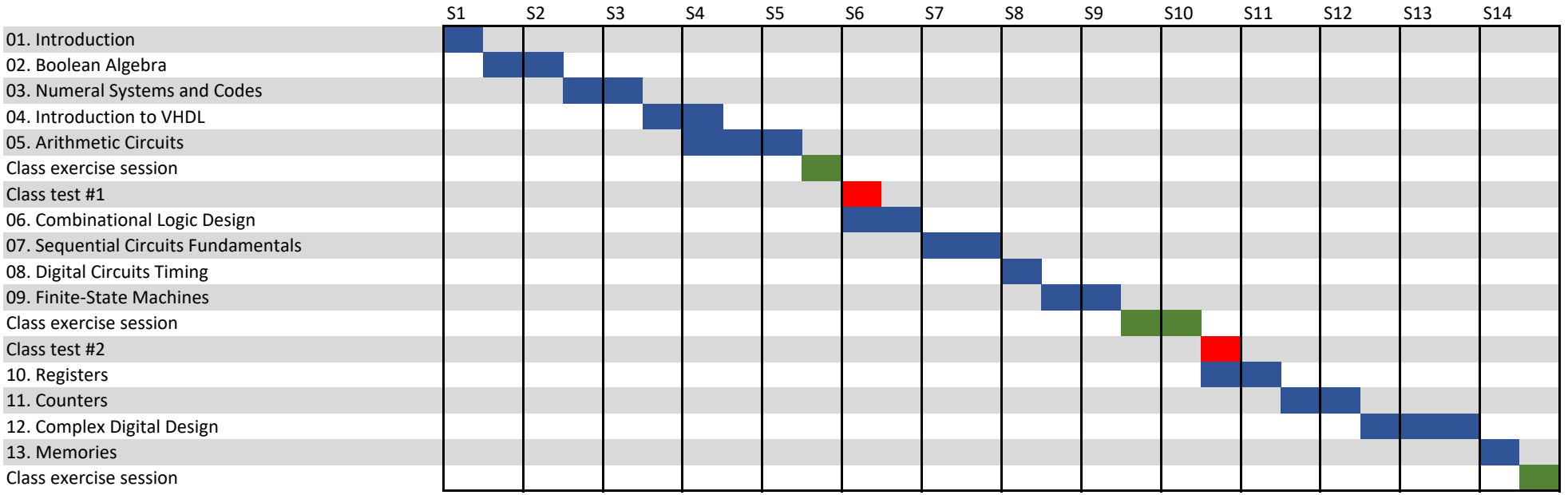
- Jose Daniel Muñoz Frías. **Introducción a los sistemas digitales. Un enfoque usando lenguajes de descripción de hardware**. (Introduction to digital systems. An approach using hardware description languages. (2011) (January 2023 edition)

Complementary References

- John F. Wakerly. **Digital Design: Principles and practices.** Prentice Hall. 2000. (4th edition)
- Thomas L. Floyd. **Digital Fundamentals**. Pearson/ Prentice Hall. 2006. (11th edition)

Digital Electronics: indicative schedule (2025 / 2026)
3º GITI

Theory schedule



Laboratory schedule