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TRABAJO FIN DE MÁSTER

Design, manufacturing and test of the On-Board Computer for DTUSat-3

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MADRID, 19 de enero del 2020

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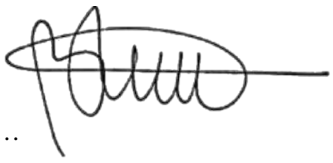

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Preface and acknowledgments

This Master Thesis concludes the Double Degree Program in Industrial and Electrical Engineering between the Comillas Pontifical University (ICAI) and the Technical University of Denmark (DTU). This thesis represents a workload of 30 ECTS points and it was developed at DTU Space between August 2019 and January 2020. This report is a result of the design, implementation and testing of the On-Board Computer for the next generation of DTUSat satellites, DTUSat-3, and contains figures and tables to illustrate and underline the results.

First of all, I would like to thank especially my supervisors, René Fléron and Denis Tcherniak, for giving me the chance to do this project, for guiding me throughout all of it and for being always available to answer my questions.

Another big thanks goes to Julia Sushkova, from DTU Space, for helping and assisting with the X-ray images, and to Torben Esmann Mølholt and Nina Jensen, from DTU Nutech, for facilitating the radiation testing. Also, thanks to the rest of the DTUsat team for asking the right questions and providing constructive feedback.

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Kgs. Lyngby, January 2020
Blanca Alejo Gago

Abstract

During this Master Thesis a PCB for the On-Board Computer of DTUSat-3 has been designed, manufactured and tested. The developed board complies with all the requirements of the satellite, runs in Linux and uses COTS components. In this report, the development of the circuit schematics and PCB layout in KiCad as well as the process of soldering the components are described. Moreover, the board is subjected to several tests and qualifications in order to identify its potential failure modes and its susceptibility to ionizing radiation dose effects. Finally, it is discussed how the designed OBC meets the desired specifications and methods for optimizing the PCB layout, mitigating identified issues and other topics for future work are suggested.

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Chapter 1

Introduction

DTUSat is a long-running project from the National Space Institute at the Technical University of Denmark which aims at building a CubeSat satellite that can be used for scientific research. DTUSat involves mainly students, but also employees, from different departments and specializations, which makes it an interdisciplinary project. Furthermore, DTUSat provides students with the chance of participating in the design and development of a satellite, thus unifying the two major goals of the university: research and education (DTU, 2010).

The physical product of the DTUSat project is a picosatellite that complies with the CubeSat specifications (The CubeSat Program, 2014). CubeSats are small cubic satellites that have several limitations, among them the size and weight, which are summarized in Table 1.1 (Hansen and Appel, 2009). Thanks to their small size and low weight, CubeSats are allowed on larger commercial launches, which reduces the cost of the launch and also makes it possible to choose from a wide range of available launches and orbits.

CubeSat structure	Size constraint	Mass constraint
1U	10 x 10 x 10 cm	1 kg
2U	10 x 10 x 20 cm	2 kg
3U	10 x 10 x 30 cm	3 kg

Table 1.1: CubeSat specificiations.

DTUSat has already launched two satellites: DTUSat-1, in June 2003, and DTUSat-2, in June 2014. Currently, the next generation of DTUSat is being developed. DTUSat-3 aims at developing a satellite that is modular, reusable and easy to program for students, as well as low-cost using Commercial Off-The-Shelf (COTS) components, which correspond to those components for which the manufacturer establishes and controls the specifications without additional requirements imposed by external users (NASA, 2014), i.e. commer-

cialized components that were not designed specifically for the space environment.

DTUSat-3 will be formed by several subsystems or modules, such as an Electric Power System and an Attitude Control System. One of the most important subsystems is the On-Board Computer (OBC). The OBC is the brain of the satellite, it is responsible for monitoring and controlling every function of the satellite as well as for implementing control laws (European Space Agency, 2015). The OBC will have to communicate with all the other subsystems and therefore needs to comply with the mechanical and electrical interfaces of the carrier board in which it will be mounted. Moreover, the OBC controls and commands all operational capabilities of the satellite, which include payload operations, subsystem activation/deactivation and attitude maneuvers among others (DTUSat, 2006). This way, the OBC needs to be able of communicating with the rest of the subsystems in the satellite as well as storing data, such as the main application.

This way, the objective of this Master Thesis is to design, manufacture and test such an On-Board Computer for DTUSat-3 that complies with all the requirements of the satellite and the mission.

1.1 DTUSat-2

DTUSat-2 is the precursor of DTUSat-3 and provides a base from which to start developing the new satellite. Therefore, it is important to understand the context of DTUSat-2 as well as the specific requirements and how they were fulfilled.

DTUSat-2 aimed to implement a spaceborne radio-tracking system capable of locating small birds on intercontinental migration routes. The experiment targeted common Cuckoos (*Cuculus canorus*) with the purpose of demonstrating the navigational mechanisms employed by these birds. It was successfully launched in June 2014 into a Sun-synchronous orbit, with a nominal altitude of 630 km and an inclination of 98°, and it was expected that the mission lasted for 18 months (EoPortal Directory, 2015). However, communication with the satellite could not be established, and has remained that way ever since. The reason for this failure lies on a permanently-damaged on-board battery as a consequence of a deep discharge, which made it impossible for the On-Board Computer to boot correctly. This could have probably been prevented if more time had been dedicated for system integration and testing (Fléron, 2019).

The primary payload on board DTUSat-2 consists of a radio system capable of receiving radio signals from transmitters mounted on birds, which contain GPS position data, and then transmitting them to a ground station. Furthermore, DTUSat-2 has a secondary payload which consists of a PICOCAM subsystem tasked with producing Earth images (DTUSat, 2006). PICOCAM is a small CCD imaging system, developed at DTU, which is specifically designed for CubeSats where there are limited power production capabilities (EoPortal Directory, 2015).

Finally, Table 1.2 summarizes the mechanical and electrical specifications for DTUSat-2 (DTUSat, 2007).

Maximum mass	1 kg
Dimensions during launch	10 x 10 x 11.3 cm
Power bus voltage	3.3 V
Available power	700 mW

Table 1.2: DTUSat-2 specifications.

On-Board Computer

The On-Board computer for DTUSat-2 is built around a distributed architecture (Benn, 2005) in which each subsystem is allowed to have a local microcontroller that handles all the interactions and communications. This architecture improves modularity, since each subsystem is almost completely independent of the rest of the subsystems from a hardware point of view (Aalbers and Gaydadijev, 2006). Furthermore, the satellite utilizes a CAN based bus system to communicate and transfer data between the subsystems.

The OBC for DTUSat-2 comprises a number of physical elements supporting different operations (DTUSat, 2006), which include:

- Main processor: based on the ARM7 core embedded in a Philips LPC2292 processor operating at a frequency of 4.7456 MHz. It features two internal CAN bus controllers, two UART communication interfaces and two SPI bus controllers.
- Power distributor system: which generates the voltages necessary for the correct functioning of the OBC.
- External memory bank: composed of a 4Mb Flash block, a 2Mb SRAM block and a 32kb PROM block.

– Data mass storage: which increases the storage capacity of the OBC.

Furthermore, the OBC supports two operational modes for DTUSat-2: Safe mode and Nominal mode. The purpose of the first is to ensure that the satellite reverts to a known fail-safe state in the event of a malfunction, while the later is considered the main operational mode of the satellite. When the satellite operates in Safe mode, only the basic OBC functions are available, thus non-vital systems are shutdown (DTUSat, 2006). When the satellite operates in Nominal mode, the OBC executes the main application.

Finally, Table 1.3 summarizes the mechanical constraints and power budget for the OBC of DTUSat-2.

Maximum mass	45 g
Maximum dimensions	83 x 53 x 12 mm
Maximum component height	5 mm
Available power	150 mW

Table 1.3: DTUSat-2 OBC mechanical constraints and power budget.

Radiation tolerance

DTUSat-2 employs aluminum side panels with a thickness of 1.5 mm, which provide some protection from the ionizing radiation present in the space environment. However, this protection is limited, therefore all the satellite subsystems were imposed with a radiation tolerance requirement of 10 krad accumulated over the mission lifetime. This means that all the subsystems, including the OBC, had to be capable of functioning in such high radiation environment without infringing the requirements during at least 18 months(DTUSat, 2006).

1.2 State of the Art

In this section, some examples of CubeSat projects developed in the last decade by universities and institutions worldwide are presented, for which some kind of information about the OBC was available. It needs to be noted that since these projects are usually performed as the scope of a Master or Bachelor Thesis, public access is not often granted to such detailed information.

The projects presented in this section are interesting for DTUSat because the satellites operate in similar orbits as the ones being considered for DTUSat-3 and because they were built using COTS components. Moreover, all of them design the OBC subsystem in a different way, hence providing inspiration for DTUSat.

1.2.1 OPTOS

In November 2013, the National Institute of Aerospace Technique (INTA) from Spain, launched the OPTOS satellite. OPTOS is based on a CubeSat 3U structure, with a mass of 3 kg, that features low power consumption and high-performance capabilities (Aragón et al., 2011; Aragón et al., 2012). The aim of this project is to provide a low-cost and easy access to space for companies and organizations. Therefore, the OPTOS satellite was partially built with COTS components, previously assessed with respect to their fault tolerance (Martín-Ortega et al., 2019).

OPTOS was launched into a Sun-synchronous near-circular orbit, with an altitude of 670 km and an inclination of 97.8°(EoPortal Directory, 2014b). Initially, the expected operation lifetime for the satellite was 1 year, however, it was increased to 3 years. During this time, INTA qualified the four payloads on board OPTOS, which are: a Giant Magneto-Resistance, for measuring the Earth magnetic field; a Dose Monitor, for measuring the total ionizing dose; a Fiber Bragg Gratings for Optical Sensing, to evaluate the feasibility of optical fiber sensors for temperature measurement; and a Athermalized Panchromatic Imaging System (Aragón et al., 2011; Aragón et al., 2012).

Furthermore, the On-Board Computer from OPTOS is based on a distributed architecture where each subsystem has a local processor. Each local processor is part of the Distributed OBC Terminals. All terminals, as well as the OBC, are connected by an Optical Wireless CAN Bus (Martín-Ortega et al., 2019). This way, to communicate data between subsystems, there is no need of cable usage. Instead, every subsystem is equipped with an emitting and a receiving diode that can pulse light at different frequencies, as well as reading the signals coming from other boards (EoPortal Directory, 2014b).

This wireless approach facilitates the implementation of collaborative hardening techniques (Martín-Ortega et al., 2019), which are needed in order to achieve a suitable level of dependability against Single Event Upsets (SEUs). In this type of hardening, all messages sent by any unit are received by all units at the same time. This makes the critical tasks in the system dependable by means of adding redundancy, even if each module is not fault

tolerant (Portela-García et al., 2011).

1.2.2 Delfi-C3

The Delfi-C3 satellite is the first student nano-satellite from the Delft University of Technology in The Netherlands (Aalbers and Gaydadijev, 2006). Delfi-C3 is based on the 3U CubeSat structure and it was design to be a low-cost, short-time-to-delivery mission using COTS components. It was launched on April 2008 into a Sun-synchronous circular orbit, with an altitude of 635 km and an inclination of 97.94°(EoPortal Directory, 2014a). The main objective of this Delfi-C3 project was to test three payloads on board the satellite: a Thin Film Solar Cell, an Autonomous Wireless Sun Sensor and an Advanced Transceiver (Breukelen et al., 2006; Bouwmeester, Aalbers, and Ubbels, 2008).

Moreover, the Delfi-C3 On-Board Computer is part of the Pumpkin FM 430 CubeSat kit, which is an affordable off-the-shelf hardware and software development and deployment solution that also includes the CubeSat structure (Pumpkin Inc, 2013). The OBC features a Texas Instrument 16-bit microcontroller, with 10KB RAM, as well as 60KB of flash memory for data storage (Brouwer and Bouwmeester, 2009). Delfi-C3 OBC is built around a distributed architecture, similar to OPTOS and DTUSat-2. However, in this case, an I2C data bus is used for communication between all subsystems and the OBC (Aalbers and Gaydadijev, 2006).

1.2.3 UWE-3

UWE is a student satellite project from the University of Wuerzburg in Germany, whose goal is to demonstrate formation flying capabilities at pico-satellite level (Busch et al., 2015). The UWE-3, launched in November 2013, focuses on in-orbit attitude determination and attitude control (Bangert, 2012). Therefore, UWE-3 is equipped with a variety of sensors, magnetic torques and one reaction wheel (Wuerzburg University, 2016).

UWE-3 was launched into a Sun-synchronous near-circular orbit, with an altitude of 650 km and an inclination of 97.7°(Wuerzburg University, 2016). Moreover, the satellite is based on the 1U CubeSat structure, with a mass of about 1 kg (Bangert, 2012). The satellite structure is built around a stack of several subsystem printed circuit boards that are all interconnected between one another by a backplane with standardized connectors. This approach allows to densely stack the subsystems and achieve a compact design (Busch

and Schilling, 2013).

Furthermore, UWE-3 features a dual-redundant low power on-board computer (Busch et al., 2015), that reduces mass and adds reliability to the overall system (Wuerzburg University, 2016). The OBC has two redundant ultra low power microcontroller units (MCUs) in a master-slave configuration which is dynamically decided by a separate arbitration unit (Busch and Schilling, 2013). This dual approach enhances reliability and robustness against radiation-induced failures (Busch et al., 2015). Moreover, it uses an I2C bus for data transmission (Busch and Schilling, 2013).

UWE-3 has been the precursor of this dual OBC architecture. Since its launch, it has proven robust and reliable operations, to the point that is was replicated for the next generation of UWE satellites, UWE-4 (EoPortal Directory, 2019).

1.2.4 CanX-2

CanX-2 is the second generation of student nanosatellites developed by the University of Toronto in Canada, with the objective of demonstrating several technologies critical for the 2009 CanX-4 and CanX-5 formation flying mission (Sarda et al., 2006). These technologies include a custom cold-gas propulsion system, a anosatellite reaction wheel and a commercially available GPS receiver (EoPortal Directory, 2017). CanX-2 is based on the 3U CubeSat structure with a mass of 3.5 kg (Rankin et al., 2005). It was launched in April 2008 into a Sun-synchronous orbit, with an altitude of 635 km and an inclination of 97.4°(EoPortal Directory, 2017).

Furthermore, CanX-2 features a hybrid architecture with two computer boards: the main OBC and the payload OBC. Both OBCs utilize a 15MHz ARM7 processor, with 2MB of SRAM, and EDAC (Error Detection and Correction) software for SEUs that occur in LEO. Moreover, each processor also holds 16 MB of flash memory for data storage (Sarda et al., 2006; EoPortal Directory, 2017). Serial (USART) and SPI buses link the OBCs to all the other subsystems and payloads (Rankin et al., 2005).

Summary

Table 1.4 summaries the characteristics of the on-board computers of the four satellites mentioned above.

	DTUSat-2	OPTOS	Delfi-C3	UWE-3	CanX-2
Architecture	Distributed	Distributed	Distributed	Dual	Hybrid
Data bus	CAN	CAN	I2C	I2C	SPI
Wireless	No	Yes	No	No	No

Table 1.4: OBC Architecture of several CubeSat projects.

1.3 Structure of the report

- Chapters 2 and 3 present the engineering challenge, as well as the motivations and objectives for this project, followed by a specification of the requirements the designed OBC must fulfill.
- Chapter 4 introduces different concepts, technologies and guidelines that are needed in order to understand the approach taken for the design and implementation of the On-Board Computer for DTUSat-3.
- Chapter 5 describes the process of designing, soldering and inspecting the printed circuit board developed for the On-Board Computer of DTUSat-3.
- Chapter 6 explains the various tests and verification processes conducted to the OBC for DTUSat-3. Test setups and test results are presented and discussed in order to evaluate the performance of the designed OBC.
- Chapter 7 concludes the design and implementation of the OBC.
- Chapter 8 discusses several issues and opportunities that were found during the development of the project and summarizes tasks for future work.
- The appendices contain mechanical drawings, PCB schematics and layouts and bill of materials of the board as well as SPENVIS models for the radiation environment and considerations when booting Linux for the first time.

Chapter 2

Problem formulation

The goal of this Master Thesis is to design, manufacture and test an On-Board Computer for DTUSat-3 that complies with all the requirements of the satellite and the mission. In this chapter, the motivation and objectives of this project, as well as the methodology, schedule and resources used, are explained.

2.1 Motivation

As explained in the Section 1.1, DTUSat already has available an existing OBC which could be implemented for DTUSat-3. However, there are several reasons behind the need to develop a new OBC for DTUSat and they are described here:

1. Have a modular and reusable satellite

For spaceflight missions, it is critical to reduce mass and reuse resources, since it brings down the costs and speeds up the development process. In order to achieve this, having a modular architecture is essential. Modules have the advantage of being replaceable and reconfigurable (Trinh et al., 2015) which allows to build a variety of small satellites with different functions. This way, the developed OBC should be a generic and versatile hardware interface that can be tailored to different mission profiles.

2. Ease the software development

It is necessary to make the software development as easy as possible so that more students can get involved in the design of the satellite and further projects can be developed in the future. For this, it is desired to have an OBC that runs a familiar operating system, like Linux, where the hassle of low-level interfacing is removed by the hardware abstraction layer provided by the Linux kernel. To achieve this, the OBC will be based around a System

in Package (SiP) component, such as the OSD335x-SM from Octavo, which has a lot of BeagleBone® functionality already integrated into a small package.

3. Reduce power consumption

Solar power depends on the conversion efficiency and on the available area for solar cells, which at the same time depends on the size of the satellite. Since CubeSats are small satellites with a rather small available area for solar cells, the total electrical power is limited (Speretta et al., 2016). This way, it is necessary that each subsystem consumes as little power as possible so that there is enough power left for the payload and the rest of the subsystems in the satellite. For this reason, the OBC for DTUSat-3 should be design to have a reduced power consumption.

2.2 Objectives

As mentioned before, the main objective of this project is to develop an On-Board Computer for DTUSat-3 that complies with all the requirements of the satellite and that runs in Linux, so that it is easier for students to develop the software. Furthermore, this OBC should be developed using COTS components to reduce cost.

Moreover, system integration and testing will be given a lot of emphasis in this project. Testing should be conducted through the final flight configuration of the bus hardware since it increases the chances of revealing any unwanted side effects of subsystem interaction.

In order to achieve this, the project will contain the following tasks:

- Design and manufacture a PCB for the OBC

A Printed Circuit Board (PCB) that contains all the components needed for the OBC and that fulfills the requirements for the satellite and the mission should be designed and manufactured. Specifications for the board include, among others, a predefined size to fit the carrier board in which it will be mounted as well as certain communication ports and protocols in order to be able of communicating with the rest of the satellite's subsystems.

- Soldering the components into the PCB

Once the PCB has been manufactured and delivered, the soldering process of the components is started. The soldering process is composed of two phases: a reflow soldering

stage, for smaller components as well as components with pads underneath the package, and a hand soldering stage, for larger components.

- Development of a standard function test

A standard function test needs to be designed in order to be able of recognizing if a failure mode has occurred when performing further tests. This will be done by developing an FMEA/FMECA analysis, identifying the potential failure modes of the OBC, followed by an study of how these potential failures can be checked during a test.

- Execution of a preliminary qualification campaign

A preliminary qualification campaign needs to be carried out on the developed board in order to guarantee the correct functioning of the OBC in the space environment. This campaign will consist of a radiation test.

In space, components are exposed to much more radiation than on the Earth's surface. For this reason, radiation tests need to be carried out to ensure that the components of the OBC will survive in such a high radiation environment. This radiation tests have to take into account Total Ionizing Dose and Single Event Effects. Both tests characterize the tolerance of the board to the radiation environment but Total Ionizing Dose tests use gamma ray sources while Single Event Effects tests use heavy ion and proton accelerators.

2.3 Methodology and Schedule

The Gantt Diagram for the project is shown in Appendix B and it is described below.

First, a preliminary research will be carried out to understand the state of the art of OBC's in the space and satellite sector. After that, the Printed Circuit Board (PCB) will be design using a specific software that facilitates the layout of schematics for electronic circuits, like KiCad. Then, the schematics will be manufactured into a physical PCB. Once the PCB is finished, all the electronic components will be assembled and soldered to it. After that, the standard function test will be developed. Finally, the OBC will go through a preliminary qualification campaign, which includes a radiation test, to guarantee the correct functioning of the board.

In parallel with the development of the project, the Thesis Report will be written.

2.4 Resources

For this project, the following resources will be used and are explained here:

- PocketBeagle®

PocketBeagle® will be the base from which to start developing the OBC for DTUSat-3. PocketBeagle® (Figure 2.1) is a Linux-based computer with a size of 55 mm x 35 mm x 5 mm. It uses the Octavo Systems OSD3358-SM System-in-Package (SiP) and it has a microSD connector to store the Linux operating system. The board is powered from +5 VDC via a microUSB connector (BeagleBoard, 2019).

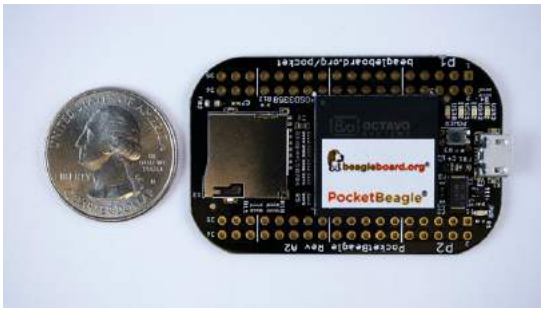


Figure 2.1: PocketBeagle® (BeagleBoard, 2019).

- OSD3358-SM System-in-Package

The OSD335x-SM (Figure 2.2), with a size of 21 mm x 21 mm, is compatible with AM335x development tools and software. It integrates into a single Ball Grid Array (BGA) Package the TI Sitara™ARM® Cortex®-A8 AM335x processor, a DDR3 memory, the TPS65217C Power Management Integrated Circuit, the TL5209 Low Dropout regulator and a 4KB EEPROM (Octavo Systems, 2015).

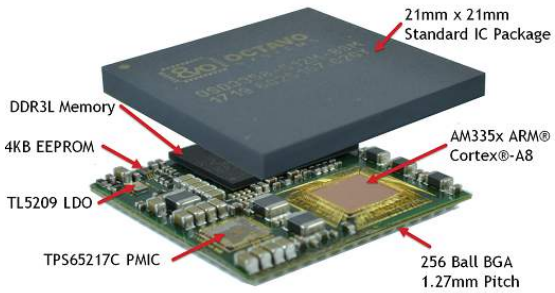


Figure 2.2: OSD335x-SM System-in-Package (Octavo Systems, 2015).

- KiCad

KiCad is a set of applications used to develop schematics for electronic circuits and their conversion to PCB designs. It will be used in this project to design the schematics and the layout of the PCB for the OBC.

- Space Environment Information System (SPENVIS)

SPENVIS is ESA's Space Environment Information System, a web interface to model the space environment and its effects, including cosmic rays, natural radiation belts, solar energetic particles, plasmas, gases and "micro-particles" (ESA, 2019b).

- Risø High Dose Reference Laboratory

The Risø High Dose Reference Laboratory will be used to carry out the radiation tests. The laboratory is located at DTU Nutech (Center for Nuclear Technologies) and it has several gamma ray sources, based on the radioactive decay of the Cobalt-60 isotope, which are suited for radiation tests on electronic circuits and devices.

Chapter 3

System specifications

In this chapter, the requirements for the DTUSat-3 satellite and OBC are described based on the preliminary document *DTUsat-3: System Requirements Document* (DTUSat, 2019).

3.1 DTUSat-3 satellite

The satellite is based on a 1U CubeSat (10 cm x 10 cm x 10 cm) of approximately 1 kg. The structure is built around a stack of several subsystem printed circuit boards that are all interconnected between one another by a Subsystem Carrier Board (SSCB). The SSCB can accommodate up to four subsystem printed circuit boards, two on the top and two on the bottom. This way, there are two standardized connectors per face in the SSCB that allow powering of and communication with the different subsystems connected to it. This approach allows to achieve a compact and modular design.

Moreover, DTUSat-3 satellite will be composed of the following subsystems: Mechanical subsystem, Electrical power subsystem, Communications system, On-Board computer system, Attitude control and determination system and a Propulsion system. Table 3.1 shows the mass and power budget for the different subsystems.

As it can be seen, comparing with DTUSat-2 (Table 1.3), in DTUSat-3 the OBC has more available power. The reason for this is that the main motivation of building a new OBC is to ease the software development by using Linux and this approach consumes much more power.

Finally, DTUSat-3 is expected to be launched into a Sun-synchronous orbit between 550 km to 700 km of altitude and an inclination of 98°. Furthermore, the expected duration of the mission is 18 months and it is assumed that satellite will employ aluminum side panels with a thickness of 1.5 mm, as in DTUSat-2 (DTUSat, 2006).

Subsystem	Mass (g)	Power (mW)
Mechanical Subsystem	700	–
Electrical Power Subsystem	300	80
Communications system	100	300
On-Board Computer	75	400
Payload	210	830
Total	1385	1610

Table 3.1: DTUSat-3 mass and power budget.

3.2 DTUSat-3 On-Board Computer

In this section, the mechanical constraints of the printed circuit board for the OBC of DTUSat-3 are explained and the minimum radiation tolerance requirement for the board is given.

3.2.1 Mechanical constraints

The printed circuit board for the OBC needs to fulfill several mechanical specifications in order to accommodate it inside the satellite structure. First of all, it needs to have a size of 35 mm x 65 mm in order to fit on top of the SSCB. The PCB should also have four holes, one in each corner, for the screws that hold it to the structure. Moreover, the board, including the components once they are soldered, should have a maximum height of 6.6 mm, which is the space left between one SSCB and the other. The schematics of the PCB dimensions can be seen in Appendix C.

3.2.2 Radiation

In order to estimate the total radiation dose for the OBC, the Space Environment Information System (SPENVIS) software from ESA was used.

For orbits with an inclination of 98°, the total ionizing dose during 1.5 years with 1.5 mm aluminum side panels varies between 5 krad, for 550 km altitude, and 10 krad, for 700 km altitude. The models and graphs can be found in Apenddix D. This translates into a minimum tolerance requirement for the On-Board Computer of DTUSat-3 of 10 krad accumulated over the mission lifetime. Moreover, the new space legislation requires the

satellite to be commanded to reenter Earth's atmosphere within 27 years of mission completion in order to remove mass from densely populated orbits (ESA, 2019a). This way, SPENVIS estimates that the total radiation dose during 25 years for the OBC is between 50 krad and 85 krad. Since the OBC should be operative after 27 years in order to comply with the legislation, the desirable tolerance requirement for the On-Board Computer of DTUSat-3 is 85 krad. Also, the OBC must also be able to handle single event effects (SEEs). These are described in Section 4.8.

Finally, Table 3.2 summarizes the requirements for the OBC of DTUSat-3.

Maximum mass	75 g
Maximum dimensions	65 x 35 x 6.6 mm
Available power	400 mW
Minimum radiation tolerance	10 krad
Desirable radiation tolerance	85 krad

Table 3.2: DTUSat-3 OBC requirements.

Chapter 4

Theory

This chapter describes and explains different concepts, technologies and guidelines that are needed in order to understand the approach taken for the design and implementation of the On-Board Computer for DTUSat-3. For this reason, this chapter should be read as a complement to Chapter 5: System design and implementation.

4.1 On-Board Computer

As mentioned before, the OBC is the brain of the satellite, responsible for monitoring and controlling every function of the satellite as well as for implementing control laws (European Space Agency, 2015). Therefore, satellite OBCs need to fulfill some specific requirements, that are not applicable for a standard computer on Earth, in order to make them suitable for space applications. These are (Eickhoff, 2011):

1. Provide the numeric performance for the mission purpose.
2. Be mechanically robust to withstand launcher induced loads.
3. Withstand challenging thermal conditions.
4. Withstand high energetic particle radiation doses.
5. Limited power consumption, imposed by the power generation subsystem.
6. Fulfill the criteria with respect to safety and redundancies, since no maintenance can be done during the satellite's operation.

In this section, the main elements that form the OBC are described. Afterwards, the different types of on-board computer architectures are explained and a suggestion of

implementation for DTUSat-3 is given.

4.1.1 OBC main elements

The OBC of a satellite needs to communicate with the rest of the subsystems as well as storing data, such as the main application or science and housekeeping information, and then transmitting it back to the ground station on Earth. Therefore, the OBC should have at least the following elements (Eickhoff, 2011):

- Microprocessor
- Internal memory RAM
- Boot memory PROM
- Data buses and bus controllers
- Debug interface
- Power control equipment

Other optional elements are also desirable, for example a mass memory in order to be able of storing more science and housekeeping data.

4.1.2 OBC architecture

When it comes to CubeSat OBCs, there are many important limitations on the available power and mass and the data storage capacity. This constitutes an important constraint on the OBC, whose requirements involve: to have a low power consumption, an automatic operation and a high reliability and to be as simple as possible. Moreover, flexibility is also desired in an OBC because it increases modularity of the system (Kiadtikornthaweeyot, 2015). All of these operational characteristics of the OBC are determined by the computer architecture, hence it is a very important issue to take into consideration. This way, the four main types of OBC architectures are explained next:

- Central or Star

This type of configuration, also referred as Star architecture, places the OBC at the center of the satellite, as it can be seen in Figure 4.1, while all the other subsystems

are directly connected to it. This means that all communications between the different subsystems need to go through the OBC. The OBC is therefore in charge of performing all of the Command and Data Handling Subsystem (CDHS) functions, which include data transfers with the subsystems and the ground (Aalbers and Gaydadijev, 2006).

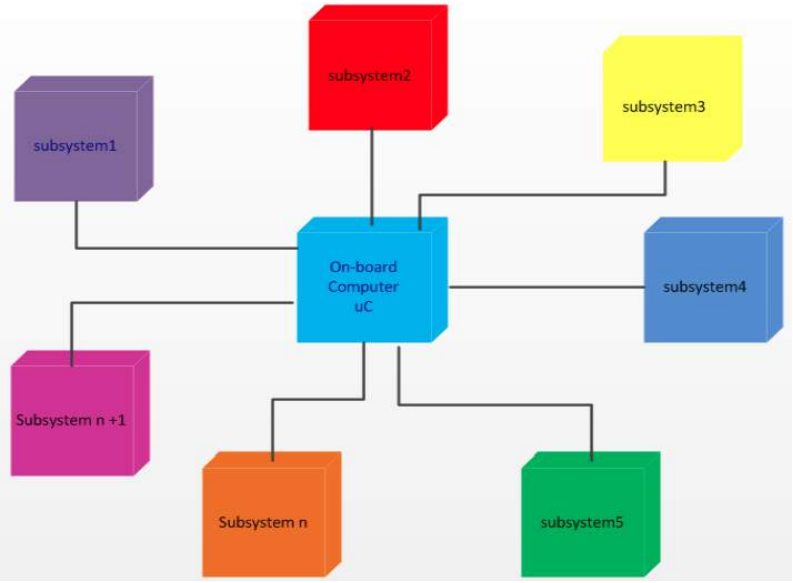


Figure 4.1: Block diagram of the central or start architecture (Kiadtikornthaweeyot, 2015).

The advantage of this type of architecture is that is reduces complexity, hence the system can be designed with simpler hardware. At the same time, a simpler architecture reduces the chance of communication problems between subsystems (Kiadtikornthaweeyot, 2015).

However, the central architecture has several disadvantages. The main one is that in this architecture the OBC is highly dependent upon all the subsystems. This reduces modularity and flexibility, since a change in one subsystem influences the design of the entire OBC (Aalbers and Gaydadijev, 2006). Another important issue is electromagnetic interference between the signals running form the subsystems to the OBC. In the star architecture all signals have to travel relatively long distances and in close proximity to other signals, with only a minimal amount of shielding, which can lead to interference. This reduces the reliability of the signals (Aalbers and Gaydadijev, 2006).

- Distributed

In the distributed architecture, the OBC is no longer directly connected to all the subsystems, as it can be seen in Figure 4.2, but it still fulfills a central role. Each sub-

system is equipped with a local processor or microcontroller that handles the interaction with the subsystem. All microcontollers as well as the OBC, are connected to a serial data bus. This means that, opposite to the central architecture, all subsystems are able to contact each other without going through the OBC (Aalbers and Gaydadijev, 2006; Townsend, Palmintier, and Allison, 2000). Examples of CubeSats that implement this OBC architecture are DTUSat-2, OPTOS and Delfi-3.

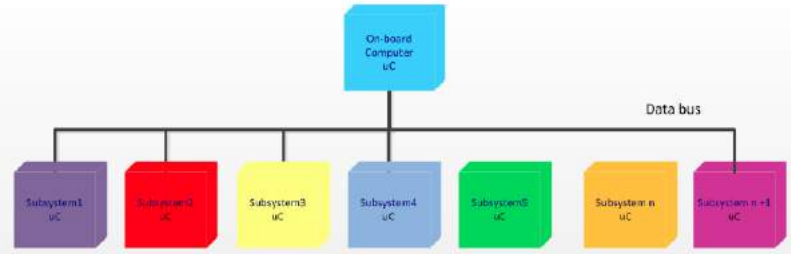


Figure 4.2: Block diagram of the distributed architecture (Kiadtikornthaweeyot, 2015).

This type of architecture solves several issues that were present in the central architecture. The main advantage of the distributed architecture is that the different subsystems can be independently developed, which increases modularity and flexibility and, also, allows independent testing of the subsystems (Kiadtikornthaweeyot, 2015). Furthermore, the distributed architecture increases the simplicity of the software used to interact with the subsystems (Aalbers and Gaydadijev, 2006).

However, the most important drawback of introducing this type of architecture is that the number of components is significantly increased, which translates into more occupied surface area on the PCBs and an increase in power consumption. This last issues is very critical because the available power in CubeSats is rather limited (Aalbers and Gaydadijev, 2006). Moreover, the hardware complexity is also increased when implementing the distributed architecture (Kiadtikornthaweeyot, 2015).

- Hybrid

The hybrid architecture combines the advantages of both the central and distributed architectures. It consists of two main microcontrollers in two separate boards, as it can be seen in Figure 4.3. On the one hand, the first microcontroller is in charge of the essential subsystems of the satellite, such as power, altitude and orbit control subsystem (AOCS) and beacon and main communication subsystems (Com-1). On the other hand, the second microcontroller is in charge of the payload of the satellite, and its design depends on the satellite mission (Kiadtikornthaweeyot, 2015). An example of a CubeSat that implements

this OBC architecture is CanX-2.

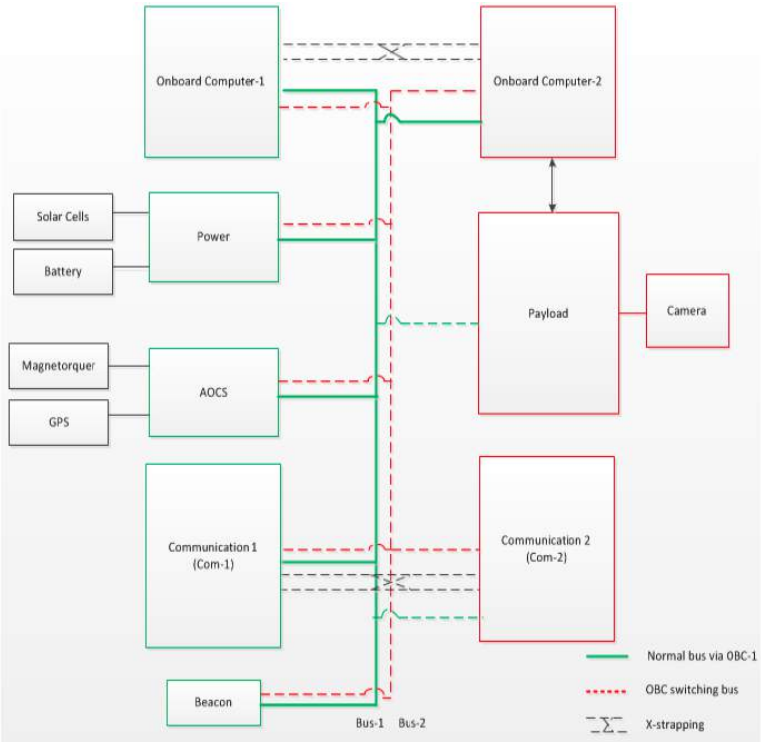


Figure 4.3: Example of hybrid architecture (Kiadtikornthaweeyot, 2015).

The main advantage of this type of architecture is that it allows to design the two boards independently from one another, which gives the system design more flexibility. Furthermore, the hybrid architecture has a main and a redundant communication subsystem as well as a bus system which increases reliability.

However, the implementation of the hybrid architecture, which consists of two separate PCBs, increases the power consumption of the OBC as well as the mass. Therefore, this should be taken into account when defining the power and mass budgets.

- Dual

The last type of OBC architecture is called dual architecture. It was first implemented by the University of Wurzburg in its UWE-3 satellite (Busch and Schilling, 2013; Busch et al., 2015). This dual architecture is built around two redundant microcontroller units (MCUs), placed on the same board, in a master-slave configuration. The decision of which MCU is the master is dynamically made by a separate watchdog controlled arbitration unit, the toggle watchdog unit (TWU). A block diagram of this architecture is shown in Figure 4.4. Moreover, in this type of architecture, all other subsystems usually carry their

own processing units, as in the distributed architecture.

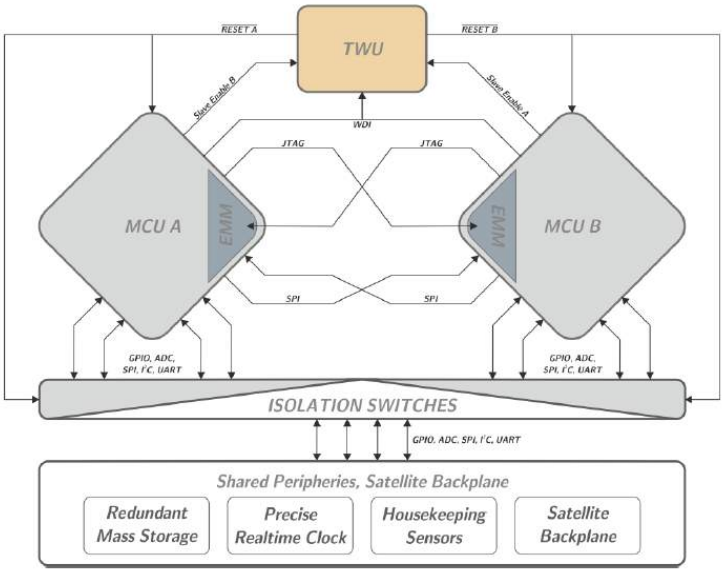


Figure 4.4: Block diagram of the dual architecture for the OBC of UWE-3 (Busch and Schilling, 2013).

The main idea behind the master-slave configuration is that the master can access and control the slave when and how it needs. This way, the slave can even be completely reprogrammed for memory recovery or secure software updates by the current master MCU. For clock synchronization between the MCUs, the system provides a temperature compensated high precision real-time clock. In normal operation, the current master periodically triggers the TWU, and, if it fails to do so within a specified period of time, the TWU performs a reset on both MCUs. The TWU then swaps the master-slave configuration but leaves the former master in reset state. Afterwards, the slave might be enabled by the master if necessary.

This redundancy scheme allows to automatically recover from failure conditions by initiating a fail-over to the redundant unit without the need for manual interaction. Furthermore, the dual architecture allows robust and reliable operations as well as fail-safe in-orbit software updates.

However, having two MCUs in the same board increases the board size and mass, as well as the power consumption, although not as much as the hybrid architecture.

Finally, Table 4.1 summarizes the main advantages and disadvantages of each type of architecture.

Type	Advantages	Disadvantages
Central or star	• Reduced complexity • Simpler hardware • Fewer communication problems	• Reduced modularity • Lack of flexibility • Lack of redundancy • Electromagnetic interference
Distributed	• Independent design • Increased modularity • High flexibility • Independent testing • Reliable and robust	• Increased components • Increased power consumption • Complex hardware
Hybrid	• Independent design • High flexibility • High redundancy • High reliability	• Increased number of components • Increased power consumption • Higher mass
Dual	• High robustness • High redundancy • High reliability	• Failure tolerance • Increased power consumption • Higher mass

Table 4.1: On-board computer architectures: advantages and disadvantages.

Comparison

This section compares all the different OBC architectures in terms of how flexible the architecture is, how reliable the design is, how much power it consumes and how much mass it takes. The reason for choosing power consumption and mass as focus points is that they are the most critical issues in CubeSats designs where the available power and mass are limited. Moreover, one of the motivations for developing this project is to be

able of having a modular and reusable satellite, therefore flexibility and reliability are also very important concerns.

In Table 4.2, the different architectures have been given a value according to their performance in each category in comparison with the other architectures (Very low (1), Low (2), High (3), Very high (4)). This means that, for example, for the reliability category, the architecture with a score of 1 is the less reliable of all the architectures. Furthermore, Figure 4.5 shows a visual representation of this, where each architecture is depicted by a circle. The x and y axis correspond to the Reliability and Flexibility performances respectively. Moreover, the color of the circle corresponds to the power consumption being: green, very low; yellow, low; orange, high; and red, very high. Also, the size of the circle represents how much mass the architecture takes, being the smallest circle the one with lowest mass, and the biggest circle the one with the largest mass.

	Central or Star	Distributed	Hybrid	Dual
Flexibility	1	2	4	3
Reliability	1	2	3	4
Power consumption	1	3	4	2
Mass	1	2	4	3

Table 4.2: On-board computer architectures comparison.

As it can be seen, the central architecture has a very low power consumption and mass, but it does not provide flexibility or reliability. Moreover, even thought the hybrid architecture gives a very high flexibility and reliability, it is the one that increases the power consumption and mass the most, hence it is not the optimal solution for a CubeSat. The distributed architecture is also discarded because it is more desirable to have a very reliable OBC rather than one with low power consumption and mass. Finally, the dual architecture provides high reliability and flexibility and also it is possible to implement further actions in order to reduce its power consumption and mass. Therefore, after this preliminary analysis, this project suggests that the dual architecture is implemented for DTUSat-3.

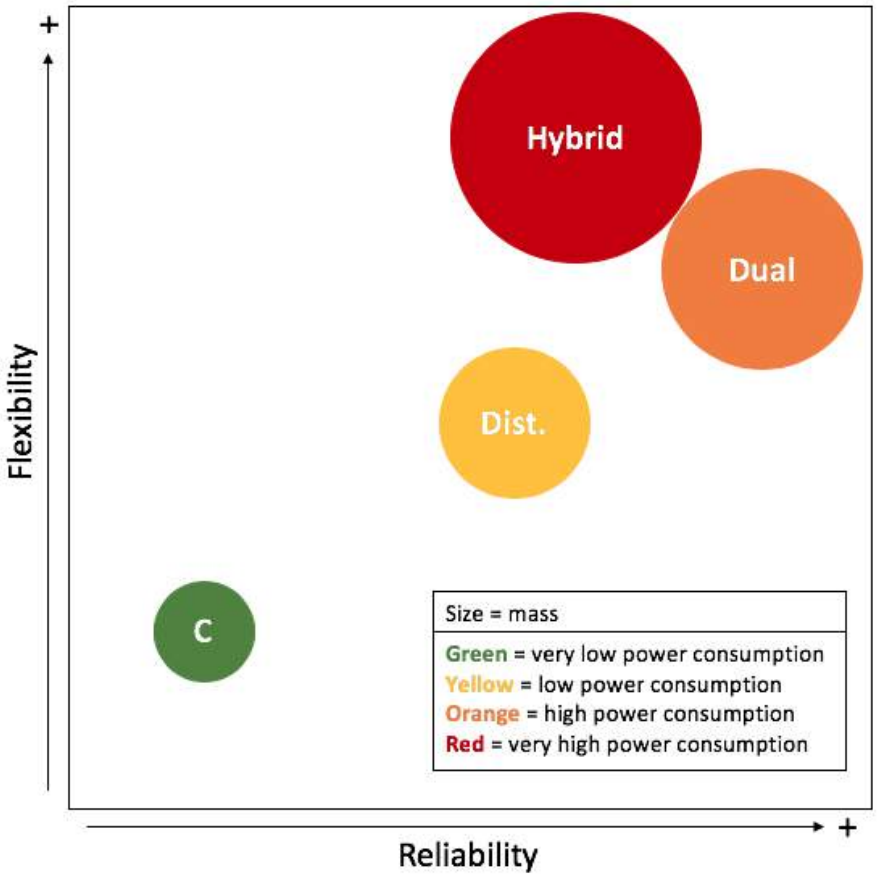


Figure 4.5: Visual representation of OBC architecture classification.

4.2 DTUSat-3 On-Board Computer components

In this section, the components that are used to built the OBC of DTUSat-3 are described. These include: the PocketBeagle board, the Octavo OSD335x-SM SiP, the XCL103D step-up converter, the SN65HVD234 CAN transceiver and the DF17 board to board connector. The reasons for choosing them as well as some functions and operational modes interesting for the project are explained next.

4.2.1 PocketBeagle®

PocketBeagle® is a Linux-based computer with a size of 55 mm x 35 mm x 5 mm. It uses the Octavo Systems OSD3358-SM System-in-Package (SiP) and it has a microSD connector to store the Linux operating system (BeagleBoard, 2019).

One of the greatest advantages of buying a PocketBeagle, and not the Octavo SiP directly, is that it is an already manufactured board, whose schematics and layout designs are open sourced. This means that the design of the OBC does not need to start from scratch and can be based on the PocketBeagle design. This approach will save time and money, both very valuable in student satellite projects like DTUSat. Furthermore, basing the design on the PocketBeagle board allows to have a modular and reusable OBC since it has UART, SPI, I2C and CAN communications available. Moreover, PocketBeagle boots directly from a microSD card and runs in Linux. Linux allows to ease the software development because of two reasons: 1) the programming language is high-level and 2) a large body of drivers is already available online which reduces the amount of code that needs to be written (Kridner, 2019). This means that more students can get involved in the design of the satellite and further projects can be developed in the future. To sum up, PocketBeagle was chosen because it fulfills all the motivations of this project.

Figure 4.6 shows the PocketBeagle board as well as the location of its different components, while Figure 4.7 shows a high level block diagram of PocketBeagle.

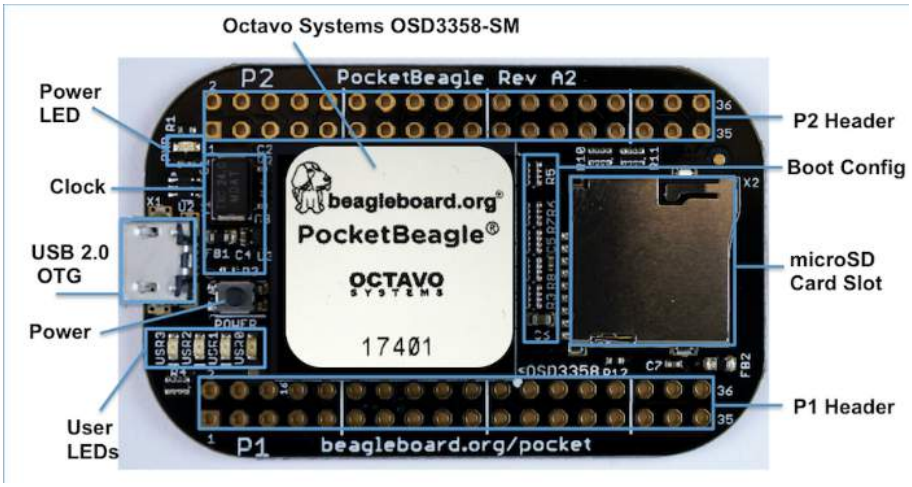


Figure 4.6: PocketBeagle components location (Kridner, 2019).

The key components on the board as well as their function are described next, based on the *PocketBeagle System Reference Manual* (Kridner, 2019):

- **Octavo Systems OSD335x-SM SiP**: it is the processor system for the board and it is explained in more detail in Section 4.2.2.
- **microSD card connector**: it acts as the primary boot source for the board. It is suitable for almost any microSD card but the most common one is 4GB, since it is

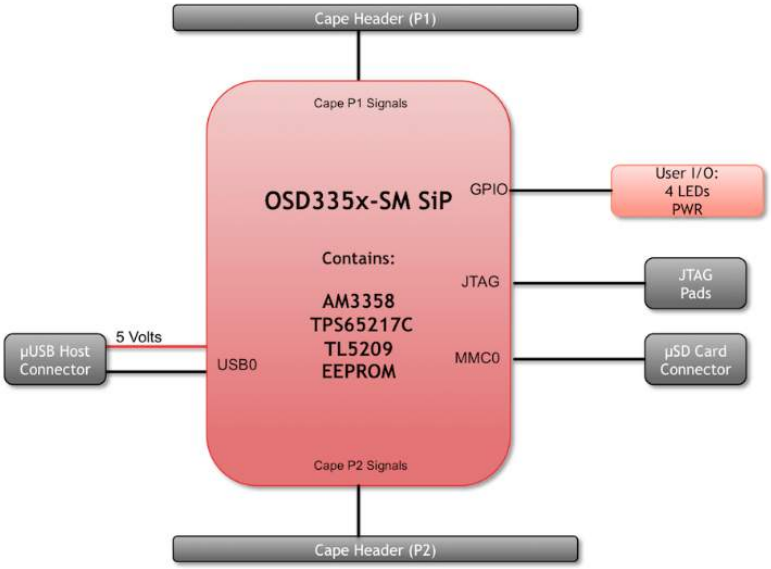


Figure 4.7: PocketBeagle block diagram (Kridner, 2019).

the size of the Linux image.

- **USB 2.0 connector**: it is a microUSB connection that is generally used as a client USB port connected to a power source, such as a computer, to power the board. However, it can also be programmed to be used in host mode.
- **Texas Instrument TPD4S012 Transient Voltage Suppressor**: it reacts when the USB input voltage is higher than its reference voltage, hence protecting the entire board from sudden or momentary overvoltage conditions.
- **Clock**: a crystal oscillator circuit provides an stable clock signal to the Octavo SiP.
- **Texas Instrument SN74LVC1G07 Single Buffer/Driver with open-drain**: it provides the systems initialization signal, so that the supply rails can settle before the Octavo SiP starts up. The Octavo SiP requires an active low warm reset that is provided by this component.
- **USER LEDs**: the board has four programmable blue LEDs.
- **Power button**: it can be used to power up or power down the board.
- **Power LED**: it provides information regarding the power to the board.
- **Expansion headers**: they give access to a large number of peripheral functions and GPIO. They have been left unpopulated to enable users to choose the header connector orientation. Moreover, the pin configuration can be seen in Figure 4.8.

– **Other**: other components include ferrite beads, capacitors and resistors.

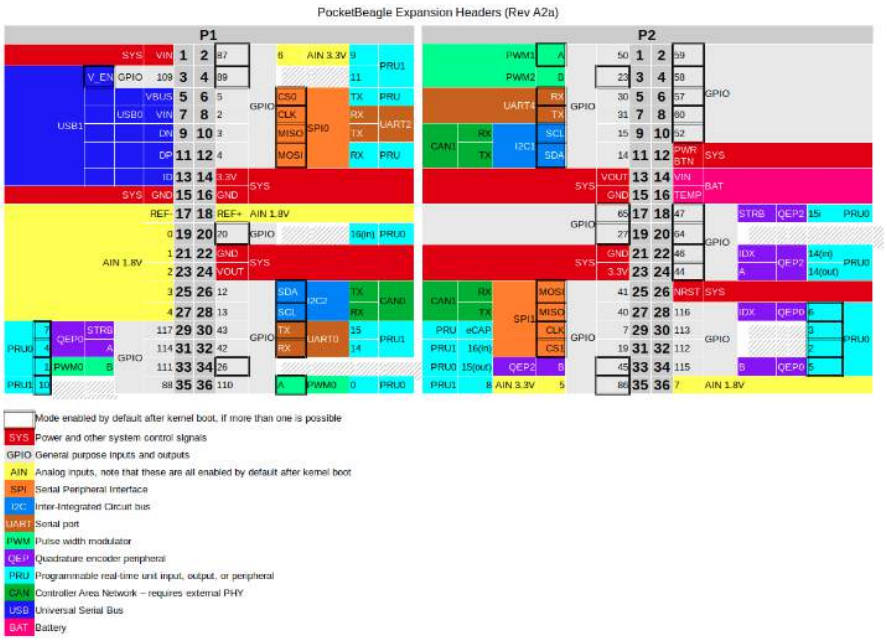


Figure 4.8: PocketBeagle expansion headers pin functions (Kridner, 2019)

Moreover, the board can be powered from three different sources: a USB port on a computer, a power supply with a USB connector and the expansion Header pins.

Finally, PocketBeagle provides on the back of the board (Figure 4.9) 7 pads for an optional connection to a JTAG emulator for debugging purposes.

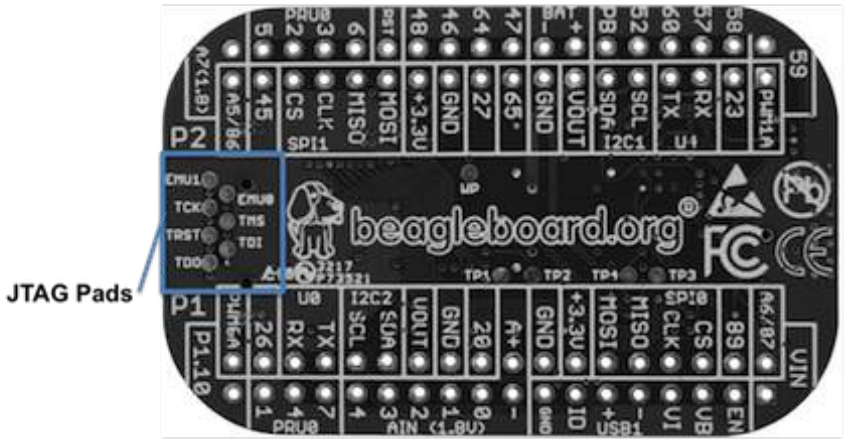


Figure 4.9: PocketBeagle JTAG pad connections (Kridner, 2019)

Power consumption

Using a powermeter, it was verified that the PocketBeagle consumes up to 1.5 W. During boot, the board consumes 1.423 W while, in idle, it consumes 0.540 W. Moreover, it was checked that the LEDs consume approximately 20 mW.

4.2.2 Octavo SiP

The Octavo Systems OSD335x-SM System-in-Package, with a size of 21 mm x 21 mm x 3 mm, integrates into a single Ball Grid Array (BGA) Package the TI Sitara™ARM® Cortex®-A8 AM335x processor, a DDR3 memory, the TPS65217C Power Management Integrated Circuit, the TL5209 Low Dropout Regulator and a 4KB EEPROM (Octavo Systems, 2015). Figure 4.10 shows a block diagram of the SiP.

Figure 4.10: OSD335x-SM System-in-Package block diagram (Octavo Systems, 2017).

The different subsystems inside the OSD335x are explained next, based on the *OSD335x System Reference Manual* (Octavo Systems, 2017):

- AM335x processor

The AM335x processor (in dark red in Figure 4.10) is based on a 1-GHz ARM® Cortex®-A8 32 bit processor. It is enhanced with a PowerVR SGX Graphics Accelerator

subsystem which provides 3D graphics acceleration to support display and gaming effects. Moreover, it has a separated Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS) that allows independent operation and clocking for greater efficiency and flexibility. The PRU-ICSS provides flexibility in implementing fast, real-time responses.

Furthermore, the AM335x processor enables the following peripherals: Controller-Area Network (CAN), SPI, UART, I2C, GPIO, USB 2.0 High-Speed DRD (Dual-Role Device) and Multichannel Audio Serial Port (McASP). In addition, the PRU-ICSS enables further peripheral interfaces and real-time protocols such as EtherCAT, PROFINET and EtherNet/IP, among others.

- TPS65217C Power Management Integrated Circuit

The Power Management IC (PMIC) (in light red in Figure 4.10) provides the necessary power rails to the AM335x and the DDR3 as well as power supply outputs that may be used to power any external circuitry.

- TL5209 Low Dropout regulator

The Low Dropout regulator or LDO (in dark orange in Figure 4.10) is not used inside the SiP, it just provides power supply outputs that may be used to power circuitry external to the OSD335x-SM.

- EEPROM

The OSD335x-SM contains a 4KB EEPROM (in light orange in Figure 4.10) for non-volatile storage of configuration information. The EEPROM is connected to I2C0 bus and it has the final 256 bytes reserved for device specific information while the rest is empty. It needs to be noted that, by default, the EEPROM is write protected.

- DDR3 memory

The OSD335x-SM integrates a 1GB DDR3 memory (in light orange in Figure 4.10). Moreover, the SiP is in charge of handling all the connections needed between the AM335x and the DDR3.

Power Management

The Octavo SiP may be powered by any of the following input power supplies: an external AC Adaptor at 5 VDC (VIN_AC), a USB port at 5 VDC (VIN_USB) and a single cell battery nominally at 3.7 VDC (VIN_BAT).

Moreover, it produces the following output power supplies:

- SYS_VOUT: shared supply to power the AM335x, DDR3 and LDO which is also used to power external circuitry.
- SYS_VDD1_3P3V: a dedicated 3.4 VDC supply to power external circuitry. However, it is important to notice that the the output voltage rail SYS_VDD1_3P3V cannot be used once VIN_BAT drops below 3.5V.
- SYS_VDD2_3P3V: a dedicated 3.3 VDC supply to power external circuitry.
- SYS_VDD3_3P3V: a shared 3.3 VDC supply that can be used to power the AM335x I/O domains.
- SYS_RTC_1P8V: a shared 1.8 VDC supply to power the AM335x RTC which may also be used to power external circuitry
- SYS_VDD_1P8V: a shared 1.8 VDC supply that may be used to power the AM335x I/O domains and external circuitry. It also supplies power to the AM335x SRAM, PLLs and USB.
- SYS_ADC_1P8V: a shared 1.8 VDC supply to power the AM335x ADC which may also be used to power external analog circuitry.

Finally, the Octavo SiP has internal power supplies that are not available to power external circuitry, but they are accessible externally for monitoring purposes only. These are:

- VDDS_DRR: a dedicated 1.5 VDC supply to power the AM335x DDR3 interface and the DDR3 device.
- VDD_MPU: a dedicated 1.1 VDC supply to power the AM335x MPU domain.
- VDD_CORE: a dedicated 1.1 VDC supply to power the AM335x CORE domain.
- VDDS_PLL: a filtered 1.8 VDC supply to power the AM335x PLLs and oscillators.

4.2.3 Step-up converter XCL103D

The XCL103D is a synchronous step-up micro DC/DC converter which integrates an inductor and a control IC in one package of size 2 mm x 2.5 mm x 1 mm.

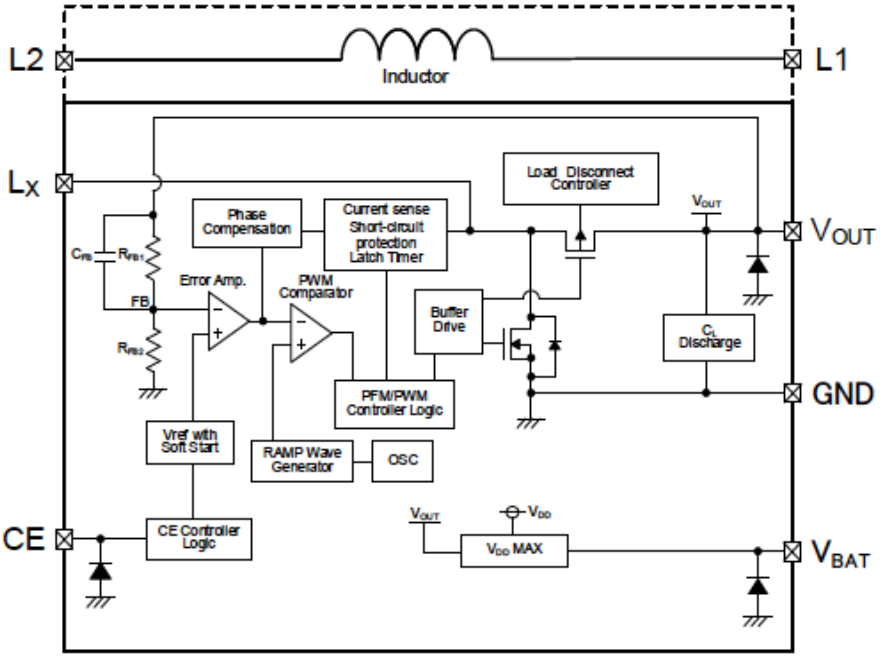
One of the reasons why it was chosen is that it has the inductor built in, which facilitates the design of the schematics and layout and enables minimization of noise and other operational trouble due to the circuit wiring. Also, since it is such a small package, it does not take that much space in the board. Moreover, the step-up converter needs to be able of providing at least 1.5 W in its output, since as it was verified that is the maximum power the Octavo SiP consumes. The step-up converter should provide 5V in its output, which means that it needs a maximum output current limit of at least 300 mA (Equation 4.1). The XCL103D fulfills these specifications because it allows 500 mA in its output. Finally, the XCL103D has an efficiency of around 86%, which is quite large. For all these reasons, the XCL103D was chosen.

$$I = \frac{P}{U} = \frac{1.5W}{5V} = 300mA \tag{4.1}$$

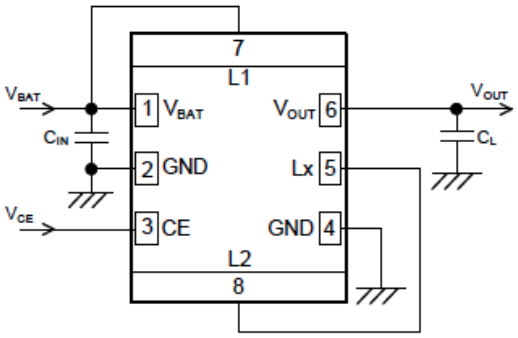
Figure 4.11a shows the block diagram of the converter while Figure 4.11b shows a typical application circuit. Moreover, Table 4.3 describes the different pins in the chip. It should be noted that the CE pin should not be left open, it should be fed with either a low (0-0.2V) or high (0.8-6V) voltage. The low signal puts the step-up converter in stand-by mode while the high signal puts the step-up converter in active mode. When the step-up converter enters stand-by mode, the C_L Discharge Function activates which quickly discharges the output capacitor C_L in order to prevent malfunctions.

Furthermore, the XCL103D incorporates a soft-start which allows the reference voltage to be controlled in a balanced manner. This way, the output voltage rises in proportion to the rise in the reference voltage. This operation prevents rush input current and enables the output voltage to rise smoothly.

Finally, two functions of the XCL103D should be mentioned:



(a) Block diagram.



(b) Typical application circuit.

Figure 4.11: XCL103D step-up micro DC/DC converter (Torex, 2019).

Maximum current limit function

The XCL103D step-up converter has a maximum current limit function which monitors the current that flows in the N-channel driver transistor connected to the Lx pin (Figure 4.11a), and consists of a maximum current limit and a latch. This function works as follows

Number	Pin name	Functions
1	V_{BAT}	Power input
2	GND	Ground
3	CE	Chip enable
4	GND	Ground
5	L_x	Switching
6	V_{OUT}	Output voltage
7	L1	Inductor electrode
8	L2	Inductor electrode

Table 4.3: XCL103D pin specifications.

(Figure 4.12).

If the current flowing in the N-channel driver transistor exceeds the current limit value I_{LIM}, which corresponds to 1.3 A, the N-channel driver transistor turns off, and remains off during the clock interval. In addition, an integral latch timer starts the count ①. The N-channel driver transistor turns on at the next pulse. If no longer in the over-current state, normal operation resumes. The integral latch timer stops the count ④.

If in the over-current state at the next pulse, the N-channel driver transistor turns off as before, and the integral latch timer continues the count ②. Then, if the count of the integral latch timer continues for 100 µs, a function that latches the N-channel driver transistor and P-channel synchronous switching transistor to the off state activates ③.

In the latched state, either restart by shutting down once with the CE pin, or resume operation by lowering the input voltage V_{BAT} below 1.2 V (V_{LAT_R}). The soft start function operates during restart. During the soft-start interval t_{SS}, which is typically 0.5 ms, the integral latch timer and latch function are stopped ⑥.

Short-circuit protection

The XCL103D step-up converter has a short-circuit protection which is a latch-stop function that activates when the output voltage drops below the short-circuit protection threshold voltage in the over-current state. This function works as follows (Figure 4.13).

When in an over-current state (the integral latch timer is counting), if the output voltage V_{OUT} drops below the short-circuit protection threshold voltage V_{SHORT}, a func-

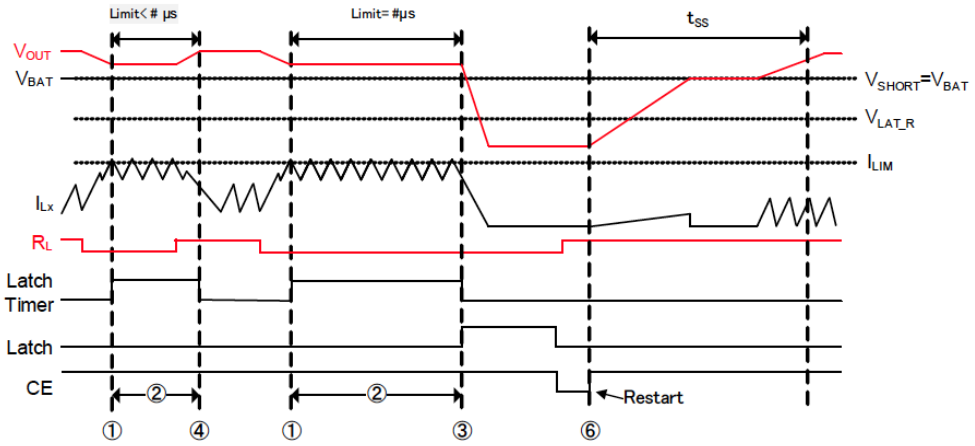


Figure 4.12: Maximum current limit function (Torex, 2019).

tion that latches the N-channel driver transistor and P-channel synchronous switching transistor to the off state activates ⑤.

Then, the same as before. In the latched state, either restart by shutting down once with the CE pin, or resume operation by lowering the input voltage V_{BAT} below 1.2 V (V_{LAT_R}). The soft start function operates during restart. During the soft-start interval t_{SS}, which is typically 0.5 ms, the integral latch timer and latch function are stopped ⑥. When the input voltage V_{BAT} is below the latch release voltage V_{LAT_R}, the integral latch timer and latch function stop, but the current limiting function continues operating.

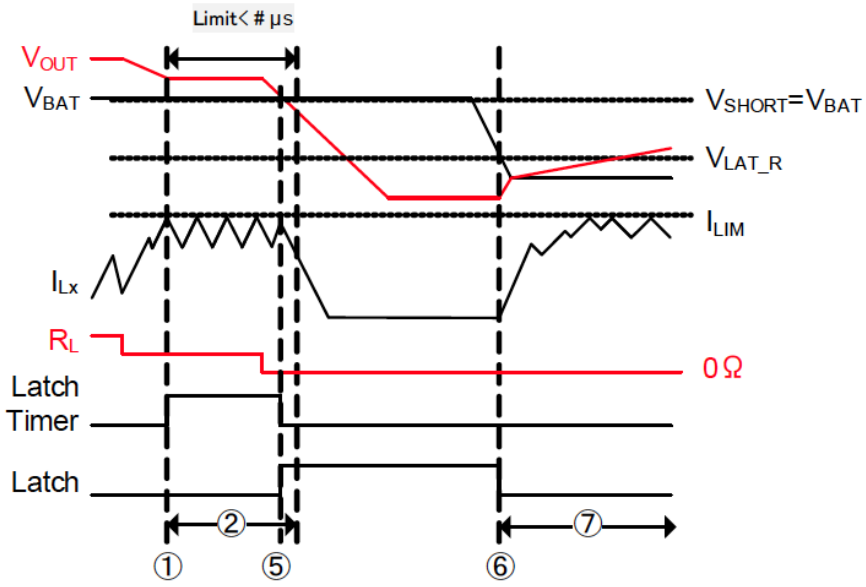


Figure 4.13: Short-circuit protection function (Torex, 2019).

4.2.4 CAN Transceiver

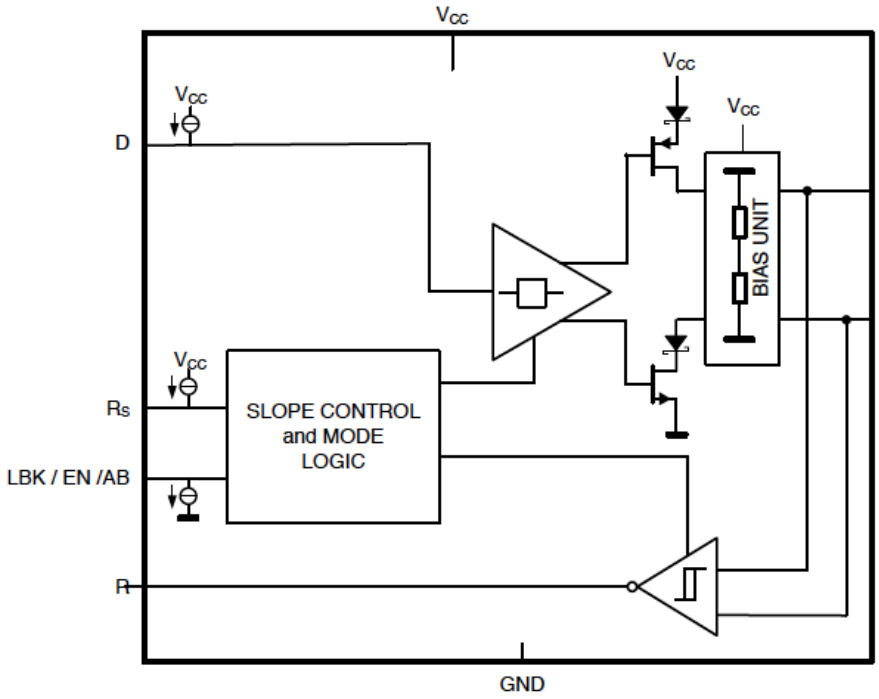
The SN65HVD234 CAN transceiver is the interface between the host CAN controller on the microprocessor and the differential CAN bus. It provides transmit and receive capability with rates up to 1 Mbps. Furthermore, one of the advantages of the SN65HVD234 CAN transceiver is that it is designed especially for operation in harsh environments. Figure 4.14a shows the block diagram of the converter while Figure 4.14b shows the device pin configuration.

Number	Pin name	Functions
1	D	CAN transmit data input
2	GND	Ground connection
3	V_{CC}	Supply voltage
4	R	CAN receive data output
5	EN	Enable input pin
6	CANL	Low level CAN bus line
7	CANH	High level CAN bus line
8	R_S	Mode select pin

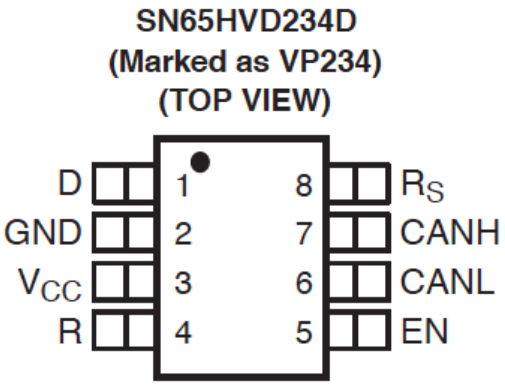
Table 4.4: SN65HVD234 CAN transceiver pin specifications.

Moreover, Table 4.4 describes the different pins in the chip. Pin 8 selects the operation mode between the three modes that the chip provides: high-speed, slope control and low-power stand-by mode. A strong pull-down to ground of pin 8 selects a high speed mode, allowing the driver output transistors to switch on and off as fast as possible with no limitation on the rise and fall slope. A 10 kΩ to 100 kΩ pull-down to ground of pin 8 selects a slope control mode. The rise and fall slope can be adjusted by connecting a resistor between the RS pin and ground. The slope will be proportional to the pin's output current. A strong pull-up to supply voltage of pin 8 selects a low-power stand-by mode in which the local protocol controller is only listening.

Finally, the enable input pin, pin 5, selects an ultra low-current sleep mode in which both the driver and receiver circuits are deactivated when it receives a low logic level. The device remains in this sleep mode until the circuit is reactivated by applying a high logic level to this pin.



(a) Block diagram.



(b) Pin configuration.

Figure 4.14: SN65HVD234 CAN transceiver (Texas Instruments, 2002).

4.2.5 Board to Board Connector

The Hirose DF17(2.0)-040DP-0.5V(57) Board to Board Connector is a 0.5 mm contact pitch with 40 contacts. The dimensions are shown in Figure 4.15. This connector has enough contacts that allow to have CAN, I2C and UART communication buses as well as 5 pins for power.

A	B	C	D	E	F	G	H	RoHS
15.0	11.7	10.6	9.5	12.0	14.8	4.3	2.0	YES

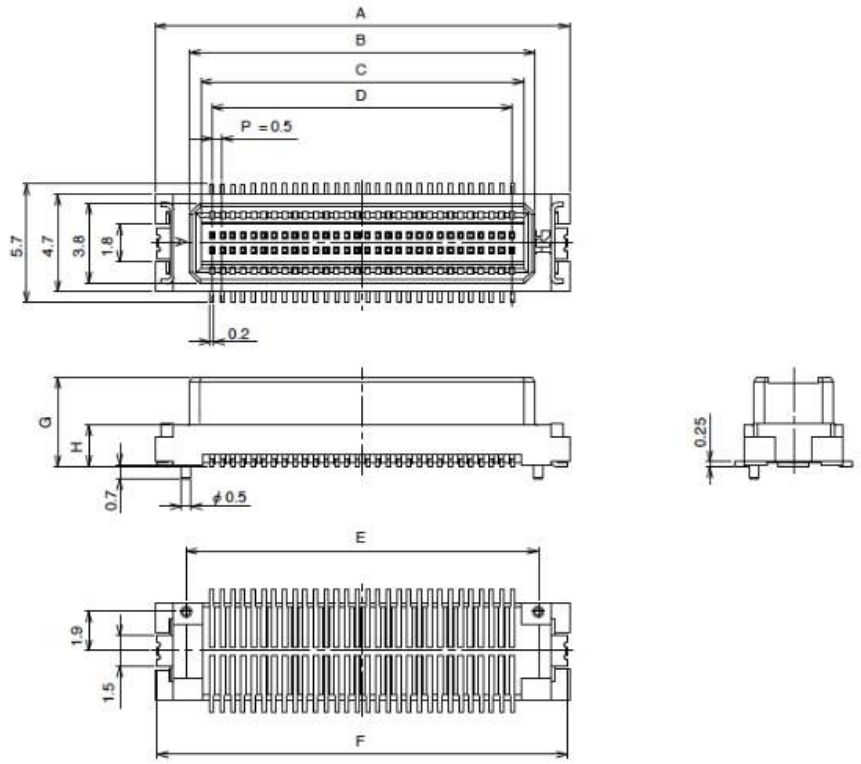


Figure 4.15: DF17 Board to Board Connector dimensions (Hirose).

4.3 PCB layout design guidelines

A Printed Circuit Board (PCB) provides a physical support and an electrical connection to the components that form a circuit. PCBs are formed by several conductive layers laminated onto and between sheet layers of a non-conductive substrate. The substrate provides insulation between the conducting layers and it is usually fiberglass FR4 (fire retardant) since it gives the PCB rigidity (Essentra Components, 2018). In these layers, there are traces and vias that allow to electrically connected the different components.

In this section, several guidelines that should be taken into account when designing the PCB layout are explained.

4.3.1 Layers

When designing the PCB layout, one should be aware of the different layers that form the PCB and what is the function of each one. Here the available layers in the KiCad software are described (KiCad, 2014):

- Copper layers: these layers are meant for placing and re-arranging traces. Furthermore, the external copper layers are also component layers because they are the only ones in which components can be placed.

  KiCad allows to have from 1 copper layer (single-layer board) up to 32 copper layers (multi-layer board). Moreover, single-layer boards are those boards that have all of the traces routed on one side of the board while double-layer boards have traces on both sides.

- Paired Technical layers: they come in pairs, one in the front and one in the back and they include:

  → Adhesive: used in the application of adhesive to stick surface mount components to the circuit board.

  → Solder Paste: used to produce a mask, also called stencil, to deposit solder paste on the pads of the components before reflow soldering.

  → Silk Screen: these are the layers in which the drawings of the components appear.

  → Solder Mask: these layers define the solder masks and all pads should appear either on one of these layers, for surface mount components, or both, for through hole components.

  → Courtyard: used to show how much space a component physically takes on the PCB.

  → Fabrication: used for documentation purposes.

- Edge and Margin layers: these layers are reserved for the drawing of the board outline. Any element placed on this layer appears on all the other layers.

- Layers for general use: these layers can be used for text, such as instructions for assembly or wiring, or construction drawings.

During layout, special attention should be given to the copper layers. It is recommended that at least one of the layers is reserved for ground and one for the main power,

and that they are placed adjacent in order to reduce impedance (Dialog Semiconductor, 2015). Also, all unused PCB areas should be flooded with ground since this further reduces ground impedance (Dialog Semiconductor, 2015)

Moreover, thermal management is an important consideration because improperly managed heat issues can degrade and damage a PCB. Also, using a thermal relief pattern for all pads connected to ground or power planes can prevent cold solder joints (Hausherr, 2007). When using thermal relief, the pad is connected to the plane by four track segments, whose parameters can be adjusted as seen in Figure 4.16.

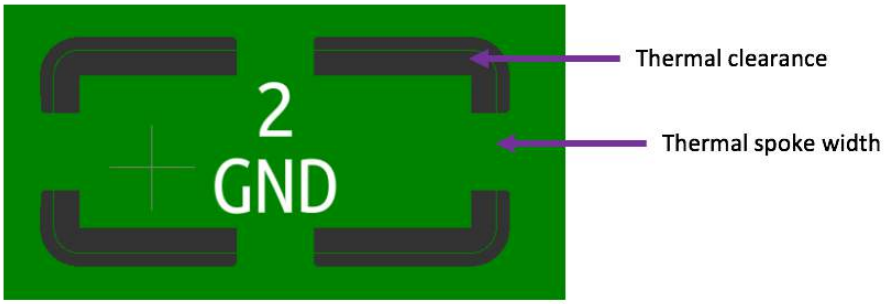


Figure 4.16: Parameters for thermal relief in pad.

Finally, PCB manufacturers such as Eurocircuits specify the minimum thickness for copper layers as 20 μm (Eurocircuits, 2019).

4.3.2 Traces

In PCBs, traces are the equivalent of a wire. There are three types of traces: signal, power and ground. Signal traces are usually narrower than power or ground traces since current-carrying traces should be as thick as possible (Dialog Semiconductor, 2015). However, in the case of high current input supplies, it is recommended to use plane shapes in stead of traces (Dialog Semiconductor, 2015).

For PCB traces, inductance increases with increasing length and decreases, although at a slower rate, with increasing width. Therefore, shorter and thicker traces are preferred (Texas Instruments, 1999). For this reason, always try to place components that need to be connected as close as possible to each other. However, this is not always possible so give priority to critical parts such as switching inductors and their capacitors as well as crystals (Dialog Semiconductor, 2015).

Moreover, special attention should be given to loops when routing traces. Lops behave as antennas that cause electromagnetic interference (Texas Instruments, 1999). A signal and its return path form a loop. Also a loop is formed where there is more than one return path in the ground of a load, this is called a ground loop (Dialog Semiconductor, 2015). Furthermore, the parasitic effect increases with the loop area, therefore, it is important to reduce the loop area as much as possible (Texas Instruments, 1999). Ground loops are best avoided by wiring all return paths within the circuit by separate paths back to a common ground point (Zumbahlen, 2008). Also, placing the trace closer to the ground plane reduces the loop area, hence it is recommended to place signal traces directly on ground planes whenever possible (Altium, 2018).

Finally, PCB manufacturers such as Eurocircuits specify the minimum trace width as 0.10 mm and a minimum space between traces, also known as margin, as 0.1 mm. Also, minimum clearance between the traces and the edge of the board of 0.25 mm for the outer layers and 0.4 mm for the inner layers is needed (Eurocircuits, 2019).

4.3.3 Vias

Vias are holes that go through the plane of one or more adjacent layers allowing electronic connections between those layers. KiCad handles 4 types of vias that are explained here and can be seen in Figure 4.17 (KiCad, 2014)):

- Through vias: used to connect the top layer with the bottom layer, crossing all the inner layers.
- Blind vias: used to connect one of the outer layers with one or more inner layers.
- Buried vias: used to connect inner layers, without touching the outer layers.
- Micro Vias: like blind vias but restricted to the nearest inner layer. They are intended to connect BGA pins and their diameter is usually very small.

Vias function as conductive paths through which electrical signals are passed between circuit layers (Millennium Circuits Limited, 2019). However, distortion occurs when the signals propagate through vias to horizontal transmission lines. Vias have a discontinuity effect which causes noise in the signal (Zenteno, Reina, and Regalado, 2010). This discontinuity effect should be taken into consideration for signal integrity.

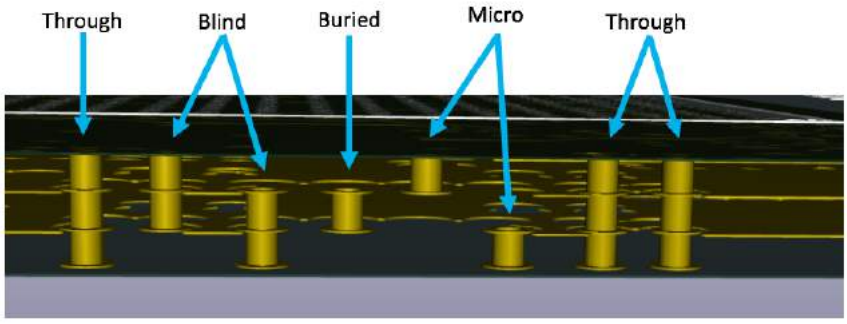


Figure 4.17: Types of vias in KiCad.

Moreover, PCB vias are inductive at high frequencies and will therefore increase the layer impedance. For this reason, it is recommended to have multiple vias in a plane since they will reduce this effect. Moreover, these vias must be spaced in such a way that the plane is not excessively divided (Dialog Semiconductor, 2015).

Finally, PCB manufacturers such as Eurocircuits specify the minimum diameter for vias as 0.25 mm, although they recommend to use 0.30 mm or above (Eurocircuits, 2019). Also, it needs to be noted that blind, buried and micro vias are more difficult to make and they add considerably to the cost of a PCB. Therefore, it is recommended to void them when possible and only used them if completely necessary (Eurocircuits, 2018).

4.4 Reflow soldering process

The two major soldering processes involved in surface mount technology (SMT) are wave soldering and reflow soldering. One of the drawbacks of wave soldering is that it can cause damage due to thermal shock when the components are directly exposed to the hot solder wave (Lee, 2002). Also, with wave soldering, adhesives have to be used to secure the components in place, therefore, the wave soldering process requires more steps. For these reasons, the reflow soldering process is chosen for soldering the components of the OBC of DTUSat-3.

In reflow soldering a solder paste is used to solder the components to the pads of the board. This solder paste is deposited, usually through stencil printing, onto the PCB pads where the SMCs are then placed. After that, the board is heated above the melting temperature of the solder paste so that it wets the pads and consequently forms the solder

joints (Lee, 2002).

In this section, the solder paste technology as well as the reflow thermal profile are explained and the different defects found in solder joints when using this type of soldering are described.

4.4.1 Solder paste technology

Solder paste is a creamy mixture obtained by blending two constituents: solder powder and flux.

- Solder powder: it forms the base of the metallic bond. The most typical binary alloy is tin (Sn) and lead (Pb), due to its eutectic properties, but other alloys include tin-silver, tin-indium, tin-antimony and lead-bismuth (Nguty, Ekere, and Adebayo, 1999). In general, for eutectic Sn-Pb alloy, a solder paste contains a fraction between 85% to 91% of metal alloy powder (Lee, 2002).
- Flux: it promotes metallic bond by providing good wetting conditions and cleaned surfaces, hence removing metal oxides as well as grease or metal carbonates during soldering (Nguty, Ekere, and Adebayo, 1999). The most commonly used fluxes include organic acids, organic bases, organic halogen compounds and organic halide salts (Lee, 2002).

The characteristics of the constituents of the solder paste affect the entire soldering process significantly, starting from the solder paste deposition to the reflow temperature profile itself (Nguty, Ekere, and Adebayo, 1999).

Finally, it is important to mention that the electronics industry is moving towards lead (Pb) free alloys due to the fact that lead is toxic for humans and a hazard for the environment (Apell, 2004; Shapiro et al., 2006). However, this Pb-free trend entails several reliability concerns when using it for aerospace applications. One of the main problems with Pb-free pure tin solder is the phenomenon known as whiskering (Figure 4.18), in which single crystals, with a typical length between 0.5 and 10 mm and a diameter between 1 and 5 microns, grow spontaneously from the solid tin. The filaments are highly conductive and can produce short-circuits. This way, when using Pb-free solder for aerospace applications, the appropriate mitigation techniques should be addressed (Baylakoglu, 2007).

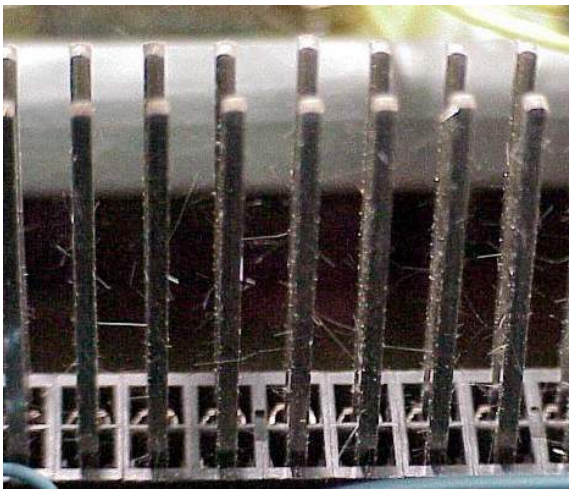


Figure 4.18: Whiskering phenomenon in pure tin solder (NASA).

4.4.2 Stencil printing

As mentioned before, one of the most common methods for solder paste deposition is through stencil printing. The reason for this is that the use of a stencil allows more precise control of the solder paste volume as well as better pattern registration and it is a much faster method (Lee, 2002). A stencil is a very thin metal foil with a pattern of aperture matching the footprint on the PCB where deposition of solder paste is desired (Nguty, Ekere, and Adebayo, 1999).

The process for solder deposition by stencil printing (Figure 4.19) starts with the placement of the stencil on top of the PCB with patterns registered properly. Then, the solder paste is wiped across the stencil with the use of a squeegee. Finally, the PCB is detached from the stencil, with solder paste deposited on top of the corresponding pads (Lee, 2002).

4.4.3 Reflow thermal profile

After the solder paste has been deposited and all the components are placed onto the PCB, the board is ready for reflow. A commonly used reflow thermal profile is shown in Figure 4.20, where four different stages can be recognized (Lee, 2002; Svasta and Simion-Zanescu, 2003):

1. **Preheat**: this phase brings the temperature of all components and board areas

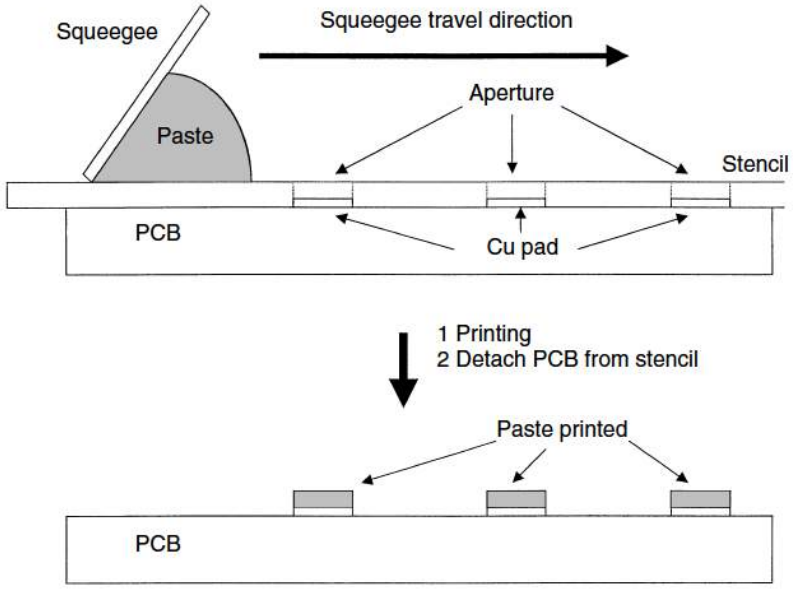


Figure 4.19: Schematic of the stencil printing process (Lee, 2002).

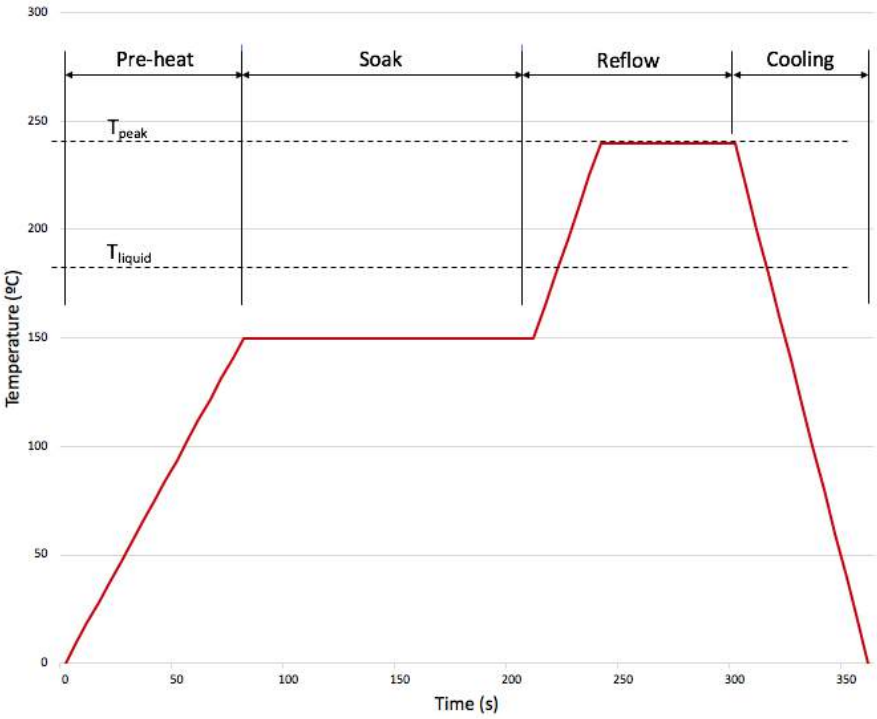


Figure 4.20: Reflow thermal profile.

to an equal level, which is below the solder paste melting point (T_{liquid}). Due to differences in thermal inertia, components do not heat up at the same speed, so

this preheat phase is needed before the reflow stage to ensure that all the solder paste starts melting at the same time. Moreover, the recommended maximum rate of temperature rise is between 2 to 4 °C/sec, to avoid component cracking and solder paste slump and scattering.

2. **Soak**: the purpose of this phase is to activate the flux in the solder paste and evaporate solvents. In general, a recommended temperature range is between 150°C and 175°C, depending on the solder paste, since most fluxes are activated above 150°C. Furthermore, the most commonly used soaking time ranges from 30 seconds to 2.5 minutes.

3. **Reflow**: during this phase, the temperature is increased to more than the solder paste melting temperature in order for the solder to flow properly. To obtain an acceptable joint quality, a minimum peak temperature (T_{peak}) between 200°C and 210°C should be reached. On the other hand, the maximum peak temperature allowed is dictated by the solder paste and the characteristics of the components and the PCB materials. If the peak temperature is too high, it can cause degradation of the PCB material and deterioration of electrical properties of components. Typically, the maximum peak temperature ranges from 230°C to 250°C.

4. **Cooling**: in this phase the board cools down to ambient temperature. Free air cooling is recommended in order to cool it down quickly and to avoid thermal stress. The recommended maximum rate of temperature fall is 4°C/s.

4.4.4 Defects in solder joints during reflow

In this section, the most common defects in solder joints due to reflow soldering are described (Lee, 2002; Lee, 1999; IPC, 2004).

- Solder balling

Solder balling (Figure 4.21) are small spherical particles that scatter away from the main solder pool. These particles are composed of the solder powder used in the solder paste and can produce short circuits or leakage currents. Solder balling is caused by a fast preheat rate, so, in order to prevent it, a slow preheat rate is recommended.

- Solder beading

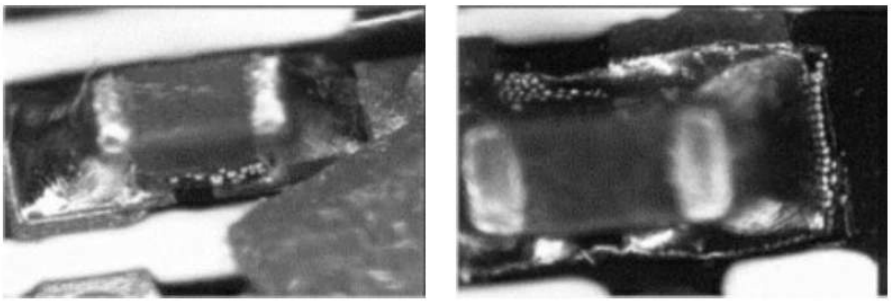


Figure 4.21: Solder balling (Lee, 2002).

Solder beading (Figure 4.22) is a special case of solder balling in which very large solder balls are formed around components with very low stand-off, such as chip capacitors or chip resistors. Solder beading is caused by flux outgassing which overrides the paste cohesive force and promotes the formation of isolated paste aggregates underneath the components, that melts during reflow forming the solder beads. As with solder balling, solder beading can be avoiding with a slow preheat rate.

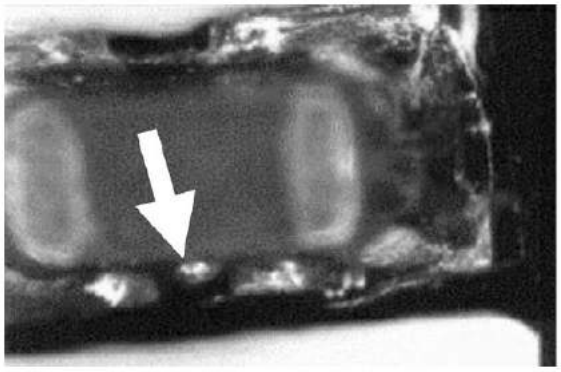
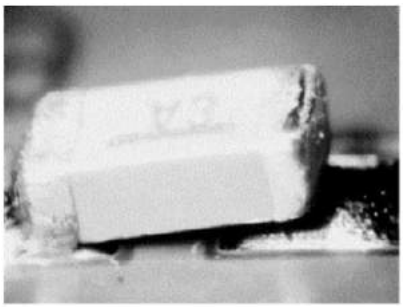


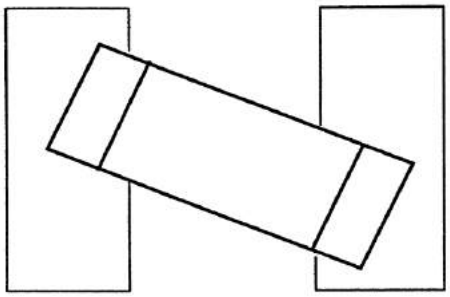
Figure 4.22: Solder beading (Lee, 2002).

- Tombstoning and skewing

Tombstoning (Figure 4.23a) is the lifting of one end of a leadless component, such as a capacitor or a resistor, that results in the component standing on its other end. On the other hand, skewing (Figure 4.23b) is the movement of a component in the horizontal plane that results in a misalignment of the component. Both phenomenons are caused by unbalanced wetting of the two ends of the component and can be minimized by using a very slow reflow rate to allow the temperature of the two ends of the component to reach equilibrium.



(a) Tombstoning.



(b) Skewing.

Figure 4.23: Tombstoning and skewing defects (Lee, 2002).

- Wicking

Wicking is a phenomenon where the molten solder flows up the lead away from the joint area, and as a result an open joint is formed, as seen in Figure 4.24. It is a result of the lead being hotter than the PCB pad during the solder melting stage. This can be prevented by allowing the temperatures of the leads and pads to reach equilibrium before any solder wetting occurs.

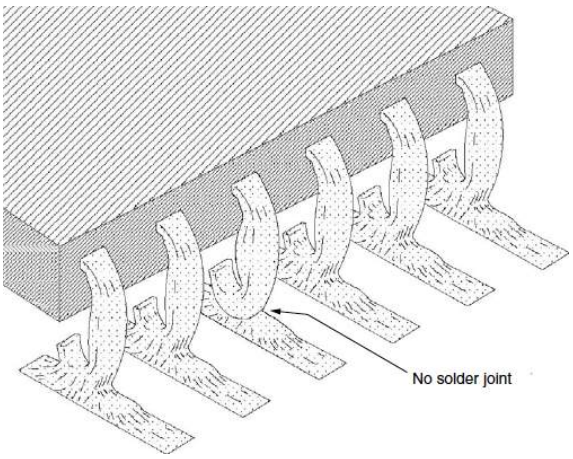


Figure 4.24: Wicking (Lee, 2002).

- Dewetting and nonwetting

In dewetting (Figure 4.25a), the surface is wetted initially but retracts after a time causing the solder to collect into discrete balls. Dewetting is characterized by irregularly shaped mounds of solder separated by areas covered with a thin solder film. On the other hand, in nonwetting (Figure 4.25b), the pad is not wetted by the solder and therefore the solder joint is not formed. Both defects happen due to excessive impurities in the solder

or inadequate cleaning prior to soldering. Therefore, application of a more aggressive flux or an abrasive cleaning of the surface can help to overcome these issues.

(a) Dewetting. (b) Nonwetting.

Figure 4.25: Dewetting and nonwetting (IPC, 2004).

- Leaching

Leaching (Figure 4.26) is a phenomenon in which the chip termination dissolves into the molten solder during reflow and, as a result, the solder joint may be saturated with these alien metals. It is caused by excessive peak temperature so it can be reduced by using a lower peak temperature.

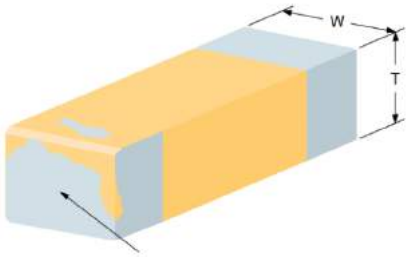


Figure 4.26: Leaching (IPC, 2004).

- Cold solder joints

Cold joints are joints that have an incomplete coalescence of solder powder due to an insufficient application of heat during reflow soldering process, either due to too low peak temperature or too short a time above the solder paste melting temperature. This way, in order to prevent cold solder joints, the reflow thermal profile should be adjusted to the specifications of the used solder paste.

4.5 X-Ray inspection of BGA solder joints

Ball Grid Arrays (BGA) are widely used because of their excellent characteristics such as better lead rigidity and self-alignment during the reflow soldering process (Ma et al., 2005). In conventional integrated circuits (IC), it is possible to detect defects in solder joints by visual inspection. For BGAs, however, visual inspection is limited to the peripheral solder joints since the rest are hidden under the IC package (Ma et al., 2005). Nowadays, the most useful method of assessing the quality of these hidden BGA interconnections is X-radiography (Wickham et al., 1999).

In this section, the process of X-ray imaging, several concepts that influence X-radiography and the most common defects in BGAs are described and explained.

4.5.1 Digital X-radiography technique

During an X-ray inspection, the component is placed between an X-ray tube that generates X-ray energy and a detection media. As the X-rays pass through the component, the different densities within the component absorb the X-rays in different amounts. The remaining X-rays pass through and hit the detector, which then converts X-rays to visible light and sends the result to the image processor. Finally, the image processor enhances the image for high resolution (Shang et al., 2008). If the component is placed perpendicular to the generated X-rays, the technique is called perpendicular transmission X-ray, while, if the component is placed with a certain angle to the generated X-rays, the technique is called angled transmission X-ray.

The resulting image is grey-scale where lighter areas correspond to least dense materials while darker areas correspond to denser materials. In the case of BGA inspection, the areas of the PCB where there are no tracks, pads or components are the least dense ones while the denser material is the tin/lead of solder joints (Wickham et al., 1999).

Furthermore, the geometric magnification (M) of the resulting image is calculated dividing the focus-detector distance (FDD) by the focus-object distance (FOD). Therefore, the smaller the focus-object distance, the greater the magnification, as it can be seen in Figure 4.27. Moreover, a better resolution of the X-ray image is obtained with a smaller focal spot of the source (GE Healthcare, 2011).

It needs to be noted that this type of technique does not allow cross-sectional imaging.

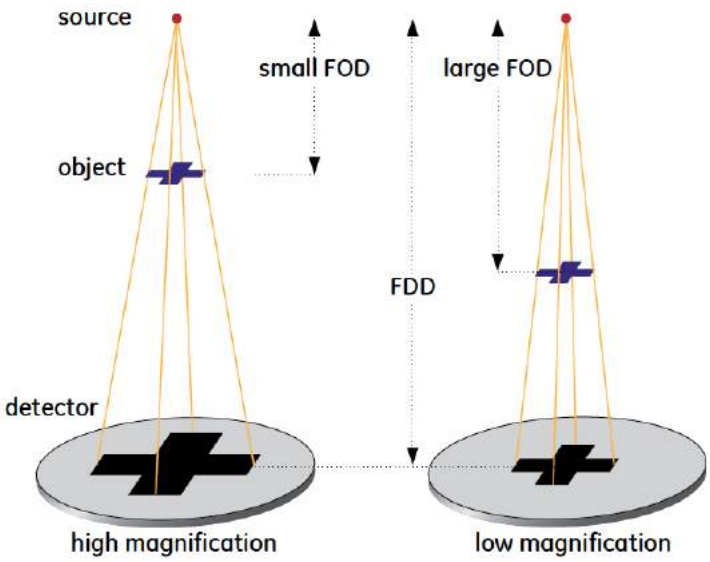


Figure 4.27: Geometric magnification of X-ray image (GE Healthcare, 2011).

Therefore, when using perpendicular transmission X-ray, the areas above and below very dense materials are masked, as shown in Figure 4.28.

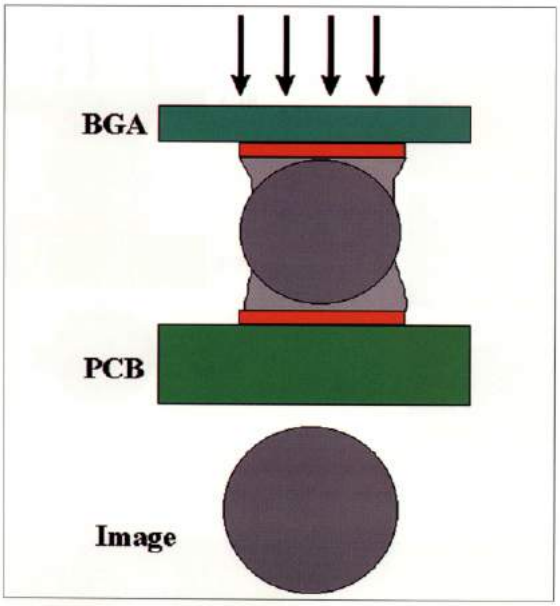


Figure 4.28: Image formation with X-ray (Wickham et al., 1999).

4.5.2 Stages of BGA reflow soldering

In this section, the three stages of BGAs during reflow soldering (Figure 4.29) are described to understand how they affect the X-ray imaging (Zweig, 2003; Zweig, 2002):

- Stage A: is the phase in which the BGA is placed on the PCB which can result in a complete or partial alignment between both. In this stage, the diameter of the balls in the X-ray image is equal to the nominal ball diameter.
- Stage B: also referred to as initial collapse, corresponds to the initial melting, in which solder balls start flowing through their pads. When all the balls have melted, the package is pulled into accurate alignment with the pads. In this stage, the solder balls acquire an elliptical shape that can be appreciated in an X-ray image.
- Stage C: also referred to as final collapse, is the phase in which the solder wets the pad completely after the alignment. In this stage, the solder balls return to a round shape and uniformity is achieved.

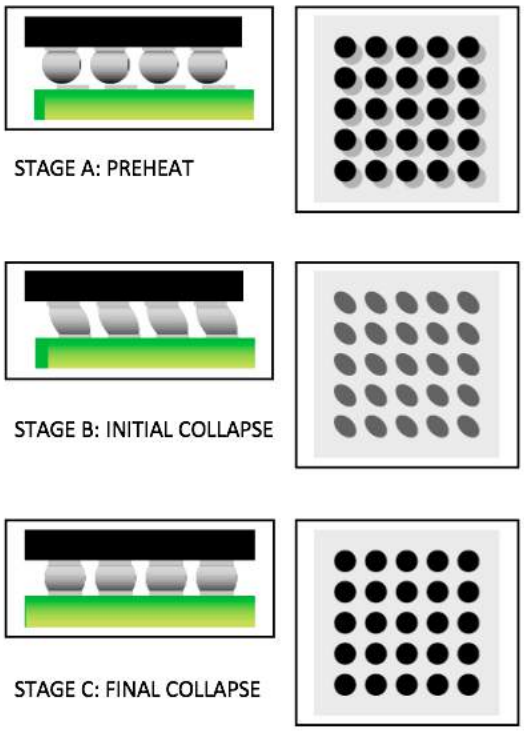


Figure 4.29: Stages of BGA reflow soldering (Zweig, 2003).

4.5.3 Uniformity

Uniformity refers to the fact that BGA balls in X-ray images are uniformly circular and equal in area, as it can be seen in Figure 4.30 . It provides the first and most important characterization of the quality of BGA bonds when using X-ray inspection.

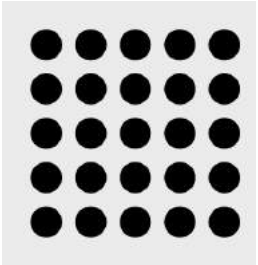


Figure 4.30: BGA uniformity, the ideal reflow result (Zweig, 2003).

4.5.4 Teardrop pad design

Some defects are highly difficult to detect with perpendicular transmission X-ray, mainly the ones in the areas around the edges of the pads, because the solder in the ball of the joint stops most X-rays. For this reason, the teardrop pad design is used. In this design, the pad is shaped as a teardrop by allowing a small portion of the track connected to the pad to be exposed. This allows to determine if the solder paste has wet the entire pad or not, because, if the pad is completely wet, it creates a distorted ball shape, which is easily seen in the X-ray image. This principle is represented in Figure 4.31 (Wickham et al., 1999).

4.5.5 Defects in BGA solder joints

In this section, the most common defects in BGA solder joints are described and their signatures in X-ray images are analyzed (Zweig, 2003; Zweig, 2002; Wickham et al., 1999; Yunus et al., 2000; Shang et al., 2008; Shang et al., 2008; ECSS, 2008).

- Misalignment

Due to an imprecise placement process of the BGA, the balls in the BGA may not be aligned with the pads in the PCB. The result in an X-ray image can be seen in Figure 4.32.

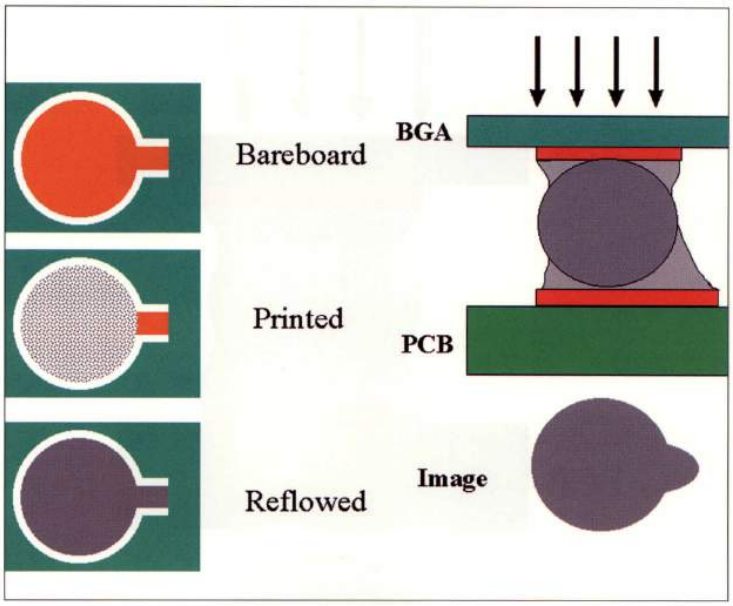


Figure 4.31: Teardrop pad design concept (Wickham et al., 1999).

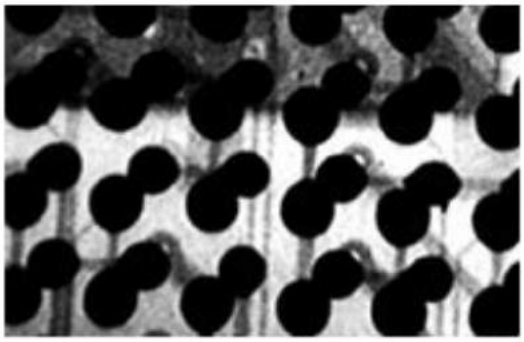


Figure 4.32: Misalignment of the BGA (Zweig, 2003).

- Missing balls

Due to problems during the manufacturing or soldering process, some balls in the BGA may be missing. The result in an X-ray image can be seen in Figure 4.33.

- Non-wetted pads

When applying the solder paste to the PCB, it may not wet all the pads and, as a result, certain balls in the BGA are not soldered to the PCB. This is difficult to see with perpendicular transmission X-ray. However, it can be eased with the teardrop pad design, since the defect will appear as a lack of the tear-drop shape, as it can be seen in Figure 4.34.

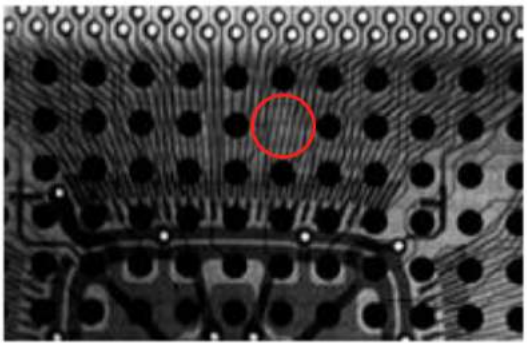


Figure 4.33: Missing ball in the BGA (Zweig, 2003).

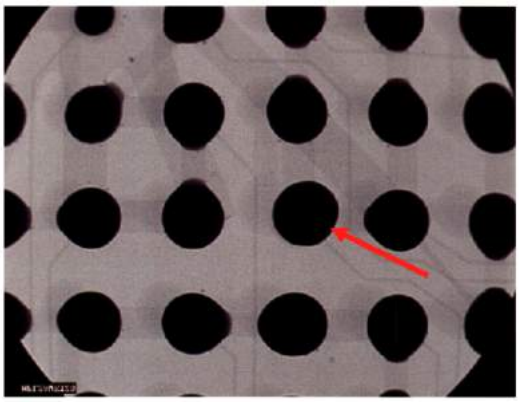


Figure 4.34: Non-wetted pads (ECSS, 2008).

- Bridges

Due to an excess of solder paste, some of it may stay in the space between pads which then melts during reflow to create a short-circuit between two balls. The result in an X-ray image can be seen in Figure 4.35.

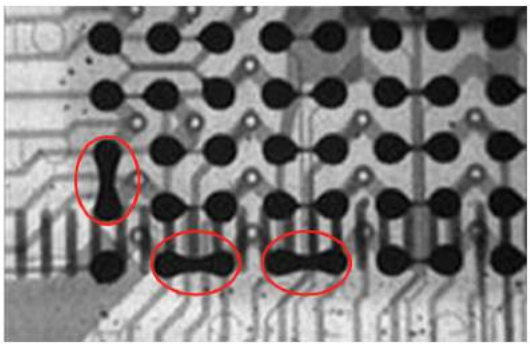


Figure 4.35: Bridges between pads in the BGA (Zweig, 2003).

- Insufficient reflow

As explained in the previous section, during stage B of reflow, the solder balls acquire an elliptical shape until complete alignment occurs, when they return to a round shape. However, if full reflow is not achieved, i.e stage C is not reached, this alignment will not occur and the balls in the X-ray image will appear elliptical, as it can be seen in Figure 4.36.

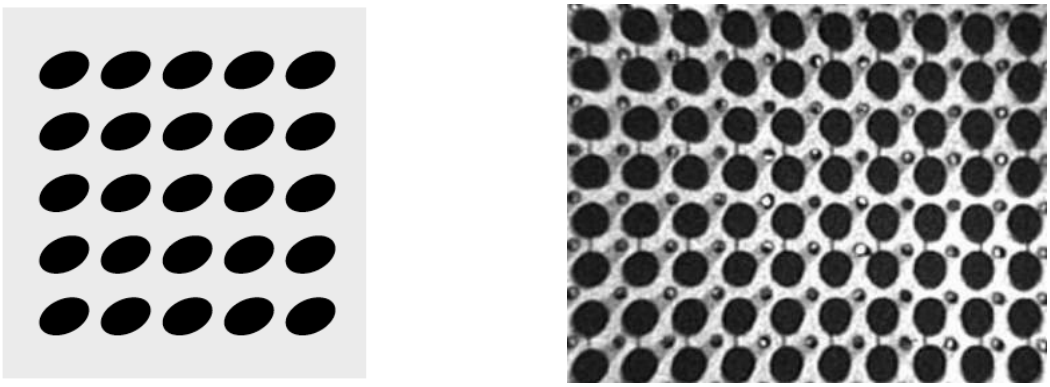


Figure 4.36: Insufficient reflow (Zweig, 2003).

- Doming and dishing of the BGA package

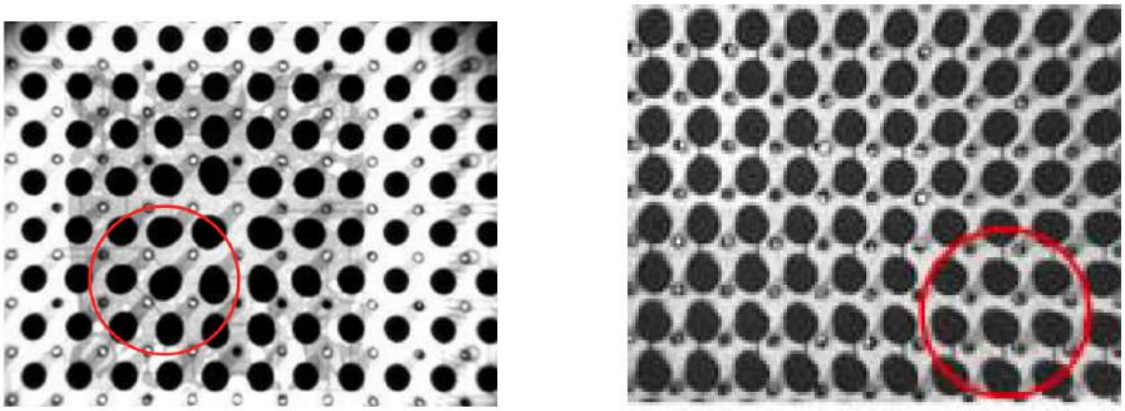
Doming and dishing are both caused by physical deformation of the BGA package due to either moisture or excessive topside temperature. In doming, also referred to as popcorning, the package domes in the center, enlarging the bonds under that area, as it can be seen in Figure 4.37a. Dishing, also referred to as potato chipping, is the opposite effect as doming, in which the BGA edges lift up. This pulls and thins the bonds on the perimeter and squashes the center bonds, as it can be seen in Figure 4.37b.

- Cold solder joints

This type of defect occurs when the reflow process fails to heat the solder paste enough to make it properly flow between the BGA ball and the PCB contact, which results in a poor solder contact. Cold solder joints are more difficult to identity in X-ray images but their common signature is bonds having irregular edges around the perimeter, as it can be seen in Figure 4.38.

- Solder voids

Solder voids are cavities or bubbles formed in the solder joints due to either out-



(a) Doming. (b) Dishing.

Figure 4.37: Defects caused by physical deformation of the BGA (Zweig, 2003).

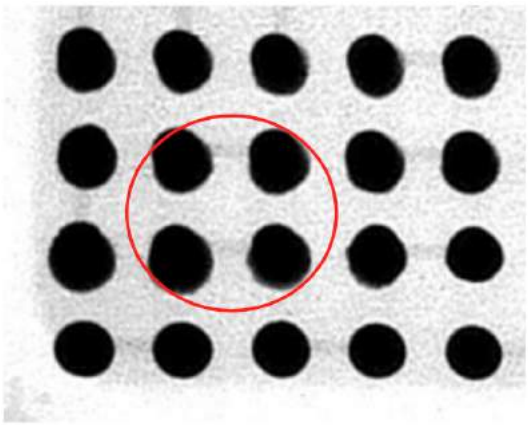


Figure 4.38: Cold solder joints (Zweig, 2003).

gassing flux or contaminants that get trapped during reflow. These gas bubbles have a lower density than molten solder paste which makes them rise to the top of the solder joints. Therefore, they are detected through X-ray inspection where they appear as lighter spots inside the solder balls. This can be seen in Figure 4.39. Solder voids are specially problematic because they affect the conducting performance of the solder joint, which at the same time can cause issues with thermal management and signal interference.

4.6 Linux boot process

This section explains the boot process of the Linux image running on the Octavo OSD335x SiP, and it is based on the application notes *OSD335x Lesson 2: Linux Boot*

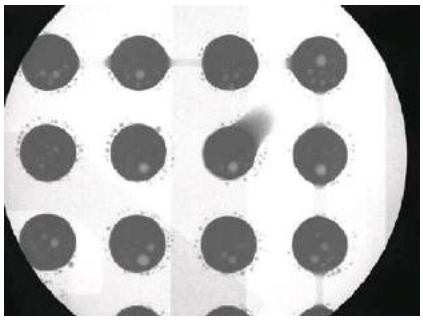


Figure 4.39: Solder voids (ECSS, 2008).

Process with the OSD335x and *OSD335x EEPROM During Boot* from (Octavo Systems, 2015).

To boot Linux, one of the most common methods is to use Universal Boot Loader (U-Boot) to perform all of the steps necessary to load and boot the Linux kernel. U-Boot environment requires more memory than is available in the AM335x internal memory. Therefore, U-Boot is split into a first-stage and second-stage bootloader. This split is done automatically during the building process for U-Boot, but the pieces are loaded into separate parts of the boot image.

Furthermore, the AM335x processor inside the OSD335x uses a four-stage boot process to load and run the operating system. The four boot stages for a standard Linux boot are explained next, and are shown in Figure 4.40.

- Stage 1: ROM bootloader

The Read-Only Memory (ROM) inside the AM335x is in charge of implementing the first stage bootloader, which corresponds to the first code that is executed by the processor when it is released from reset. The ROM bootloader code initializes the boot peripherals, such as the memory section, the watchdog timer and the system clocks; loads the next stage bootloader into the internal RAM of the AM335x and begins its execution.

- Stage 2: Secondary Program Loader (SPL)

The second stage of the OSD335x Linux boot process corresponds to the first stage of the U-Boot bootloader. It operates entirely within the internal memory of the AM335x processor since only the boot peripherals have been initialized by the first stage. The main function of the SPL is to perform the hardware initialization of the DDR3 memory within the OSD335x, load the full version of U-Boot into the DDR memory and begin the

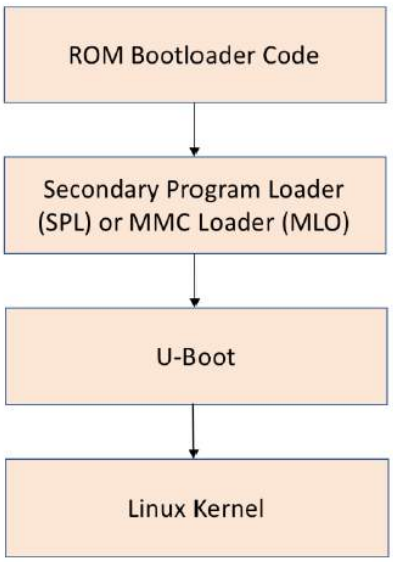


Figure 4.40: Linux Boot stages on OSD335x (Octavo Systems, 2015).

execution of that code.

- Stage 3: U-Boot bootloader

The third stage of the OSD335x Linux boot process corresponds to the second stage of the U-Boot bootloader, which is in charge of loading and beginning the execution of the Linux kernel. In order to do this, U-Boot looks for a *uImage* file, which can be found in non-volatile memory such as a micro-SD card. The *uImage* file (Figure 4.41) contains both the Linux kernel and a header that describes the kernel.

- Stage 4: Linux Kernel

In this final stage, the Linux kernel is started, which boots and configures the Linux operating system. The kernel also loads and configures all the necessary device drivers so that the system can operate properly.

4.6.1 Boot process memory usage

First of all, the ROM Bootloader stays permanently on the AM335x processor and cannot be modified. Before the device powers up, the BeagleBoard boot image, which contains the second and third stage bootloaders, the Linux kernel and the file system,

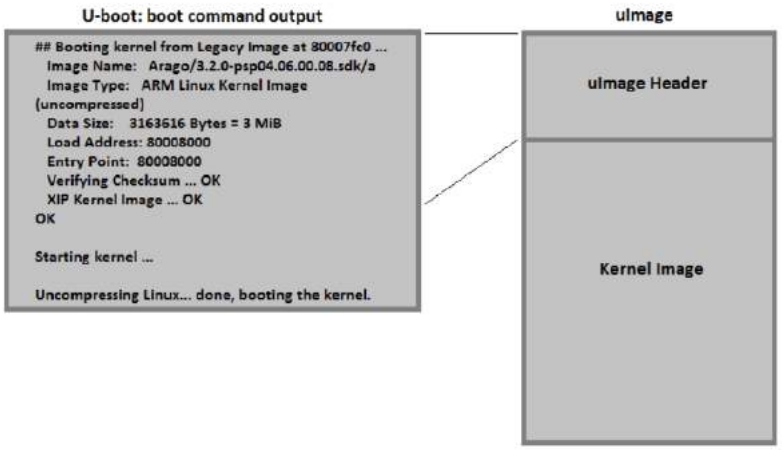


Figure 4.41: uImage header info displayed by U-Boot (Octavo Systems, 2015).

resides in the microSD card. Once the device powers up, the ROM Bootloader loads the SPL into the internal AM335x memory. After that, the SPL loads the U-Boot into the DDR3 memory inside the OSD335x device. Finally, the Linux kernel is pulled into the DDR3 and executed. At this point, the Linux operating system will run using all of the resources of the AM335x and the OSD335x as well as continuing to use the non-volatile storage as the file system, as it is shown in Figure 4.42.

4.6.2 EEPROM during boot and board ID

It is important to notice that the U-Boot bootloader within the BeagleBoard boot image looks for a board ID in an EEPROM attached to the I2C0 bus before booting the Linux kernel. This board ID is used by U-Boot to identify the printed circuit board on which it is running so that software drivers can be properly configured and loaded. This makes U-Boot more flexible and allows a single U-Boot image to be used for many different development platforms.

If U-Boot cannot find the board ID in the EEPROM, either because the EEPROM is blank or it has not yet been programmed, or if there is no EEPROM on the board, then U-Boot will not boot the Linux kernel. This is especially problematic because this check occurs before the serial console has been initialized so no boot messages will be displayed on the UART0 serial console.

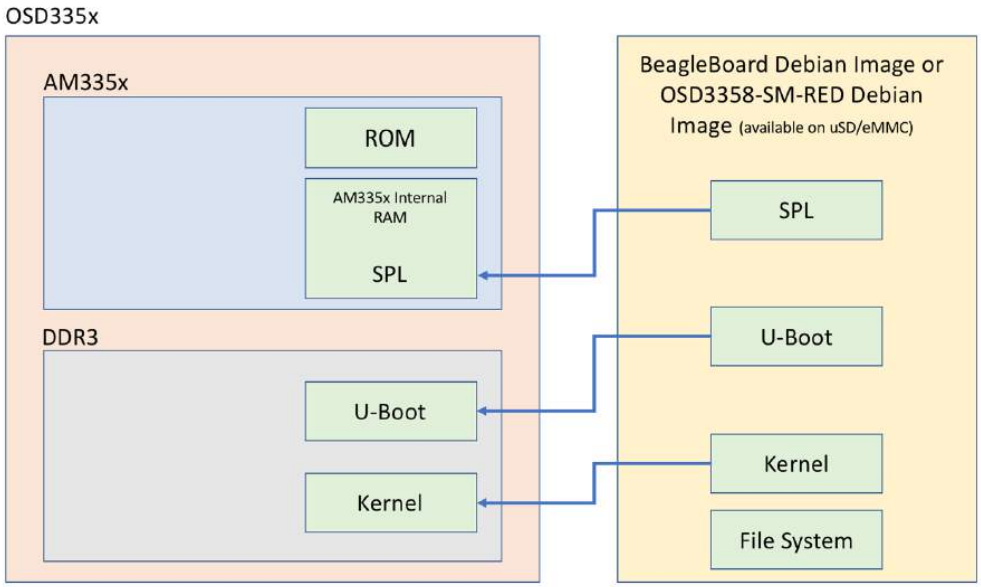


Figure 4.42: Boot Process Memory Usage (Octavo Systems, 2015).

4.6.3 Linux device tree

The board ID mentioned before enables U-Boot to load the corresponding device tree. A device tree is a tree data structure that describes the hardware configuration of the system to the Linux operating system. During boot, the Linux kernel will use the information in the device tree to recognize, load appropriate drivers and manage the hardware devices in the system.

A Linux device tree begins from a root node and consists of one level of child nodes and one or more levels of children nodes. Each child node represents a hardware component of the processor, which in this case is the AM335x processor. Each child node or children node can have only one parent and the root node has no parent. For the PocketBeagle board, each child node represents a component of the AM335x processor, such as the CPU, the I2C peripheral and so on. Then, each children node represents a sub-component of a child node or a device that is attached to the child node. For the PocketBeagle board, the TPS65217C PMIC is attached to the I2C0 peripheral bus of theAM335x processor hence it appears as a children node under the I2C0 child node.

4.7 Failure mode analysis

In this section, the two most common analysis techniques for system reliability are described and explained for their later used in the project. In particular, the Failure Mode and Effects Analysis (FMEA) and the Failure Mode, Effects and Criticality Analysis (FMECA) are studied. These methodologies identify ways a product, process or system can fail in order to efficiently define mitigation measures to reduce risk (IEC, 2006), starting with the highest priority ones which are related to failures having the most critical consequences (ECSS, 2009).

The reasons for undertaking this type of analysis include:

1. Identify those failures that have unwanted effects on system operation, such as degrade operation or affect the safety of the user.
2. Satisfy contractual requirements of a customer.
3. Allow improvements of a system's reliability and safety, by designing quality assurance actions.
4. Allow improvements of a system's maintainability, by highlighting areas of risk.

This analysis is preferably performed early in the development cycle, so that removal or mitigation of the failure mode is most cost effective (IEC, 2006).

4.7.1 FMEA

The ECSS-Q-ST-30-02C standard (ECSS, 2009) describes the Failure Mode and Effects Analysis (FMEA) as the analysis by which each potential failure mode in a system is analyzed to determine its effects. Here, the term system is used as a representation of a product, a function or a process. By identifying the effects of potential failures, one can develop measures to ensure that all system reliability and safety objectives are fulfilled (Mozaffari et al., 2013).

A FMEA is applicable to various levels of system decomposition, from the highest level of block diagram to the functions of discrete components. Therefore, FMEA can be classify as (Mozaffari et al., 2013; ECSS, 2009):

- System FMEA: it examines system deficiencies caused by potential failures between

the functions of the product. It focuses on system-related issues such as: integration, interactions and interfaces between subsystems.

- Design FMEA: it analyzes the components and subsystems used in the implementation of the product functions to ensure that the product operation is safe and reliable during the useful life of the equipment.

- Functional FMEA: it focuses on the intended function that a product must perform rather than the characteristics of the specific implementation.

- Process FMEA: it examines the ways that failures in processes, such as manufacturing, assembling and integration or pre-launch operations, can affect the operation and quality of a product. It can be performed at any level from limitations in equipment to operators training.

Furthermore, FMEA classifies the different failure modes according to their severity in order to prioritize the removal or mitigation actions. The ECSS-Q-ST-30-02C standard (ECSS, 2009) designates four severity levels depending on the effects and implications of a failure. These levels, as well as the dependability and safety effects associated to them (ECSS, 2017), are described in Table 4.5.

4.7.2 FMECA

The ECSS-Q-ST-30-02C standard (ECSS, 2009) describes the Failure Mode, Effects and Criticality Analysis (FMECA) as a FMEA extended to classify potential failure modes according to their criticality. In this sense, criticality corresponds to a combined measure of the severity of a failure mode and its probability of occurrence.

A failure mode can be classified according to its criticality by calculating its criticality number as follows. First, similar to the FMEA, a severity number, which depends on the severity level, is assigned to each failure, as specified in Table 4.6. Then, each failure is identified by a probability number, which depends on the probability level, as specified in Table 4.7. Finally, the criticality number is calculated as the severity number times the probability number. This way, the larger the criticality number, the higher the criticality of the failure. Furthermore, a failure is considered critical either if it is classified as catastrophic, or if its cirticality number is greater than or equal to 6. Table 4.8 specifies the levels of criticality in relation to the severity and probability numbers.

Severity category	Severity level	Failure effects	
		Dependability effects	Safety effects
Catastrophic	1	Failure propagation	• Loss of life • Permanently disabling injury or illness • Loss of an interfacing manned flight system • Severe detrimental environmental effects • Loss of launch site facilities • Loss of system
Critical	2	Loss of mission	• Temporarily disabling injury or illness • Major detrimental environmental effects • Major damage to public or private properties • Major damage to interfacing flight systems
Major	3	Major mission degradation	
Minor or Negligible	4	Minor mission degradation or any other effect	

Table 4.5: Severity levels and consequences.

Severity level	Severity category	Severity number
1	Catastrophic	4
2	Critical	3
3	Major	2
4	Negligible	1

Table 4.6: Severity levels and numbers.

Probability level	Probability number
Probable	4
Occasional	3
Remote	2
Extremely remote	1

Table 4.7: Probability levels and numbers.

Severity category	Severity number	Probability number			
		1	2	3	4
Catastrophic	4	4	8	12	16
Critical	3	3	6	9	12
Major	2	2	4	6	8
Negligible	1	1	2	3	4

Table 4.8: Criticality matrix.

4.8 Radiation effects in space

Satellites are subject to radiation effects during flight operation. The severity of those effects vary depending on the orbit of the satellite since it depends on the particles that are present. For higher altitudes, the Van Allen radiation belts entail the greatest problems because they contain energetic protons and electrons. For lower altitudes and inclinations, the environment is governed by the South Atlantic Anomaly, where radiation is enhanced. All types of energetic particles cause radiation effects, but some of them contribute more than others (Fortescue, Swinerd, and Stark, 1992). Therefore, it is important to understand the environment in which DTUSat-3 will be operating in order to be able of mitigating the radiation effects.

For orbits between 550 km to 700 km of altitude, such as the one for DTUSat-3, the predominant particles are trapped protons (Fortescue, Swinerd, and Stark, 1992) and it is estimated that satellites are exposed to 1 to 10 krad radiation dose per year. In this section, the main radiation effects in EEE components as well as testing and mitigation techniques are explained.

4.8.1 Main radiation effects in EEE components

The three main radiation effects in Electrical, Electronic and Electro-mechanical (EEE) components are: Single Event Effects, Total Ionizing Dose and Displacement Damage (ECSS, 2012). These are explained next.

Single Event Effect (SEE)

Single Event Effects (SEEs) group all the possible effects induced by the passage of ionizing particles through sensitive electronic components (Paccagnella, Gerardin, and Cellere, 2009). The flux of particles varies with latitude, altitude and, to a lesser extent, with longitude, therefore SEE occurrence is based on probability (Gaillard and Nicolaidis, 2011). Single Event Effects (SEEs) induced by heavy ions, protons and neutrons become an increasing limitation of the reliability of electronic components. For this reason, improving the understanding of SEEs and developing mitigation techniques is crucial (Gaillard and Nicolaidis, 2011).

Moreover, SEEs are classified into hard and soft errors. Hard errors are non-recoverable errors while soft errors may be recovered by a power cycle, i.e. disconnecting the power for a period of time and then reconnecting it; a rewrite of the information or a reset (Gaillard and Nicolaidis, 2011).

Soft errors include, among others, Single Event Upsets (SEUs). SEUs occur when an ionizing particle modifies the state of a storage cell. In an SRAM or a flip-flop the state of the cell is reversed, while in a DRAM, the charge stored is slightly modified. All of these cause an error when the cell is read (Gaillard and Nicolaidis, 2011).

Hard errors include, among others, Single Event Gate Ruptures (SEGRs) and Single-Event Latch-Ups (SELs). SEGRs are caused by the passage of a heavy-ion through a biased MOS structure which results in the catastrophic breakdown of the gate oxide (Paccagnella, Gerardin, and Cellere, 2009). Moreover, SELs are latch-ups triggered by an SEU. SELs

are caused by activity of parasitic structures in bulk CMOS technology, in which some PNPN junctions switch to a low impedance state creating a a low impedance, high current path (Hansen and Tcherniak, 2017a).

Other types of hard and soft complex SEEs such as Digital Single Event Transients (SETs) and MCU Multiple Bit Upsets, are introduced in References (Johnston, 2001), (Paccagnella, Gerardin, and Cellere, 2009) and (Gaillard and Nicolaidis, 2011), and other lessons from CERN, NASA and ESA.

Total Ionizing Dose (TID)

Long term ionizing damage is the result of exposure to low-energy electrons and protons over a long period of time (Johnston, 2001). The Total Ionizing Dose (TID) induced effects are a major concern for the design and operation of electronic devices (Hsieh et al., 2016). Accumulative radiation effects can cause devices to suffer threshold shifts, increase in power consumption, leakage currents and noise, and change in timing. For this reason, monitoring the degradation suffered by devices is a must, specially in hostile environments such as space (Agustin et al., 2014).

Displacement damage (DD)

Displacement damage refers to the dislodging of atoms from their normal lattice sites (Srour and Palko, 2013). It is caused by lattice collisions between energetic protons or electrons, from solar flares or trapped radiation belts, that transfer sufficient energy to the lattice to move an atom out of its normal position (Johnston, 2001; Becker, Elliott, and Alexander, 2006). The resulting damage causes degradation of the electronic and optical properties of materials and devices (Srour and Palko, 2013), specially in certain types of optoelectronic devices like CCD image sensors, solar cells, laser diodes and LEDs (Hansen and Tcherniak, 2017b).

4.8.2 Qualification of commercial components

Since COTS components are the base for the design of the OBC for DTUSat-3, the entire board should be radiation tested in order to ensure proper operation over the lifetime of the satellite.

TID testing and mitigation

Cobalt-60 gamma rays is the standard and dominant method for TID testing. The reason for this is that it is simple, cost-effective and requires only little infrastructure (Hansen and Tcherniak, 2017b; Johnston, 2001). Even though gamma ray testing has several limitations, such as that there are no protons involved while high energy protons are abundant in the space environment, it has been proven to be a useful simulation of the penetrating electrons and protons in the space radiation spectrum. Moreover, gamma ray testing is one of the fastest methods since one can simulate years of radiation exposure in LEO in only a few hours (Hansen and Tcherniak, 2017b).

Moreover, in order to mitigate TID effects, aluminum shielding should be incorporated since electrons and low-energy protons are effectively attenuated by this type of shielding (Label, 2004).

SEE and DD testing and mitigation

Testing for SEE is done with high-energy protons or heavy ions, which require access to an accelerator, while DD testing is done using a neutron source (CERN, 2019). These tests are much more demanding and costly than TID testing (Hansen and Tcherniak, 2017a). For this reason, SEE and DD tests are not a possibility within the scope of this project, hence alternative ways to deal with these radiation effects are studied here.

In order to avoid SEEs, all systems sensitive to SEL should be protected using a stand-alone power-cycling circuit, similar to the one in Figure 4.43 (DTUSat, 2019). Also, SEU mitigation measurements include a redundant watchdog timer and an external reset connection (DTUSat, 2006). Finally, since no components in the OBC incorporate optoelectronic technology, mitigation measures against DD are not needed.

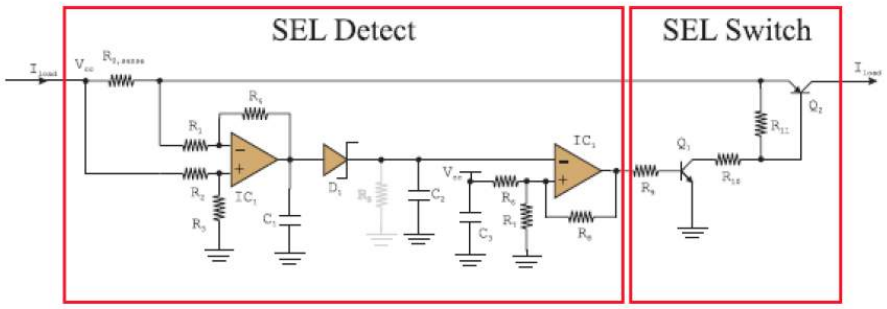


Figure 4.43: Circuit for single event latch up protection (DTUSat, 2019).

Chapter 5

System design and implementation

This chapter describes and explains the process of designing, soldering and inspecting the printed circuit board developed for the On-Board Computer of DTUSat-3 based on the insights given in Chapter 4: Theory.

5.1 DTUSat-3 On-Board Computer design

The design for the OBC of DTUSat-3 is based on the PocketBeagle board, which is described in Section 4.2.1, with several modifications in order to fulfill DTUSat-3 requirements. This approach allows to save time and money since the design does not need to start from scratch.

In this section, the components that form the computer as well as a block diagram of the OBC are presented. Moreover, a description of all the components and their functionality can be found in Section 4.2, while the bill of materials can be seen in Appendix E.

5.1.1 OBC Components

As mentioned before, the design for the OBC of DTUSat-3 is based on the PocketBeagle board. However, the PocketBeagle alone does not fulfill all the requirements for the DTUSat-3 satellite mentioned in Section 3. For this reason, several components were added to the board and are explained in this section.

In particular, the components that were introduced to the PocketBeagle original board are the following:

- CAN transceiver

A CAN transceiver is needed in order to enable CAN communication. The chosen device is the Texas Instruments SN65HVD234 CAN transceiver and the reasons are explained in Section 4.2.4.

- Subsystem Carrier Board (SSCB) stack connector

Even tough the PocketBeagle board is powered trough a USB port connected to a computer, the OBC for DTUSat-3 should be powered using the batteries inside the satellite. For this reason, the OBC needs to be connected to the Subsystem Carrier Board (SSCB) and for that a board-to-board connector is needed. The stack connector provides with 3.3 V to the board and also several communication buses. The chosen device is the Hirose DF17(2.0) and the reasons are explained in Section 4.2.5. Also, it needs to be noted that the USB is left in this first revision of the board for debugging purposes.

- Step-up converter

As explained in Section 4.2.2, the Octavo SiP can be powered by either an USB port at 5 V or a single cell battery at 3.7 V. Moreover, as mentioned before, the board should be powered using the stack connector while the USB port should be used just for debugging purposes.

This way, during normal operation of the satellite, the Electric Power Subsystem supplies the OBC with 3.3 V. Therefore, the second powering option could allow to connect the power coming from the stack connector directly to the Octavo SiP, so that the Octavo SiP sees the stack connector as a battery. However, this option cannot be used once the voltage drops below 3.5 V (Octavo Systems, 2017), hence feeding 3.3 V directly to the Octavo SiP is not possible.

The remaining option, on the other hand, is powering the Octavo SiP using 5 V, but the stack connector provides only 3.3 V. This means that a DC/DC step-up converter is needed to rise the voltage from 3.3 V to 5 V before reaching the Octavo SiP. For this, the chosen device is the Torex XCL103 step-up micro DC/DC converter and the reasons are explained in Section 4.2.3.

5.1.2 DTUSat OBC block diagram

Figure 5.1 shows a high level block diagram of the OBC for DTUSat-3, which is based on the PocketBeagle board. As it can be seen, the OBC includes the Octavo Systems OSD3358-SM System-in-Package (SiP), which at the same time includes the AM3358 processor, an EEPROM, a Power Management IC and a DDR3 memory; a microSD connector to store the Linux operating system, a USB 2.0 connector, four USER LEDs and a power LED, two expansion headers, a CAN transceiver, a step-up converter and a SSCB stack connector.

Other components also found on the board are: the Texas Instrument TPD4S012 Transient Voltage Suppressor, a crystal oscillator circuit, the Texas Instrument SN74LVC1G07 Single Buffer/Driver with open-drain and a power button, as well as ferrite beads, capacitors and resistors.

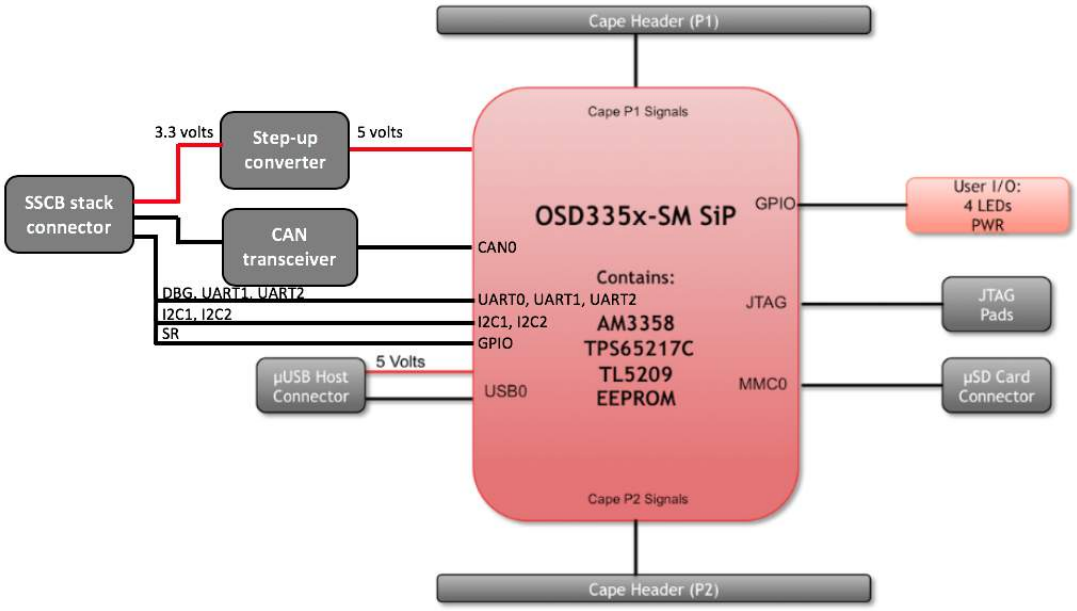


Figure 5.1: DTUSat OBC block diagram.

5.2 PCB design and layout

In this section, the design of the PCB for the OBC of DTUSat-3, which was developed using KiCad, is described. The design is divided into two parts: the circuit schematics and the PCB layout, which was developed following the guidelines mentioned in Section

4.3.

It needs to be noted that both the schematics and the layout design were developed using as a base the PocketBeagle board design which has a public license. This means that the KiCad schematic and layout design for the PocketBeagle board are available to the general public and my be used freely, with the condition that the BeagleBoard.org logo or trademarks are not used. Due to this public licensing, the design is not updated regularly. For this reason, all the components were reviewed beforehand in order to make sure that they were still commercialized. Just one of the components was outdated, the microSD card holder, therefore it was changed in this first revision of the board.

Finally, the components that were added to the base PocketBeagle design were: the XCL103D step-up converter, the SSCB stack connector, the CAN transceiver and the new microSD card holder. The circuit schematics as well as the PCB layout of all these components are explained next.

5.2.1 Schematics

First of all, the schematics of the circuits were developed, which can be found in Appendix F. As mentioned before, the designed is based on the PocketBeagle, therefore there is some circuitry that stayed untouched while other was changed or added. Here, just the new additions are explained since a detail description of the PocketBeagle schematics can be found in the *PocketBeagle System Reference Manual* (Kridner, 2019).

- microSD connector

The microSD card connector (Figure 5.2) is a 9 (8+1) position surface card connector. The first eight pins corresponds to communication pins while the last pin, pin 9, is a card detector pin. This pin detects when the card is inserted so that the access to the card can be initiated. This is done when the level on the pin is low and it is further explained in the layout design next.

Moreover, R10 and R11 are pull-up resistors while C6 and C5 are decoupling capacitors needed to stabilize the signals and reduce noise.

- SSCB stack connector

In the SSCB stack connector block (Figure 5.3) pins 1,3,5,7 and 9 are the 3.3 V input

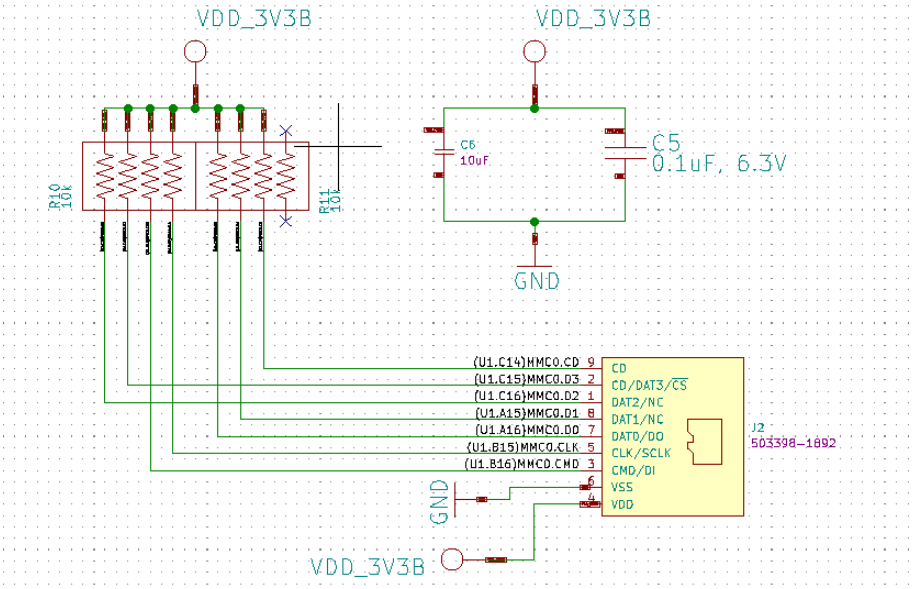


Figure 5.2: micoSD card connector schematics.

voltages, that are connected to the signal called *STACK_3V3*, while pins 6, 10, 14, 18 and 22 are connected to ground. The communication pins UART0, UART1, UART2, I2C1, and I2C2 are connected to their respective pins in the Octavo SiP, while the CAN Low and High signals are connected to their respective pins in the CAN transceiver. Finally, the SR signals are connected to General Purpose I/O pins in the Octavo SiP so that they can be programmed later as necessary. The rest of the pins are not needed, hence they are left unconnected.

It should be noted that the I2C protocol often needs pull-up resistors connected from the I2C lines to the supply voltage in order to pull the lines high when they are not driven low by the open-drain interface. However, in this design, the pull-up resistors are omitted because the lines are internally pulled up in the Octavo SiP. The pull-up resistors inside the Octavo SiP have a value of 4.7 kΩ.

- CAN transceiver

The CAN transceiver block can be seen in Figure 5.4. Pin 1, the CAN transmit data input, also called TXD; and pin 4, the CAN receive data output, also called RXD; are connected to the CAN0 TD and RD signals in the Octavo SiP, while pins 6 and 7 are the CAN Low and High bus lines respectively, that come from the SSCB stack connector. Moreover, pin 8 is the mode select pin, which, in this case, is selecting a low-power stand-by mode using a strong pull-up to the supply voltage via resistor R13 of value 10 kΩ. Pin

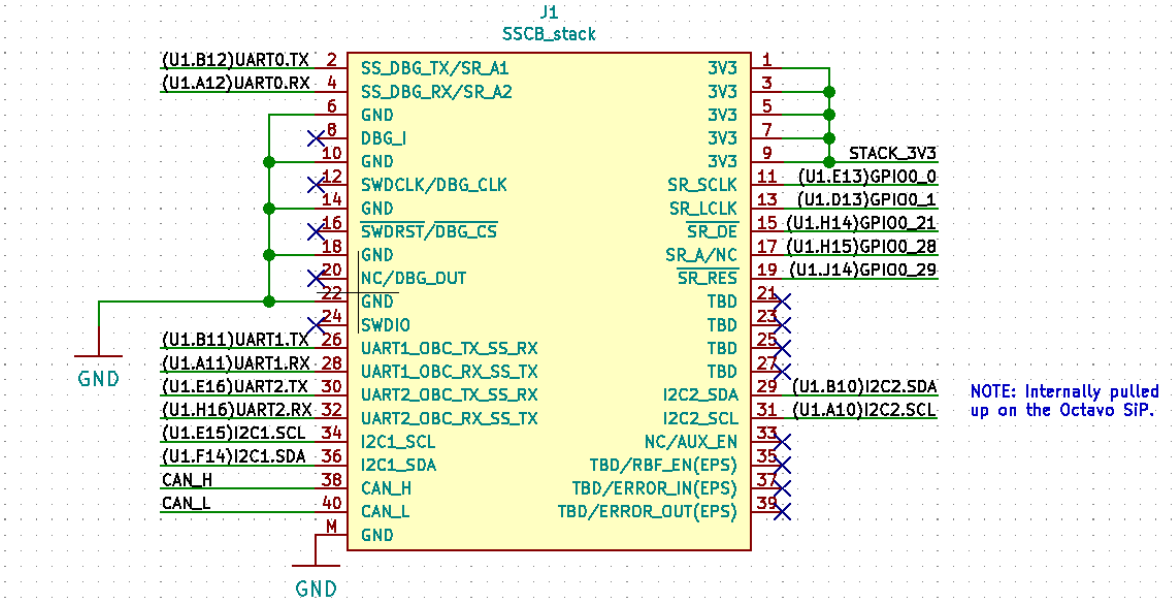


Figure 5.3: SSCB stack connector schematics.

5 is the enable input pin which is connected to a logic high, in this case a General Purpose I/O pin in the Octavo SiP that can be programmed afterwards, to enable a normal mode. Finally, pin 3 is the supply voltage pin which is connected to the input voltage coming from the SSCB stack connector while pin 2 is connected to ground.

It should be mentioned that capacitor C8 is placed as close to the VCC supply pin as possible, in order to ensure reliable operation at all data rates and supply voltages, and that it is a ceramic capacitor with a value of 100 nF, as specified in the datasheet.

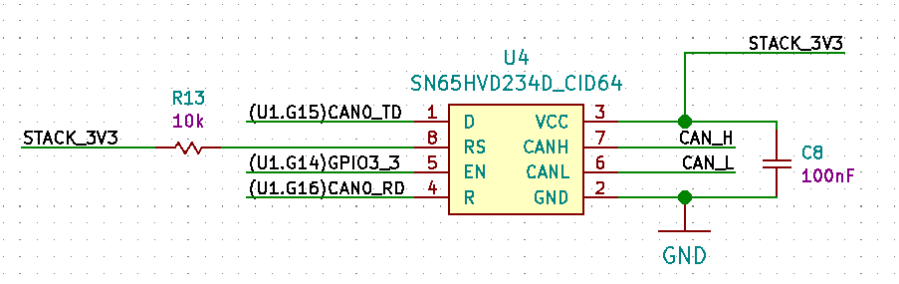


Figure 5.4: CAN transceiver schematics.

- Step-up Bus Converter

For this component, the symbol was designed from scratch using the Symbol Editor tool of KiCad. The designed symbol, as well as the a table with all the pins information,

is shown in Appendix H.

The step-up converter block has eight pins (Figure 5.5) and the schematics were done following the typical application circuit explained in Section 4.2.3. Pin 1, which corresponds to the input power, and pin 7, which correspond to one of the inductor electrodes, are both connected to the input power coming from the SSCB stack connector, while pin 6 is the output voltage that goes to the Octavo SiP (called signal VDD_5V). Moreover, pin 3 is the chip enable pin, which is always high, and pin 5, which is the switching pin, is connected to pin 8, which corresponds to the other inductor electrode. Finally, pins 2 and 4 are connected to ground.

It needs to be noted that the chip enable pin, pin 3, understands as high any voltage between 0.8 V and 6 V. For this reason, pin 3 is connected to a resistor (R14) of value 10 kΩ which allows to have a voltage of approximately 3.3 V, calculated following Equation 5.1 and knowing that the CE high current is 0.1 μA, as specified in the datasheet. Moreover, capacitors C9 and C10 were also selected according to the step-up converter's datasheet.

$$V_{CE} = V_{in} - R * I_{CE} = 3.3V - 10k\Omega * 0.1\mu A \simeq 3.3V \tag{5.1}$$

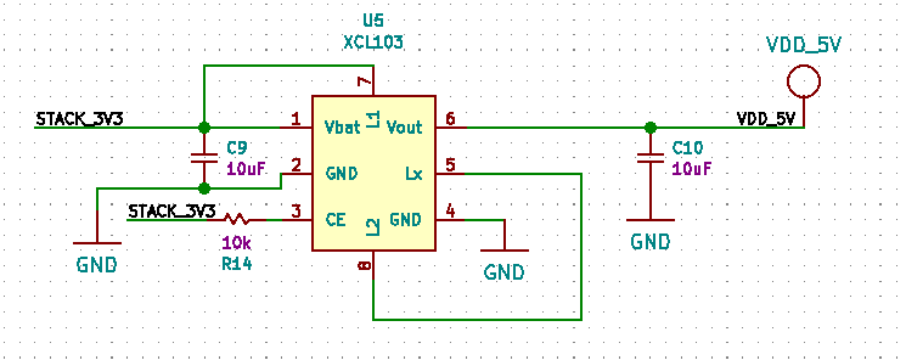


Figure 5.5: Step-up converter schematics.

5.2.2 Layout

The next step is to design the layout of the PCB, which is a multi-layer double-sided board. First of all, the PocketBeagle has a smaller size and a different shape than the one needed for DTUSat-3, whose dimensions are specified in Appendix C. Therefore, the size was increased to be 65 mm x 35 mm and the PCB shape was slightly modified as well as four holes were added. The two boards can be seen in Figure 5.6, where the white edge

corresponds to the PocketBeagle board and the yellow edge corresponds to the DTUSat OBC board.

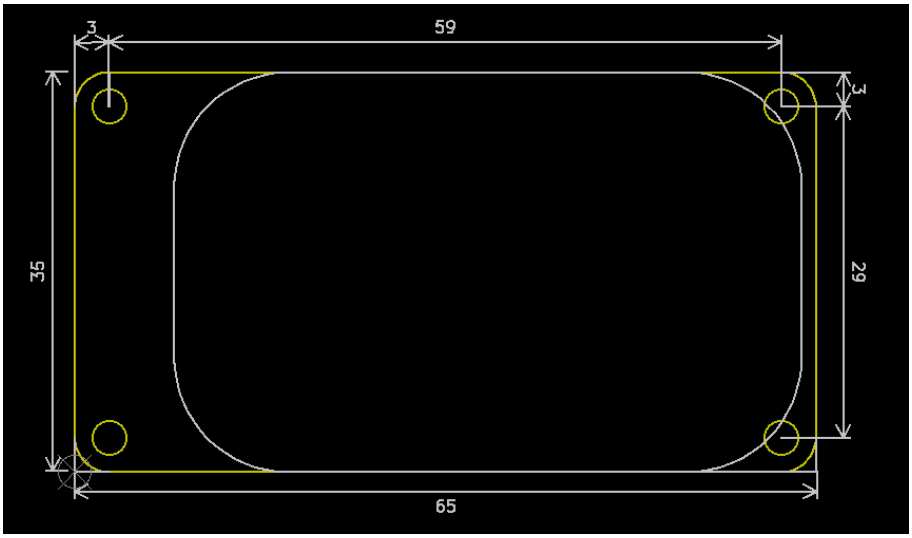


Figure 5.6: PocketBeagle and DTUSat-3 OBC board dimensions (in mm).

Moreover, the number of layers was also increased from the four layers of the PocketBeagle board to six layers. The reason for this increase is that more traces needed to be drawn since more components were added. As explained in Section 4.3, traces should be as short as possible, trying to avoid loops that could induce electromagnetic currents hence interfering with the signals. For this reason, two more layers were added. Furthermore, except for the layer called *VDD* which is a power layer, the rest are all ground layers in order to reduce the loop area as explained in Section 4.3. Table 5.1 shows the implemented properties of the copper layers, which include the thermal relief parameters.

Margin	0.1524 mm
Minimum copper thickness	0.1524 mm
Thermal clearance	0.1524 mm
Thermal spoke width	0.3048 mm

Table 5.1: Parameter of the PCB copper layers.

Also, it needs to be noted that all vias are through hole vias in order to reduce the manufacturing cost. Table 5.2 shows the default via and trace parameters used in the design. However, some larger vias and traces, such a as some GND vias and VDD traces, were used in order to reduce impedance.

Furthermore, the resulting layout as well as the different layers can be found in Ap-

Via Diameter	0.64 mm
Via Drill	0.4 mm
Trace width	0.1524 mm
Margin	0.1 mm

Table 5.2: Via and trace design set up.

pendix G. However, in this section, only the components that were modified or added to the PocketBeagle board are going to be explained in terms of layout. The rest of the layout was left as in the original PocketBeagle board.

- USB connector

When the board was increased in length, the USB remained in the middle of the board, therefore it needed to be moved to the edge of the board as it can be seen in Figure 5.7. The communication pins are connected to the transient voltage suppressor through thin traces while the GND pads are directly connected to the bottom plane which corresponds to ground.

It needs to be noted that the SSCB stack connector is placed just below the USB. For this reason, several through hole vias that were found in the PocketBeagle configuration had to be removed, in order not to interfere with the SSCB stack footprint. However, this was not an issue because these vias fulfilled just mechanical purposes, their function was to give mechanical stability to the USB and prevent the holder from falling out when inserting the cable.

- microSD card connector

The microSD card holder is placed on the opposite edge of the USB, in such way that the microSD card is introduced from the outside of the board, as it is shown in Figure 5.8. The communication pins are connected through vias to resistors R10 and R11, which at the same time are connected to the Octavo SiP. Moreover, pads M and the GND pins are directly connected to the bottom plane which corresponds to ground, and they have several vias to facilitate current flow.

Furthermore, the card detector pin, pin 9, works as follows: when the card is inserted, pins 9 and 6 are short-circuited, which puts a low level on pin 9. Therefore, when pin 9 is low, it means that the microSD card card has been inserted.

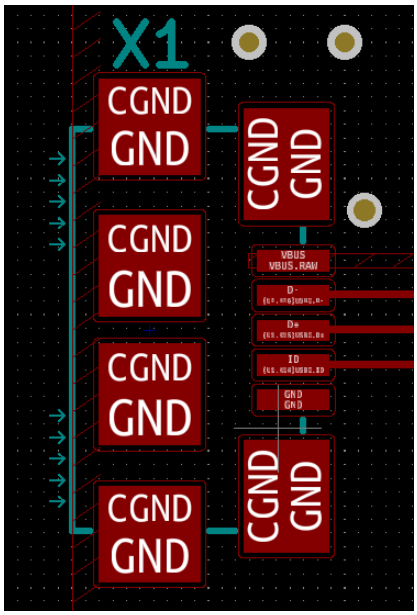


Figure 5.7: USB connector layout.

- SSCB stack connector

The SSCB stack connector is placed on the bottom layer. Figure 5.9 shows the layout of the stack connector. Pins 1, 3, 5, 7 and 9, in the bottom left, are connected to a plane of 3.3 V. This plane has several vias in order to facilitate current flow, which at the same time go to the step-up converter input plane and the CAN transceiver using thick traces to reduce impedance. Moreover, pads M and the GND pins are directly connected to the bottom plane which corresponds to ground. The rest of the pins are communication signals, therefore thin traces connected these pins with the Octavo SiP.

- CAN transceiver

The CAN transceiver is also placed on the bottom layer, close to the stack connector. Moreover, the external components were placed as close as possible to the IC as shown in Figure 5.10.

- Step-up Bus Converter

For this component, the footprint was designed from scratch using the Footprint Editor tool of KiCad. The designed footprint as well as the dimensions are shown in Appendix I.

Then, Figure 5.11 shows a recommendation of how the layout of the step-up converter

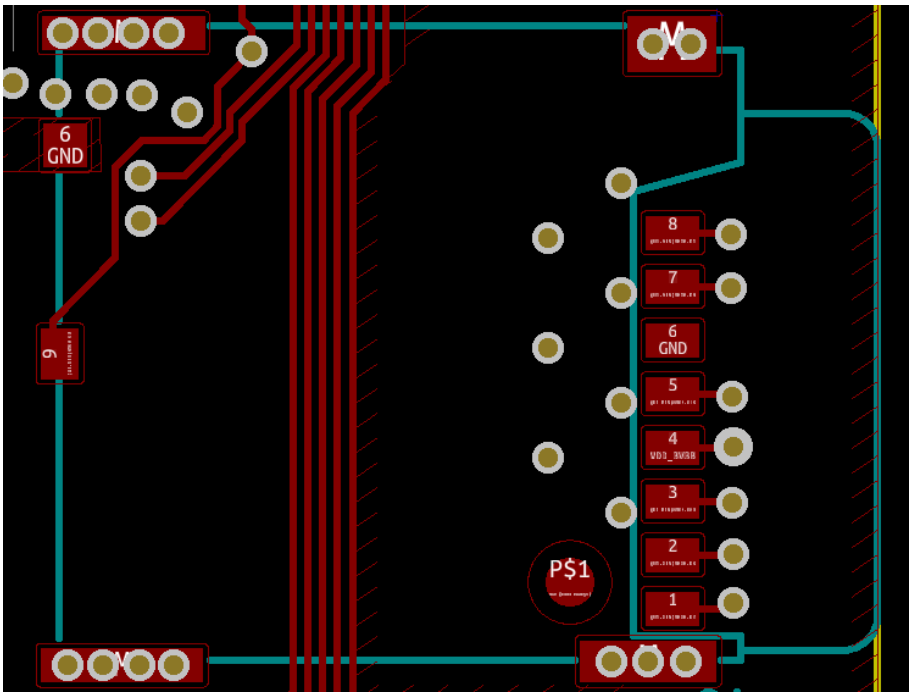


Figure 5.8: microSD card connector layout.

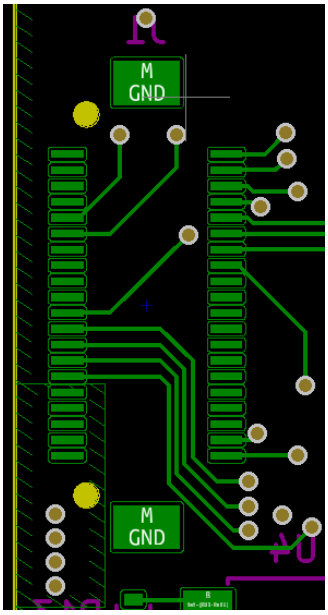


Figure 5.9: SSCB stack connector layout.

should be done. In order to reduce the circuit impedance, all the external components should be placed as close to the IC as possible and thick and short connecting traces should be used, since high impedance induces noise in the output current. Moreover, the input capacitor needs to be placed close to pins 1 and 2 to stabilize the input voltage level.

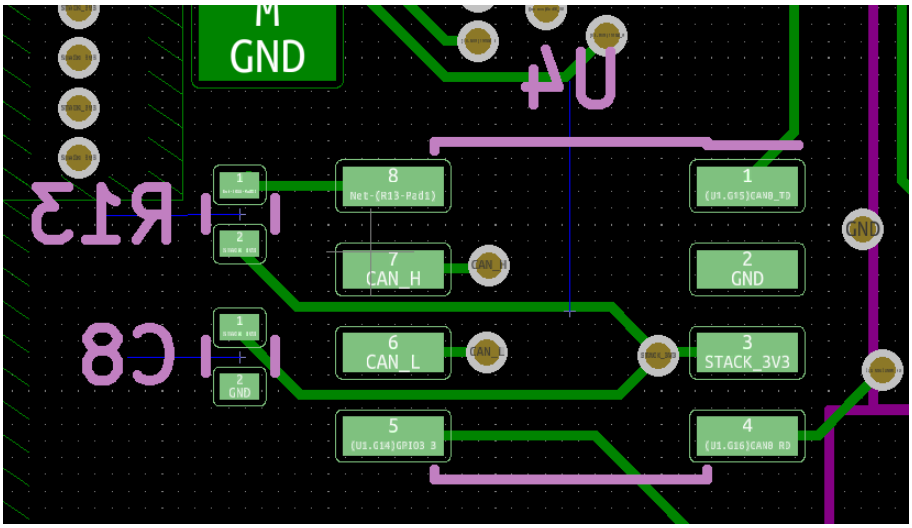


Figure 5.10: CAN transceiver layout.

Also, it is important to ensure that the GND traces are as thick as possible, as variations in ground potential caused by high ground currents at the time of switching may result in instability of the IC.

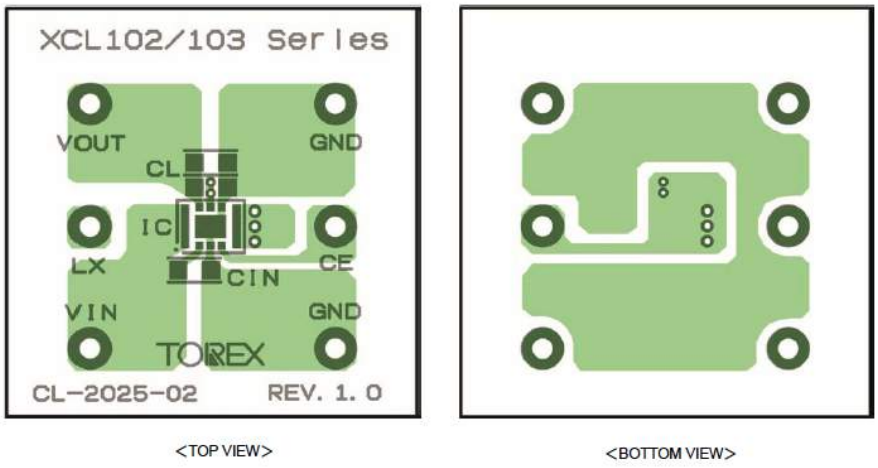


Figure 5.11: Recommendation for the Step-up converter XCL103D layout (Torex, 2019).

This way, the implemented layout for the step-up converter, which is placed on the top layer, is shown in Figure 5.12. Here, capacitors C9 and C10 and resistor R14 are placed as close as possible to the pins in the IC to which they are connected. Furthermore, there are three planes in the top view (in striped red): the upper one corresponds to 5 V, the bottom one corresponds to 3.3 V and the one in the right is connected to pin 8. There is also one plane in the bottom view (in striped green) that is connected to pins 5 and 8. All

these planes have several vias in order to facilitate current flow. The rest corresponds to a ground plane.

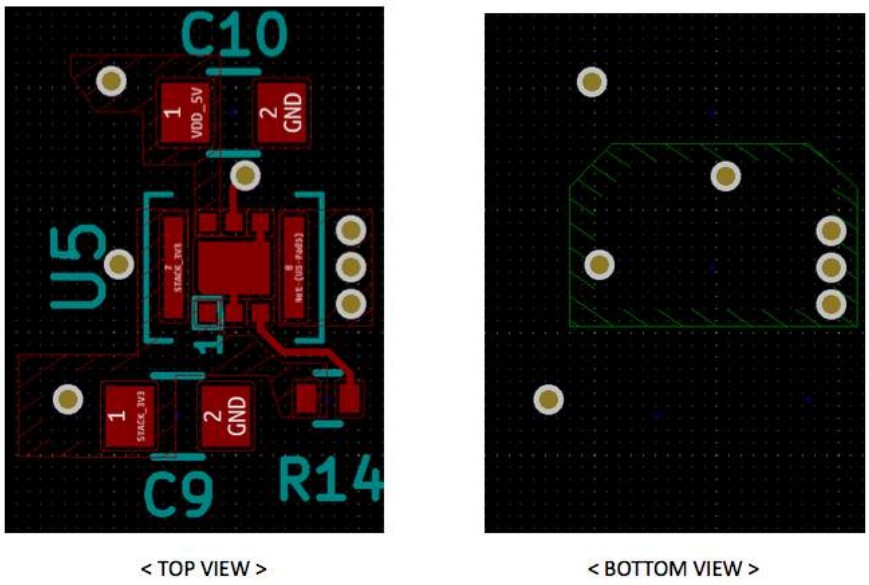


Figure 5.12: Step-up converter layout.

5.2.3 Result

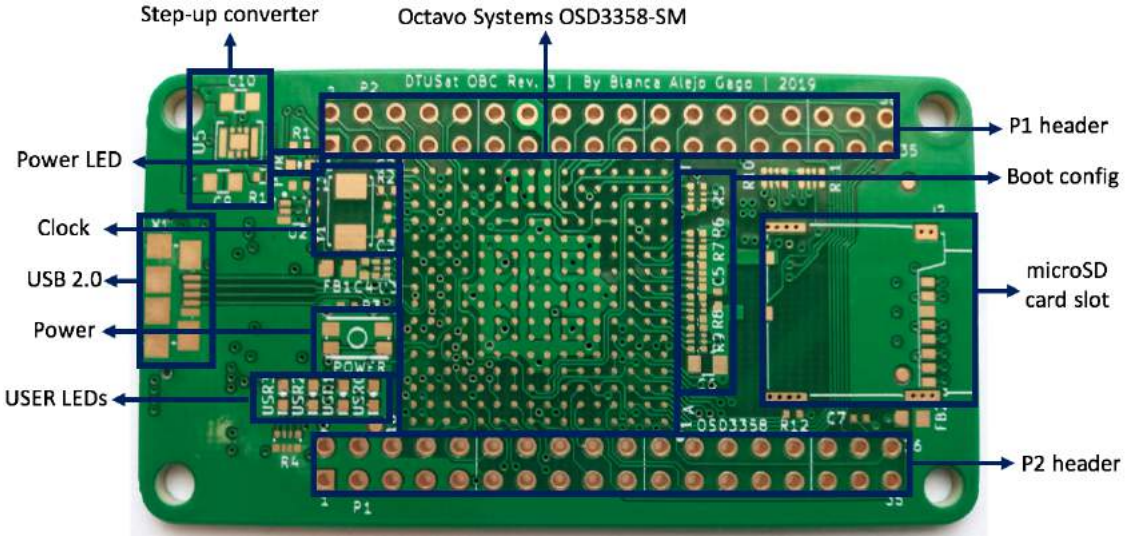
Finally, the manufactured PCB before being soldered in shown in Figure 5.13 and has a dimension of 65 mm x 35 mm x 1.6 mm.

5.3 Soldering

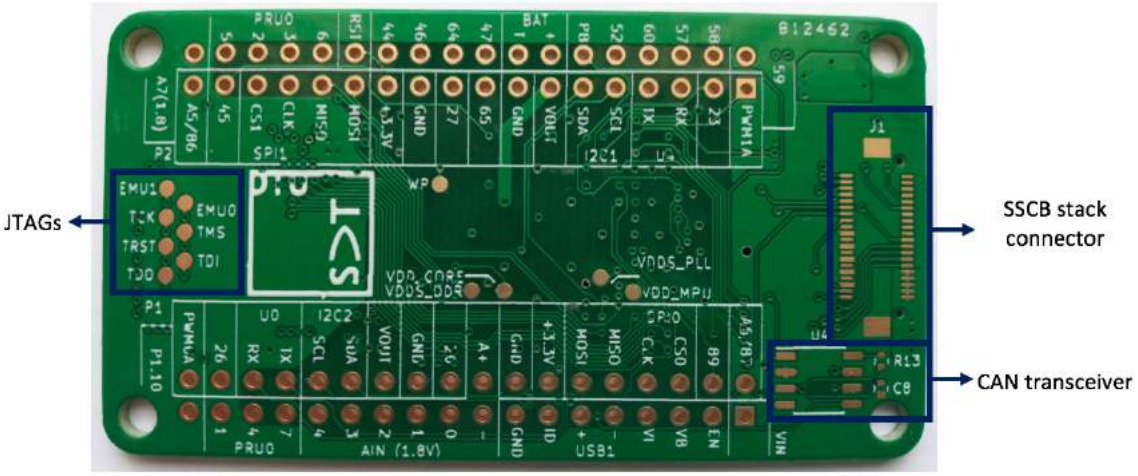
In this section, the soldering process that was carried out after the board was manufactured and delivered is described. It needs to be noted that the soldering process consisted of two phases: a reflow soldering stage and a hand soldering stage. Also, it is important to mention that all the components in the OBC are surface mounted.

5.3.1 Reflow soldering

The first step of the reflow soldering process is to cover the pads in the PCB with solder paste. The solder paste that was used is made of 63% tin (Sn) and 37% lead (Pb), which



(a) Top view.



(b) Bottom view.

Figure 5.13: Manufactured PCB.

is a eutectic alloy with a melting point of 183°C. The reasons for not using a lead-free solder paste, even though lead is toxic, are explained in Section 4.4.1.

For this first step, the PCB was laid down on a table and the stencil was placed on top, making sure it was perfectly aligned with the pads in the PCB, as it can be seen in Figure 5.14. Everything was secured with tape so that it did not move during the process.

Next, the solder paste was rubbed into the wholes of the stencil with a spatula, making enough pressure so that all the pads were completely filled with paste. If a pad is not fully

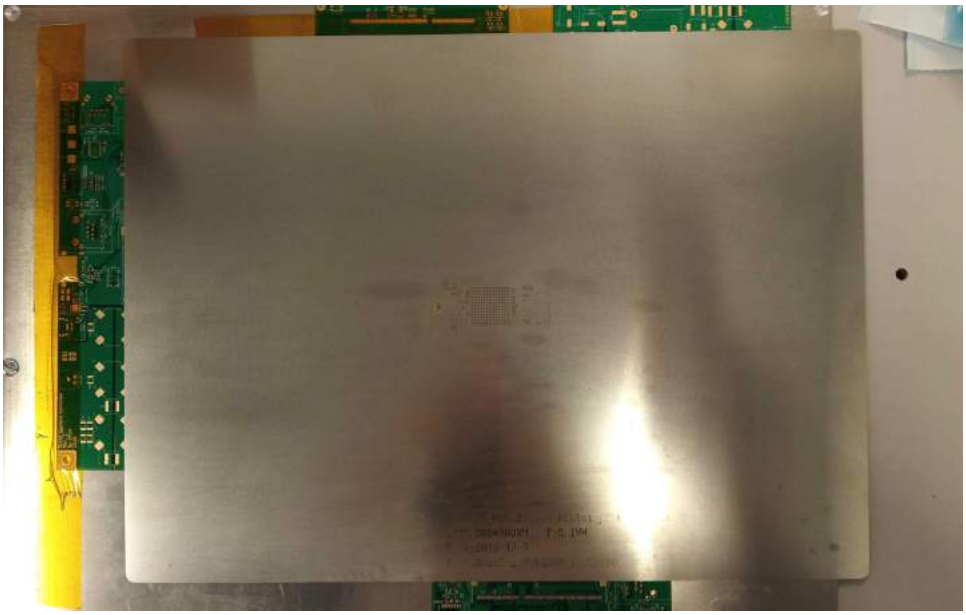


Figure 5.14: Stencil

wet by the solder paste, the solder connection afterwards is not reliable. Particularly important are the pads of the BGA footprint, since all the balls need to be correctly soldered. After that, the stencil was removed, making sure that none of the solder paste stayed attached to the stencil and, therefore, removed from the pads in the PCB.

The next step is to put the components onto their corresponding footprints in the PCB. The first component to be placed was the BGA, followed by the smaller components, i.e. resistors, capacitors and LEDs, since they are harder to settle. Finally, the rest of the largest components were placed. Especial attention needs to be given to polarized components, such as the LEDs, as well as components with several pins, since they need to be put in a certain orientation. For the smallest components a microscope may be of great help. The results can be seen in Figure 5.15.

Once all the components are placed on top of their footprints, the PCB is taken into the oven, where the solder paste melts and solders the components to the pads in the PCB. The oven is a reflow oven that, on the first stage, pre-heats the board up to 160°C (just below the solder paste melting point) during 200 seconds, and then, on the second stage, gradually increases the temperature up to more than 200°C during 50 seconds. The different stages of the reflow soldering process are explained in Section 4.4.

Furthermore, it should be noted that this type of soldering can only be done for components in the front of the board. For components in the back of the board, the

Figure 5.15: Components placed onto their footprints with the solder paste.

soldering needs to be done by hand and using the microscope.

5.3.2 Hand soldering

The components on the back of the board, i.e. the stack connector and the circuit of the CAN transceiver, were soldered by hand. This type of soldering was done with a very thing tin thread and a soldering iron with a very narrow tip.

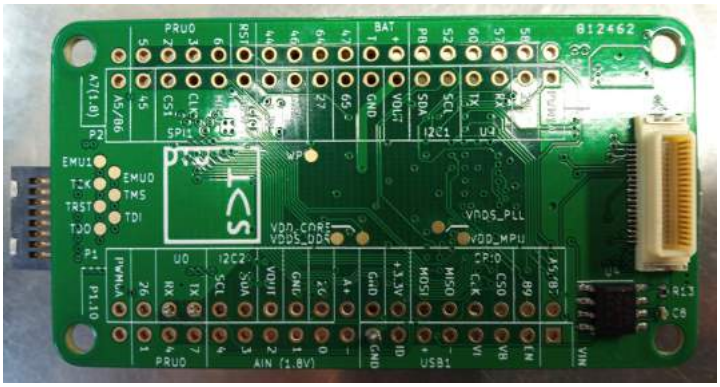
Furthermore, hand soldering was also used for the components that fell out of their corresponding pads during reflow (tombstoning) as well as for the pins where extra solder paste was needed to ensure mechanical stability and conduction.

5.3.3 Solder joint inspection

The last step is to inspect the PCB with the help of a microscope to check that all the components are soldered correctly, that they are all aligned with their footprints and that there is no excess nor defect of solder paste. The finished board can be seen in Figure 5.16. The reason why the microSd card holder is not soldered to match the footprint on the board is explained in Section 5.5 and it is due to issues with the design.

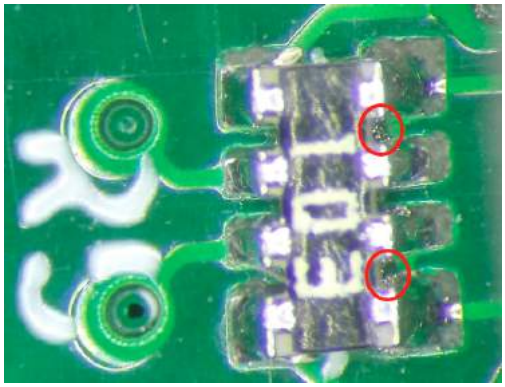
Especial attention should be given to solder balls between the pins of the components which could lead to short-circuits, as explained in Section 4.4.4. Some of these solder balls can be seen in Figure 5.17. In order to clean them, the PCB was soak into Isopropilalcohol for about 15 minutes. This way, the excess soldering is detached and it can be removed afterwards with a brush.

(a) Front.

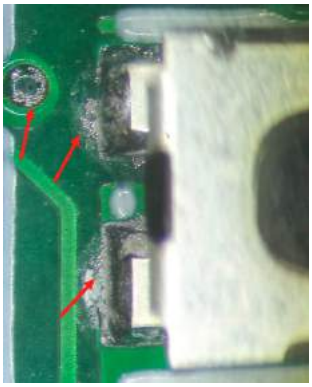


(b) Back.

Figure 5.16: PCB of the OBC for DTUSat-3.



(a) Pins of R5.



(b) Pins of the power button.

Figure 5.17: Solder balls.

Also, it is particularly important to inspect the soldering of the balls in the BGA. As it can be seen in Figure 5.18, the peripheral solder joints seem to be correctly soldered,

there is no soldering between the balls that could lead to a short-circuit and all the balls look uniform in size and shape. However, just a visual inspection is a limited procedure, since the solder joints in the center cannot be reached. For this reason, in Section 5.4 a more accurate method for assessing the quality of the soldering of the BGA is carried out.

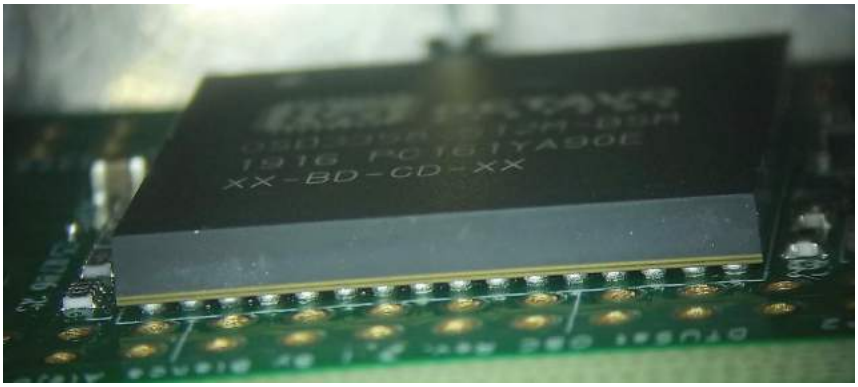
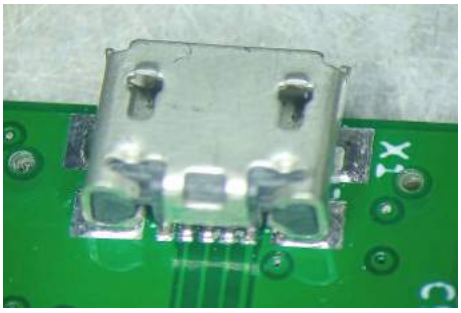
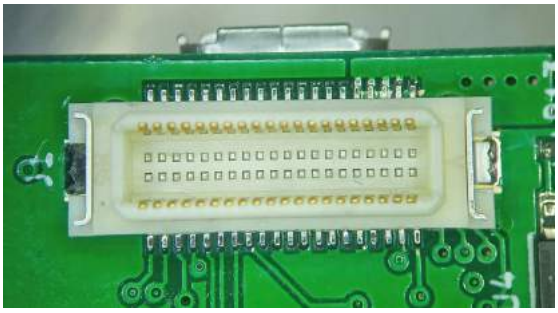


Figure 5.18: BGA.

Furthermore, it is also important to check that the USB and the stack connector are soldered correctly since they are the ones providing power and communication to the entire board. Figure 5.19 shows that they are both correctly soldered, since there are no solder balls between the pins.



(a) USB.



(b) Stack connector.

Figure 5.19: USB and stack connector.

Finally, no dewetting or nonwetting of the pads nor cold solder joints are appreciated in the images. Also no leaching, solder beading, wicking nor skewing can be seen in the PCB. Therefore, after this first visual inspection, it can be concluded that the soldering process was performed correctly.

5.4 X-Ray inspection of BGA

In this section, the X-ray test that was carried out to ensure that the soldering of the BGA was performed correctly is explained. The X-ray imaging process as well as the most common defects found on BGA solder joints are described in Section 4.5 and are the base for the study of the obtained images of this X-ray test.

For taking the X-ray images, the PCB was placed above and perpendicular to the X-ray source, i.e. the X-rays were coming from below the board. Therefore, it is important to remember that this does not allow cross-sectional imaging, which means that the areas above and below very dense materials are masked. Furthermore, the pads in the PCB do not have a teardrop design, which makes it difficult to detect some of the possible defects.

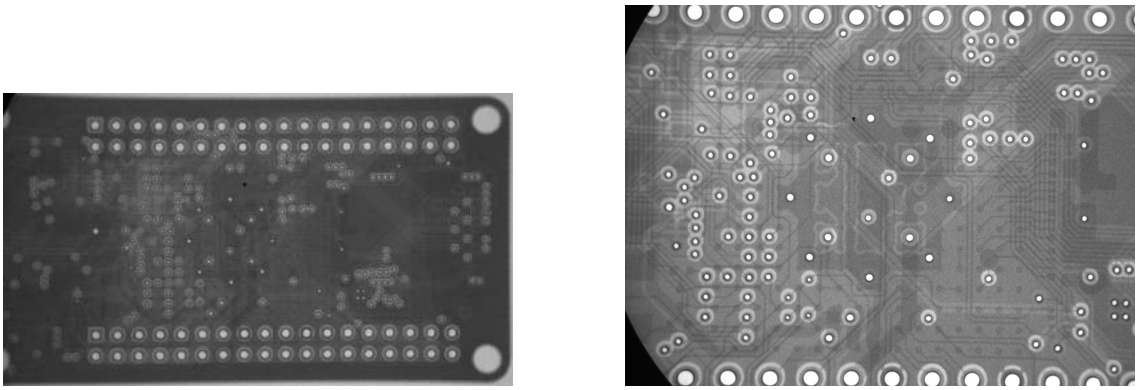
The process for inspecting the BGA using X-ray imaging was performed in three steps, obtaining three different images: the bare PCB board, the Octavo Sip before being soldered and the soldered board with all the components and the BGA. Having X-ray images of the PCB and BGA before and after being soldered allows to determine what belongs to the BGA or the PCB and what is solder paste, therefore facilitating the identification of defects.

Furthermore, the X-ray machine that was used for taking the images had the FDD (focus detector distance) fixed and just the FOD (focus object distance) could be adjusted to obtain the different magnifications, as explained in Section 4.5. Finally, the resolution of the images go from a pixel size of 0.046695 mm, the highest, to a pixel size of 0.007184 mm, the lowest. The pixel size was calculated as the size of the object in the image divided by the number of pixels in the image.

The study of the resulting X-ray images is explained next.

5.4.1 Bare PCB board

First of all, an X-ray image of the bare PCB board was taken to identify the different components in it. As it can be seen in Figure 5.20, the PCB has some through-hole vias as well as traces in different layers crossing the BGA footprint. This will interfere with the BGA components in the X-ray image when the board is soldered.

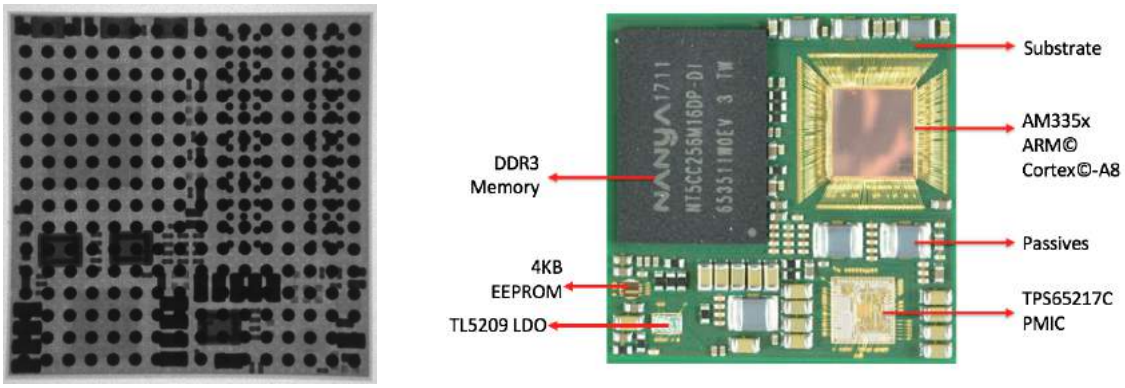


(a) Printed Circuit Board (b) Zoom to the BGA footprint.

Figure 5.20: X-ray image of the PCB before soldering.

5.4.2 Octavo SiP BGA

Then, an X-ray image of the Octavo SiP before being soldered was taken to identify the circuity inside the BGA (Figure 5.21a). Comparing Figure 5.21a, the X-ray image, and Figure 5.21b, which shows the components inside the Octavo SiP, one can see that Figure 5.21a is actually a mirror image of 5.21b. One can identify the passives components above the ARM and on each side of the PMIC as well as the ARM itself and the DDR3 memory. The reason for being a mirror image is that the board was pace above the X-ray source.



(a) X-ray image. (b) Components inside.

Figure 5.21: Octavo OSD335x-SM SiP.

5.4.3 Soldered PCB with BGA

Finally, an X-ray image of the soldered PCB with the BGA was taken, as it can be seen in Figure 5.22. It is important to remember that when obtaining the image, the X-rays were coming from below. For this reason, Figure 5.22 shows the SD card holder is in the top-right, not bottom-right, and the CAN transceiver in in the top-left, not bottom-left. After soldering, the resulting X-ray image should be a superposition of Figure 5.20b and Figure 5.21a.

Furthermore, comparing Figure 5.23a, which corresponds to the BGA after been soldered to the PCB, and Figure 5.23b, which corresponds to the BGA before been soldered to the PCB, one can determine if the soldering was done correctly or not.

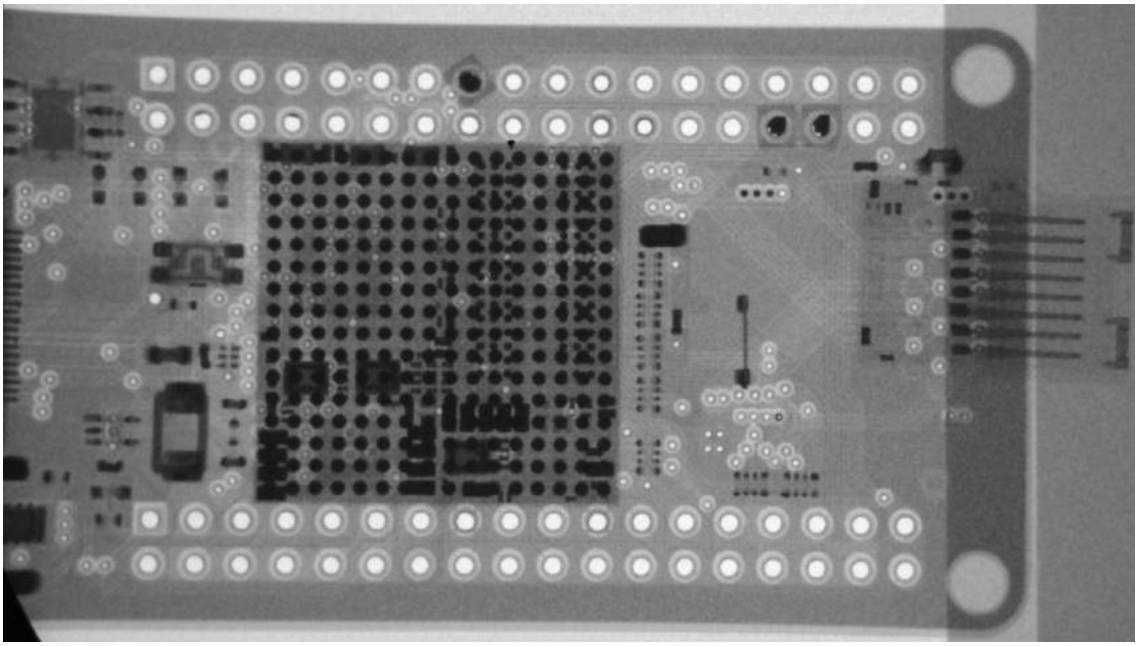
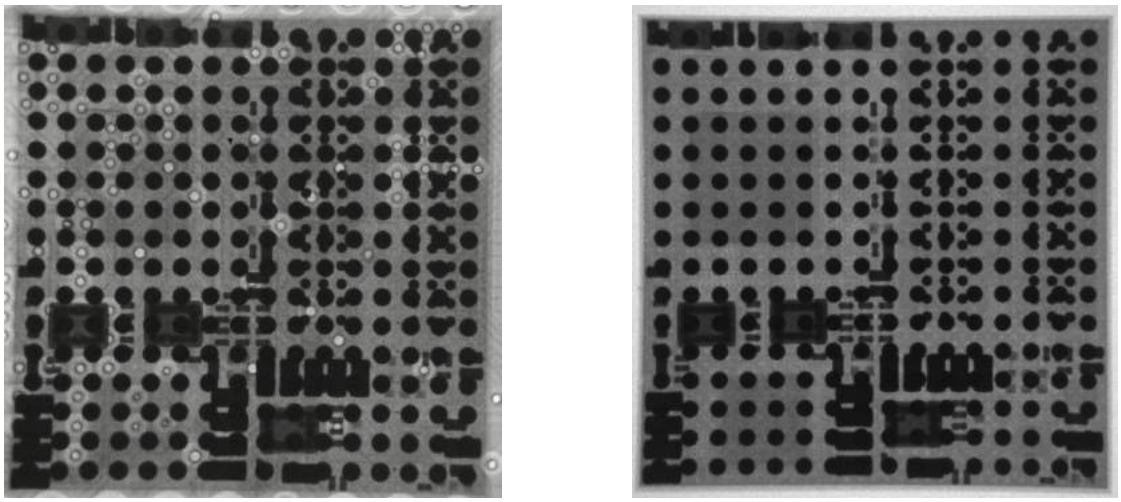


Figure 5.22: X-ray image of the PCB after soldering.

Analyzing both images in Figure 5.23, the first thing that appears correct is the uniformity of the solder balls. All the solder balls are uniformly circular and equal in area, which suggests that the reflow soldering process was completely achieved. Furthermore, no doming or dishing of the BGA package nor cold solder joints are appreciated in the images. Finally, no misalignment, missing balls, bridges nor solder voids can be seen in the images. This way, it can be concluded that the soldering of the BGA was done properly and the solder joints are reliable.



(a) Soldered BGA. (b) Non-soldered BGA.

Figure 5.23: Comparison between soldered and non-soldered BGA.

5.5 Preliminary functional test

In this section, the preliminary functional test that was carried out to ensure that the soldering of the board was done correctly and that all components were functioning as intended is described.

It needs to be noted that the microSD card on the board was configured to have the Linux image. Furthermore, after booting, the LEDs in the board should blink as follows: PWR lights up when the board is powered, USR0 blinks with the heartbeat frequency of the Linux kernel, USR1 lights up just when the microSD card is being accessed, USR2 lights up when there is activity in the board and USR3 is in idle, so it is not suppose to blink unless it is specified otherwise.

For this preliminary functional test, the board was powered through the USB, connected to the computer. When the board was powered up for the first time, it did not produced the expected lighting in the LEDs, therefore several evaluations and verification were carried out in order to find and solve the potential issues.

All the steps that were followed to ensure the correct functioning of the board are explained next.

- External power

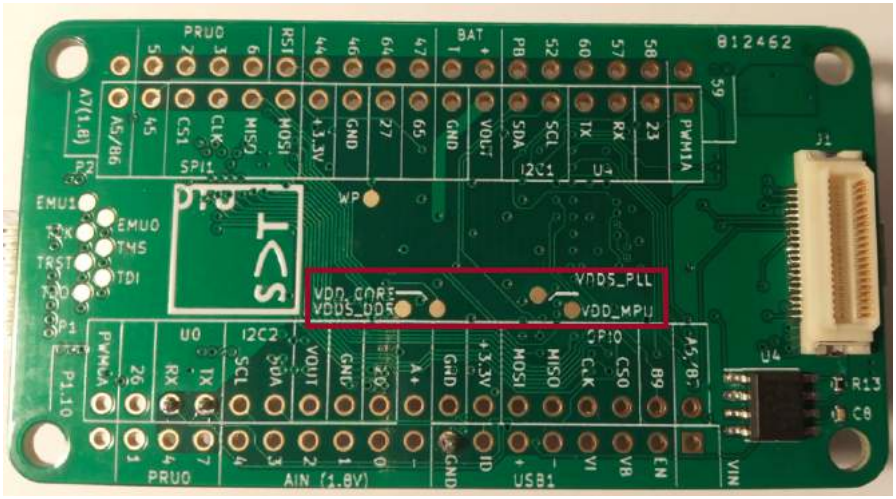


Figure 5.24: Test points in the board.

First of all, it was checked that there was indeed power on the board, since the power LED did not light up. For this, the USB was inspected to verify that there were no short-circuits between its connections using a multimeter. This way, it was confirmed that the USB was providing 5V to the board.

- Test points

The next step was to check the test points available on the back of the board. These test points (Figure 5.24), that are are accessible externally just for monitoring purposes, correspond to internal power supplies inside the Power Management IC, as explained in Section 4.2.2. This way, it was verified using a multimeter that the voltages on the test points were as expected. Therefore, it was assumed that the Octavo SiP Power Management IC was working properly.

- LEDs

Since it was proven that there was indeed power in the board and that the Octavo SiP Power Management IC was working properly, but the power LED still did not light up, all the LEDs were inspected. This way, the power LED was found to be connected in the wrong orientation and it was corrected by hand soldering. After that, when the board was powered up, the power LED lighted up, which again confirmed that the board was powered correctly. Moreover, the user LEDs were verified to be soldered correctly in the first place so no hand soldering was needed.

- Power button

Then, the power button was tested, to verify that the board, as well as the power LED, switched on and off when the power button was pushed. This way, it was proven that the power button was working fine.

- Voltages

Also, other interesting voltage points were tested using the multimeter to check that the voltages of the board were as expected and that there were no short-circuits. For example, pins 5 to 8 in resistor R10, which is connected between the microSD card and the Octavo SiP, were verified to have 3.3 V.

- Crystal oscillator

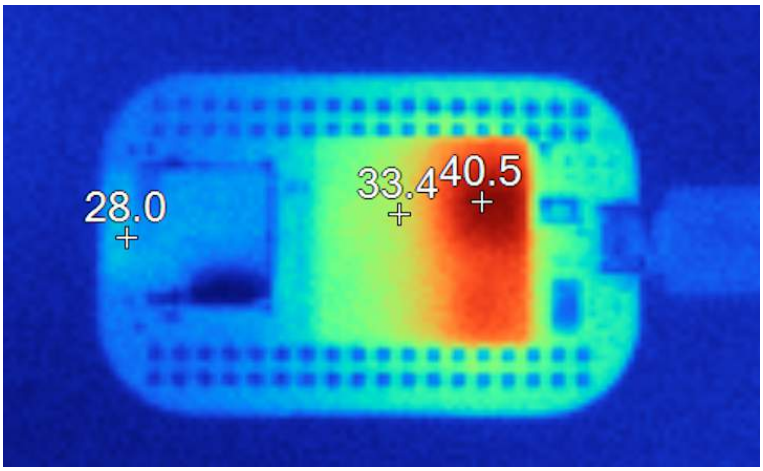
The next step was to check the crystal oscillator, since it should provide a stable clock signal to the ARM processor. This way, using an oscilloscope, it was verified that the output signal from the crystal had a frequency of 24 MHz, as expected.

- microSD card

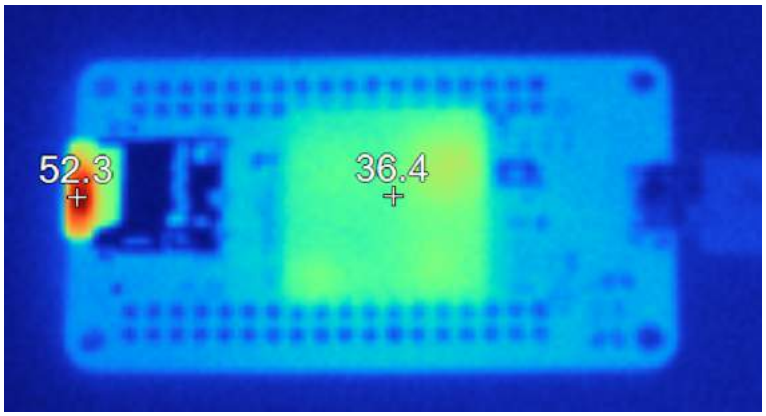
Then, with a thermal camera, the temperature of the board was inspected. This temperature was compared with the temperature of the PocketBeagle board working with the same code. The difference in temperature can be seen in Figure 5.25. From this, it was clear that the microSD card was not working correctly. The problem was that the footprint was design so that the pins in the card holder were inverted with respect to the pins in the microSD card. This way, when the card was introduced from the outside of the board, the pins did not match. In order to solve this, the microSD card holder was soldered by hand so that the pads in the footprint match exactly the pins of the microSD card. This means that the microSD card is now introduced from the inside of the board, as it can be seen in Figure 5.16. Furthermore, the card detect pin, pin 9, and pin 6 were short-circuited to ensure that the microSD card is always accessed.

- Stack connector

The next step was to test the stack connector. For this, the USB was disconnected and an auxiliary board was used, which had a male stack and several pin headers. 3.3V were connected between the power and the ground pins of the auxiliary board, and, as a result, the OBC powered up, which was verified by the lighting up of the power LED. Furthermore,



(a) PocketBeagle board.



(b) DTUSat-3 OBC board.

Figure 5.25: Difference in temperature using the thermal camera.

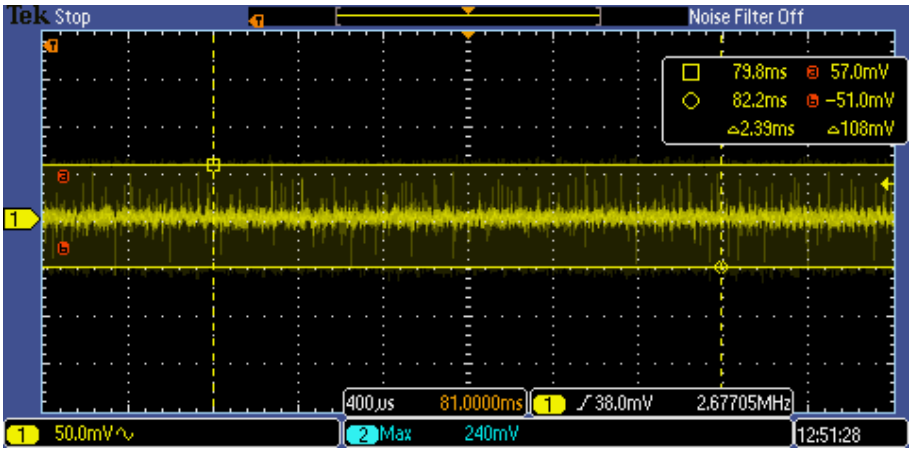
it was verified that the stack was providing with 3.3V to the step-up converter.

- Step-up converter

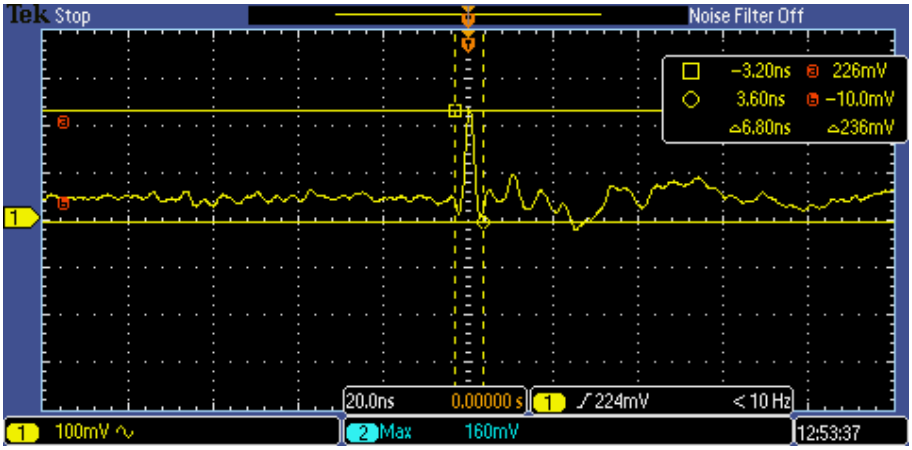
The output signal of the step-up converter was checked using an oscilloscope. First, it was verified that the output voltage was indeed 5 VDC. Moreover, the efficiency of the converter was calculated. It was observed that, when the board was fed with 3.3 V, it draw a current of around 0.534 A, which corresponds to an input power of 1.762 W approximately. Furthermore, it was proven that the Octavo consumes a maximum of 1.5 W, as explained in Section 4.2.1, therefore the step-up converter output power is 1.5 W. With all this, the efficiency of the step-up converter is calculated as the output power divided by the input power, which corresponds to approximately 85%. This result matches

the datasheet specifications, which gives the converter a 86% efficiency (Octavo Systems, 2017).

Finally, the signal was inspected in AC terms to verify that there were no peaks that could affect the Octavo SiP. As it can be seen in Figure 5.26a, most of the the output voltages oscillate between ± 50 mV, however some peaks outside this range can be slightly appreciated. Zooming in in the time scale, one can see an important peak that increases the signal by 226 mV which lasts less than 6.8 ns, as it shown in Figure 5.26b. Nevertheless, the maximum supply voltage accepted by the Octavo SiP is 5.8 V (Octavo Systems, 2017), which means that this peak is not a threat.



(a) AC component (400 us per division).



(b) Peak in the AC component (20 ns per division).

Figure 5.26: Step-up converter output signal.

- Conclusion

After this preliminary functional test, it can be concluded that the board is functioning properly and that it is ready for the next steps of the project.

5.5.1 Booting Linux for the first time

Before booting Linux for the first time there are some considerations that need to be taken into account. As explained in Section 4.6.2, the BeagleBoard Linux image used for the OSD335x identifies designs by a code, a board ID, that is stored within an EEPROM. This board ID is then used within U-Boot to configure the system.

However, all EEPROMs are initially unprogrammed when placed on a board, i.e the board ID is blank. This way, when U-Boot first reads the board ID, it finds a value that does not match any board ID causing the boot process to pause. Therefore, the Linux kernel is never booted. To avoid this issue, there are several steps that should be followed when booting a board for the first time that are explained in Appendix J.

5.5.2 Limitations

Here, some limitations of this preliminary functional test are mentioned.

First of all, it needs to be noted that several components that are found in the board were not tested, which are: the single buffer/driver with open-drain output (U2), the transient voltage suppressor (U3) and both ferrite beds. The reason for this is that this was a preliminary functional test therefore only the functionality of the OBC, i.e. that it can boot, was tested. All the components that were not tested are there for protection purposes not functional, hence, they were not the target of this test.

Furthermore, the CAN transceiver was not tested either because there was no CAN connection available at the moment.

5.6 Step-up converter limitations

Even though the preliminary functional test verified that the XCL103D step-up converter was performing correctly, it was later found that it did not do so in every situation. The reason for this is that the Power Management IC inside the Octavo SiP interferes

with the correct functioning of the step-up converter, hence, in some cases, the converter is able of providing the 5V in its output and, in other cases, it is not. In this section, the problematic with the step-up converter as well as how it was solved for this project, are explained.

5.6.1 Case 1: Power Management IC interferes

Figure 5.27a shows how the Power Management IC inside the Octavo SiP interferes with the correct functioning of the step-up converter. In this Figure, 1 (in yellow) is the converter's output voltage, 2 (in cyan) is the current draw by the board and 3 (in magenta) is one of the Power Management IC's output voltage which corresponds to 3.3V.

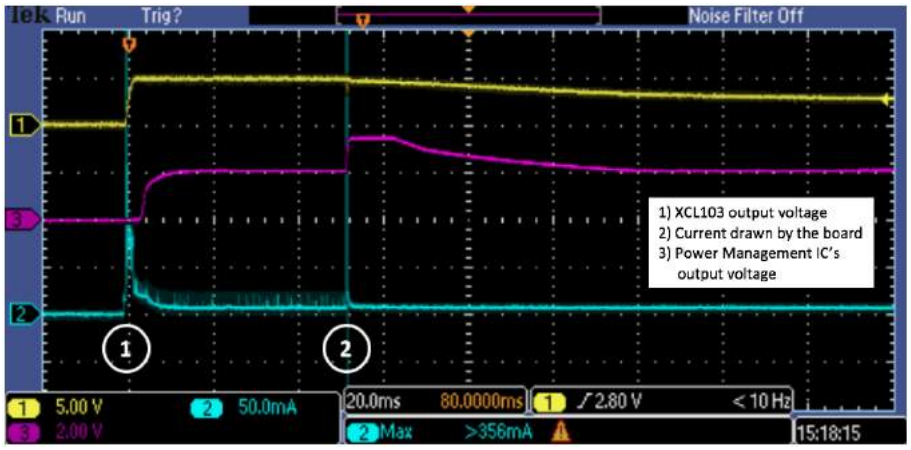
As it can be seen in Figure 5.27a, when the board is powered, the converter functions correctly and it is able of transforming 3.3V into 5V ①. After 50 ms, the Power Management IC starts functioning ②, which is verified by the increased in the Power Management IC's output voltage (signal 3 in Figure 5.27a), and it draws a very high current (peak in signal 2). This peak, which is shown in Figure 5.27b, lasts for about 120 µs and has a value of 1.66 A, which is way above the step-up converters maximum current limit. Therefore, at this moment ②, the maximum current limit function acts, as explained in Section 4.2.3, which makes the step-up converter shut down, leaving the board without power. This is verified by the decreased of the Power Management IC's output voltage. This way, the system cannot boot.

It needs to be noted that this 50 ms delay until the Power Management IC starts working is not random. As it is specified in the Octavo SiP datasheet (Octavo Systems, 2017), the rise time for input rails, defined as time for the input voltage to rise from 100 mV to 4.5 V, is 50 ms.

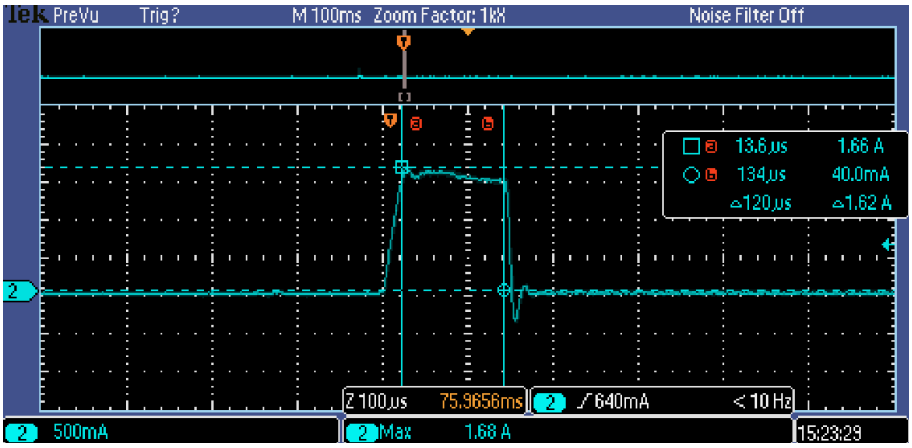
5.6.2 Case 2: Step-up converter functions correctly

As it was mention before, the step-up converter functions correctly in some cases but in other cases it does not. While Figure 5.27a shows a case in which the step-up converter shuts down as a safety feature, Figure 5.28 shows a case in which the step-up converter is able of booting the system.

Similarly to Figure 5.27a, in Figure 5.28 the step-up converter starts functioning properly when the board is powered and, after 50 ms, the Power Management IC starts drawing



(a) Step-up converter and Power Management IC's output voltages and current drawn by the board (20 ms per division).



(b) Peak in the current consumption (100 μs per division).

Figure 5.27: Power Management IC interfering with step-up converter.

a very high current. However, in this case the step-up converter does not shut down and the system boots as usual. The reason for this are the capacitors inside the Octavo SiP, which are charged and provide part of the very high current that the Power Management IC is asking for. This way the step-up converter provides a lower current, below its maximum current limit, and it does not shut down.

In order to charge the capacitors before being able of booting the system, the board needs to be powered on and off several times, leaving little time between cycles so that the capacitors inside the chip do not discharge and, at some point, are able to provide part of the current. If the board is powered on after a long time, then the capacitors inside the chip are completely discharged, hence they can not help the converter.

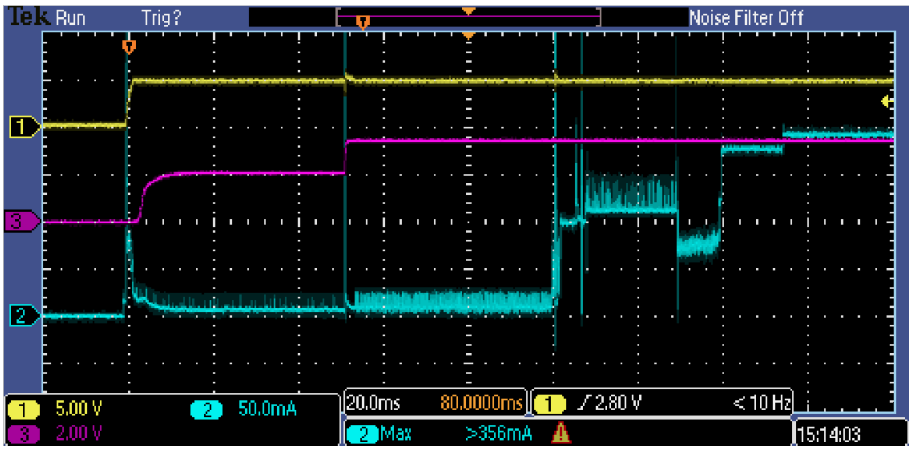


Figure 5.28: Step-up converter normal functioning.

5.6.3 Solution

In Section 8.2, two potential solutions to this issue are given. However, these are solutions to be implemented on the next revision of the board. For this revision and this project, a provisional solution was found in order to be able of testing the step-up converter in terms of radiation. The XCL103D step-up converter is of interested to DTUSat and can be used in other applications thanks to its high efficiency. Therefore it is necessary to know its performance in the space environment.

This way, the connection between the step-up converter and the Octavo SiP was cut and a bank of six 100 Ω resistors in parallel was soldered at its output. This bank of resistors simulates the load of the Octavo SiP and was calculated taking into account that the Octavo SiP consumes a maximum of 1.5 W. Furthermore, several resistors needed to be put in parallel because each resistor can only withstand 0.25 W. The reasoning behind the estimation of the resistors value is provided in Equations 5.2 to 5.5.

$$I_{out} = \frac{P_{out}}{U_{out}} = \frac{1.5W}{5V} = 0.3A \tag{5.2}$$

$$R_{out} = \frac{U_{out}}{I_{out}} = \frac{5V}{0.3A} = 16.67\Omega \tag{5.3}$$

$$\text{Number of resistors in parallel} = \frac{P_{out}}{P_{resistor}} = \frac{1.5W}{0.25W} = 6 \tag{5.4}$$

$$R_{parallel} = R_{out} * \text{Number of resistors in parallel} = 16.67\Omega * 6 = 100\Omega \quad (5.5)$$

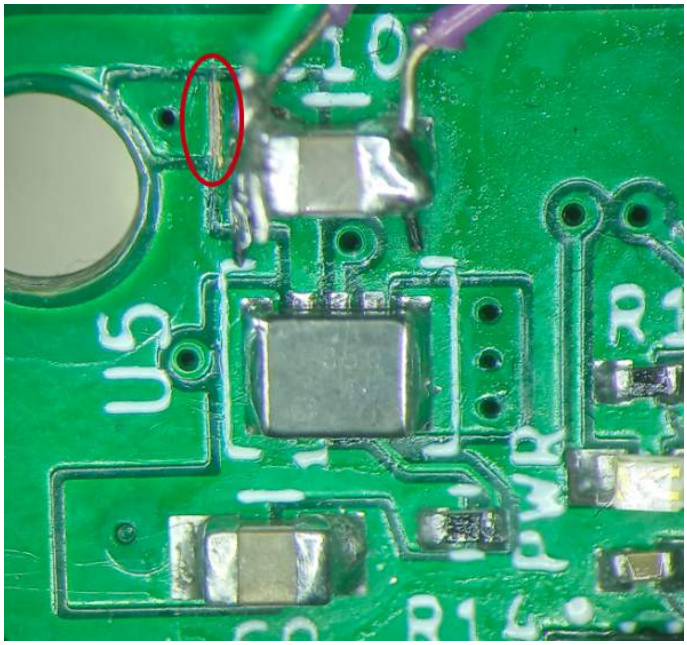


Figure 5.29: Board with the connection between the step-up converter and the Octavo SiP cut.

The board with the connection between the step-up converter and the Octavo SiP broken is shown in Figure 5.29. Finally, it needs to be noted that cutting the connection between the step-up converter and the Octavo SiP means that the board can only be powered through the USB and that the stack connector powers the step-up converter only.

Chapter 6

Test and verification

This chapter describes the tests and verification performed to the OBC for DTUSat-3 and presents the associated results. Firs of all, a FMEA analysis was developed to identify the potential failure modes of the board. Afterwards, an standard function test, that can be implemented for any qualification campaign, was designed that monitors interesting points in the board to understand if a potential failure mode has occurred. Finally, a Total Ionizing Dose test was carried out the 17th of December of 2019 at the Risø High Dose Reference Laboratory.

6.1 Failure mode analysis

In this section, a FMEA is performed for the OBC of DTUSat-3. Although this type of analysis is primarily a reliability task, it also provides information and support to test planning as well as failure detection, isolation and recovery (FDIR) (ECSS, 2009). This constitutes the main reason for applying FMEA to this project, since later a Standard Function Test is going to be developed in Section 6.2 and several tests will be carried out.

In particular for this project, a Design FMEA is carried out and the reason are given next. First of all, a System FMEA is ruled out since, as explained in Section 4.7.1, this type of FMEA focuses on the entire satellite rather than on one particular subsystem. Then, Process FMEA and Functional FMEA are also discarded because the identified failure modes are related to the OBC and not that much to the manufacturing process nor the functions. Furthermore, this project puts emphasis on improving the design and ensuring that the operation is safe and reliable during the entire duration of the mission. For all these reasons, a Design FMEA is carried out in this project. Finally, it should be noted that for this FMEA it is assumed that the product is manufactured according to

the specifications and there are no errors in the process.

Furthermore, as described in Section 4.7.1, the ECSS-Q-ST-30 standard (ECSS, 2009) designates four severity levels depending on the effects and implications of the failures modes: Catastrophic, Critical, Major and Negligible. This way, each failure mode identified is assigned a severity level depending on the implications and consequences of the failure.

6.1.1 Potential failure modes

The different failure modes identified as well as their implications and their severity classification are explained next.

- AM335x Processor

As explained in Section 4.6.1, the first state of the boot process is stored in the ROM memory of the AM335x. This way, if the AM335x Processor fails, the system will not be able of booting, which means that the mission is lost.

However, if the dual architecture is implemented, there would be two processors in a master-slave configuration, which means that if the master processor fails, the slave processor becomes the new master and takes over the satellite control. This will imply a major degradation of the mission since one of the two processors cannot be used anymore. For this reason, this potential failure is classified as **Major**.

- EEPROM

As explained in Section 4.6.2, before booting the Linux kernel, the bootloader looks for a board ID in the EEPROM. If it cannot find this board ID, then U-Boot will not boot the Linux kernel. This way, if the EEPROM fails, the board ID cannot be found, U-Boot does not boot the Linux kernel and the OBC is not able of running its specified functions, which means that the mission is lost.

However, there is a feasible solution for this: reprogram U-boot so that it loads the right device tree by default. This will ensure that the OBC boots even when the EEPROM fails. For this reason, this potential failure is classified as **Minor**.

- DDR3

As explained in Section 4.6.1, the Secondary Program Loader (SPL) loads the U-Boot into Octavo's DDR3 memory and after that, U-Boot loads the Linux kernel into the DDR3. This way, if the DDR3 fails, the system can not boot, which means that the mission is lost.

However, if the dual architecture is implemented, there would be two processors in a master-slave configuration, which means that if the DDR3 memory of the master processor fails, the slave processor becomes the new master and takes over the satellite control. This will imply a major degradation of the mission since one of the two processors cannot be used anymore. For this reason, this potential failure is classified as **Major**.

- Power Management IC

The Power Management IC provides the necessary voltages to the AM335x and the DDR3 memory. Therefore, if the Power Management IC changes its generated voltages, the Octavo SiP may not be able of powering up.

On the one hand, if the voltages generated by the Power Management IC are slightly disturbed, then the board will consume more or less power but the system will still be able of booting and performing its designated functions. However, if the OBC consumes more power, then the batteries may not be able of providing power for the rest of the subsystems, which implies a major mission degradation. For this reason, this potential failure is classified as **Major**.

On the other hand, if the Power Management IC changes the generated voltages significantly, way above/below the component threshold, then the board will not power up and therefore will not able of performing its designated functions, which means that the mission is lost. For this reason, this potential failure is classified as **Critical**.

- microSD card

As explained in Section 4.6.1, before powering the device, the BeagleBoard boot image, which contains the second and third stage bootloaders, the Linux kernel and the file system; resides in the microSD card. Therefore, if the microSD card is not working properly, the bootloader cannot find the BeagleBoard boot image, hence the system cannot boot and the OBC cannot perform the designated function for the satellite, which means that the mission is lost.

However, there is a feasible solution to this potential failure: adding another flash

memory, such an eMMc, to store a second image of the operating system. This way, if the microSD card fails, the bootloader will look into the eMMC for the Linux image and boot from there. This ensures that the OBC boots even when the microSD card fails. For this reason, this potential failure is classified as **Minor**.

- Crystal oscillator

The crystal oscillator provides with a stable clock signal for the processor, so if the crystal changes its frequency, the Octavo SiP may not be able of booting.

On the one hand, if the crystal resonance frequency is slightly disturbed, then the Octavo SiP may still be able of communicating depending on the bit rate of the communication channel. For this reason, this potential failure is classified as **Minor**.

On the other hand, if the crystal resonance frequency changes significantly, then OBC cannot perform its designated functions for the satellite, which means that the mission is lost. For this reason, this potential failure is classified as **Critical**.

- Step-up converter

The step-up converter provides the correct voltage to the Octavo SiP so that it can be powered up through the stack. Therefore, it the step-up converter changes its output voltage, the board may not be able of powering up.

On the one hand, if the output voltage generated by the step-up converter is slightly disturbed, the the board will consume more or less power but the system will still be able of booting and performing its designated functions. However, if the OBC consumes more power, then the batteries may not be able of providing power for the rest of the subsystems, which implies a major mission degradation. For this reason, this potential failure is classified as **Major**.

On the other hand, if the step-up converter changes the output voltage significantly then the board will not power up and therefore the OBC is not able of performing its designated functions, which means that the mission is lost. For this reason, this potential failure is classified as **Critical**.

6.1.2 Severity matrix

It should be noted that no potential failure is classified with a catastrophic severity level. The reason for this is that this mission is unmanned, which means that if the OBC fails to operate, no life would be lost. Moreover, a failure in the OBC subsystem does not result in any other subsystems failing, therefore no risk of failure propagation nor lost of the entire system. This way, the highest severity level in this project is Critical and it will be assigned with the highest severity number, i.e. 4, followed by Major, with a 3, and Minor, with a 2.

These results are summarized in Table 6.1.

Part	Failure mode	Action	Severity level	Severity number
ARM processor	The OBC cannot boot	Implement dual architecture	Major	3
EEPROM	The board ID is not found	Right device tree by default	Minor	2
DDR3	The OBC cannot boot	Implement dual architecture	Major	3
Power Management IC	Voltage slightly disturbed	—	Major	3
	Voltage change significantly	—	Critical	4
SD card	The Linux image is not found	Add an eMMC flash memory	Minor	2
Crystal oscillator	Frequency slightly disturbed	—	Minor	2
	Frequency change significantly	—	Critical	4
Step-up converter	Output voltage slightly disturbed	—	Major	3
	Output voltage change significantly	—	Critical	4

Table 6.1: Severity matrix.

6.1.3 Limitations

The reason for not having developed a FMECA for the OBC of DTUSat-3 is that the criticality could not be calculated. As explained in Section 4.7.2, the criticality of a potential failure corresponds to a combined measure of the severity of a failure mode (FMEA) and its probability of occurrence. In this sense, to obtain a statistically significant result, several tests should be carried out to ensure a reliable probability percentage of the occurrence of the failure mode. However, for DTUSat-3 there is not enough budget to perform that many tests which results in not being able of determining the probability levels for the potential failures.

6.2 Standard Function Test

In this section, a standard function test is develop for the OBC of DTUSat-3. This test is based on the failures modes identified in the FMEA, developed in the previous section. A standard function test is the process design to verify if a potential failure mode has occurred. For this, all the potential failure modes need to be monitored.

This standard function test is divided into two parts: hardware and software. Voltages, currents and power consumption of the board are monitored through hardware while the components inside the Octavo SiP as well as the microSD card are monitored through software. Furthermore, the testing should be performed as similar as possible to the flight conditions (following the "Test as you fly, fly as you test" concept).

Finally, it needs to be reminded that, during testing, the board is powered through the USB while the step-up converter is powered through the stack connector, and that the step-up converter has a bank of resistors soldered to its output simulating the load of the Octavo SiP. This is explained in Section 5.6.

6.2.1 Hardware

Several components in the board are monitored through hardware to determine if any potential failure mode associated to them has occurred. For this, wires were soldered to the interesting points and connected to mutimeters to monitor either voltages, currents or power consumption.

The voltages that are monitored are: the four test points on the back of the board that correspond to the Power Management IC and the output pin of the step-up converter. For this, the board common ground needs to be used. Apart from that, the power consumption of the board and the step-up converter are also monitored. On the one hand, the power consumption of the step-up converter is checked by monitoring the amount of current that the board draws combined with the 3.3 VDC voltage supply. On the other hand, the power consumption of the board is checked using a powermeter connected between the board and the computer with an USB cable.

It needs to be mentioned that the purpose of monitoring the power consumption of the step-up converter is to be able of verifying if its efficiency is increased or reduced during the tests. The efficiency is calculated as the output power divided by the input power and at the same time the output power is calculated as a relationship between the value of the bank of resistors that simulate the Octavo SiP load and the output voltage.

Figure 6.1 shows a diagram specifying which points are interesting to monitor in the hardware part of the standard function test, to be able of determining how many multimeters are required. Furthermore, Table 6.2 shows the expected values for the different monitored points during normal functioning, and, therefore, this table is a based from which to know if a failure mode has occurred or not.

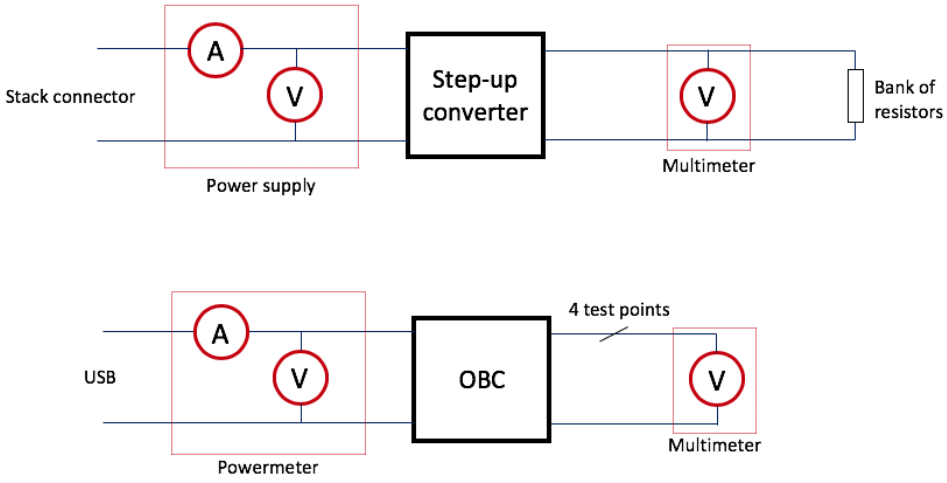


Figure 6.1: Diagram for the Standard Function Test.

Finally, it needs to be noted that there are several components on the board that are not monitored in this standard function test and the reasons are explained in Section 6.2.3.

Point	Value in normal functioning
Test point VDDS_DRR	1.5 V
Test point VDD_MPU	1.1 V
Test point VDD_CORE	1.1 V
Test point VDDS_PLL	1.8 V
Step-up converter output	5 V
Stack connector voltage supply	3.3 V
Stack connector current supply	0.6 A
Board power consumption	max 1.5 W

Table 6.2: Expected values for the different monitored points.

6.2.2 Software

In terms of software, a test code was developed by DTU student Florian Agez in (Agez, 2020) that allows to monitor the EEPROM and DDR3 memories, the microSD card and the I2C bus. The outcome of the code is displayed through the UART, so a connection between the RX and TX ports of the board and a computer is needed.

This test code boots the system, performs several checks, waits for 30 seconds and then reboots. The basic principle behind these checks is called stress or exhaustive testing, in which the hardware is put under high levels of stress, which include extreme workloads, tasks and memory usage among others; in order to ensure stability (Ehrlich et al., 1998). In this case, the stressapptest is used which generates a bast and randomized variety of transactions, such as coping, inverting or writing data, with the intent of creating a realistic high load situation in the memory and bus. Then, after a specified period of time, all memories have their data compared with the original fill pattern, therefore verifying if it is correct or not (Paslaru, 2015).

The outcome of this test is as follows:

- If the ARM processor fails, the UART will print nothing, because the system is not even booting.
- If the EEPROM fails, the UART will show that the system started booting during a reboot but suddenly stopped because it cannot find the board ID.
- If the DDR3 fails, the UART will print a warning.

– If the SD card fails, the the UART will show that the system started booting but suddenly stopped because it cannot find the Linux image.

– If the I2C bus fails, the UART will print a warning.

More detail on how the software was developed can be found in (Agez, 2020).

Finally, it is important to mention that, even though the Power Management IC is part of the Octavo SiP, it is monitored through hardware and not through software. The reason for this is that the Power Management IC has several test points available externally and it is more convenient to monitor them through hardware.

6.2.3 Limitations

The limitations that were found when developing this standard function test are explained next.

First, the crystal oscillator cannot be monitored in this standard function test. The reason for this is that the long wires soldered to the pins of the crystal can affect the resonance frequency of the circuit. The wires will change the value of the capacitors in the circuit therefore disturbing the resonance frequency. In addition, the CAN Transceiver is not monitored either because there is no CAN connection available at the moment.

Furthermore, as mentioned before, the test should be developed following the "Test as you fly, fly as you test" concept, and for this reason, nor the LEDs nor the power button are monitored, since they are not used during flight operation.

Finally, the single buffer/driver with open-drain output, the transient voltage suppressor and both ferrite beds are not monitored either because they are all there for protection purposes not functional, hence, they were not the target of this test.

6.3 Total Ionizing Dose Test

Radiation tests are needed to determine the radiation tolerance of the components of the OBC as well as to ensure that they will survive in such a high radiation environment as it is space. In this section, the Total Ionizing Dose test that was carried out for the OBC of DTUSat-3 is explained. The reason for just focusing on TID is explained in Section 4.8.

6.3.1 Radiation chamber

This radiation test was carried out the 17th of December of 2019 at the Risø High Dose Reference Laboratory, which is located at DTU Nutech (Center for Nuclear Technologies). This laboratory has several gamma ray sources, based on the radioactive decay of the Cobalt-60 isotope, which are suited for radiation tests (TID) on electronic circuits and devices (Hansen and Tcherniak, 2017b).

In particular, for this radiation test the Gamma 2 radiation chamber (Figure 6.2) was used. This test chamber has a diameter of 120 mm and a height of 150 mm, which means that it is possible to test an entire Cubesat subsystem PCB horizontally within a diagonal constraint of 120 mm. Furthermore, the chamber has two cable ducts that go into the test chamber, with a dimension of 10 mm in diameter and a length of 450 mm (Figure 6.3a). For testing, once the port is closed, the tube is commanded to move down, at which point the gamma ray exposure starts. The control unit allows programming the exposure time, after which the tube is automatically raised again (Hansen and Tcherniak, 2017b).

Figure 6.2: Gamma 2 Cell at DTU Nutech (Hansen and Tcherniak, 2017b).

6.3.2 Test set up

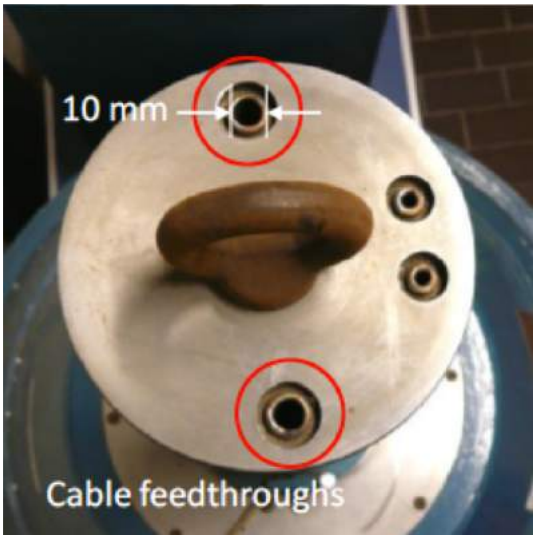
As mentioned before, the radiation chamber has only two ducts of 10 mm diameter each that allow cables in and out of the cell. Since the ducts are rather small, there is a limit on how many cables can go through and therefore how many points can be monitored during test. Also, the cables that are used need to be long enough to be able of connecting the board inside the cell with the measurement devices, this is 2-3 meters. In this section, the set up that was implemented during the test to be able of monitoring all the necessary voltages and currents is explained.

The standard function test explained in Section 6.2 was implemented. This test requires a total of nine wires (four test points, the voltage output of the step-up converter, connections to the RX and TX ports of the UART and two grounds) plus the USB connection to power the board and the power supply to the stack connector.

This way, four cables were introduced in the chamber, two per duct (Figure 6.3b). These cables were:

1. A USB A to microUSB B cable to power the board.
2. A power supply cable: an auxiliary board was used to power the stack, which had a male stack and several pin headers. 3.3V were connected between the power and the ground pins of the auxiliary board.
3. A multicore cable containing 5 cores: it had female connections in one end, that were connected to the four test points and one of the grounds in the board; and bananas on the other end, which were connected to the multimeters.
4. A multicore cable containing 5 cores: it had female connections in one end, that were connected to the RX and TX ports (in the expansion headers), one of the grounds in the board and the step-up converter output; and male connections on the other end, one of which was connected to a multimeter while the RX, TX and ground were connected to a TTL to USB A cable thata t the same time was connected to the computer.

Finally, Figure 6.4 shows how the OBC board and the auxiliary board were placed into the tube.



(a) Cable ducts dimensions (Hansen and Tcherniak, 2017b).

(b) Four cables going into the chamber.

Figure 6.3: Gamma 2 Cell cable ducts.

Figure 6.4: Board set-up inside the tube.

6.3.3 Test development

For this radiation test, four different tests of 12 minutes each with a radiation dose of 20 Gy, which corresponds to 2 krad, per test were carried out. Between tests there was a

break of 4 minutes to allow the board to rest. This way, the board was tested a total of 60 minutes, with 12 minutes of rest. Moreover, during the test, measurements were taken every 30 seconds approximately, which means that a total of 96 measures per monitored point were extracted from the test.

The objective was to simulate the same amount of radiation that the board would withstand in 1.5 years of life, which corresponds to 10 krad, as mentioned in Section 3. However, there was just enough time to carry out four tests, which sums up to 8 krad in total. For this reason, the results and conclusions of the test are going to be extrapolated to 10 krad.

Finally, it needs to be noted that two of the test points, in particular VDD_MPU and VDD_CORE, could not be monitored because the wires broke during the test set up. Furthermore, the power consumption of the board could not be monitored either during the radiation test because there were no cables long enough to connect the board inside the chamber with the powermeter. However, the power consumption was checked before starting and after finishing the entire test.

6.3.4 Test results and conclusions

Finally, in this section the test measurement data is presented in the form of graphs , which were created in MATLAB, and conclusions are drawn from them. The MATLAB code used to performed several calculations based on test results as well as to generate the plots can be seen in Appendix K.

Figure 6.5 and Figure 6.6 show the changing voltage of the Power Management IC VDD_DDR and VDD_PLL respectively. In both graphs there is a clear slight increase in the voltage supply of the Power Managament IC. Comparing these values with Table 6.2 one can conclude that the voltages are in the range of the expected values for these test points. However, this voltage increase suggests an increase in the power consumption of the Octavo SiP and, therefore, the entire board.

Figure 6.7 shows the changing efficiency of the step-up converter. The efficiency was calculated as the output power divided by the input power. The input power was deduced from the voltage and current drawn by the board that were monitored, while the output power was calculated knowing the monitored output voltage of the step-up converter and the value of the bank of resistors. From this graph one can conclude that the efficiency of

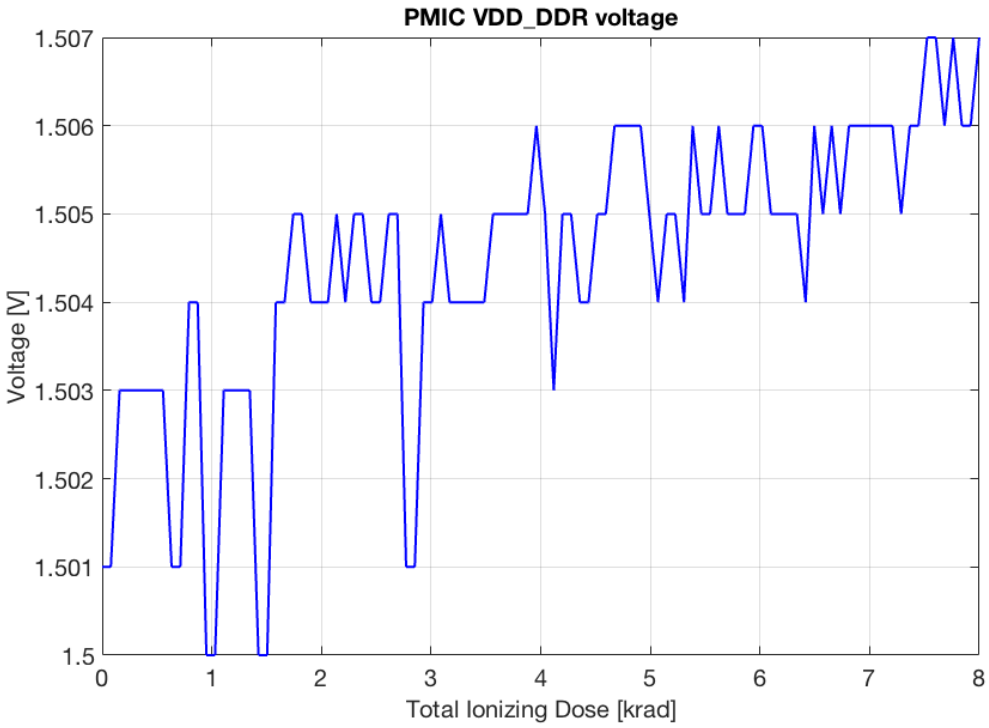


Figure 6.5: Voltage of VDD_DDR test point during radiation test.

the step-up converter slightly decreases with increasing radiation. However, the changes could be due to a low resolution of the measuring devices.

Moreover, the power consumption of the board was verified before and after the TID test. Before starting the tests the board consumed 1.17 W while after finishing the tests the board consumed 1.25 W. This could imply that the board increases power consumption with increasing radiation. However, the results are not very representative due to the small amount of measurements that were taken.

In conclusion, although some interesting phenomena were observed during the TID test, none of the tested ICs showed any significant degradation due to radiation, hence the board passed the test.

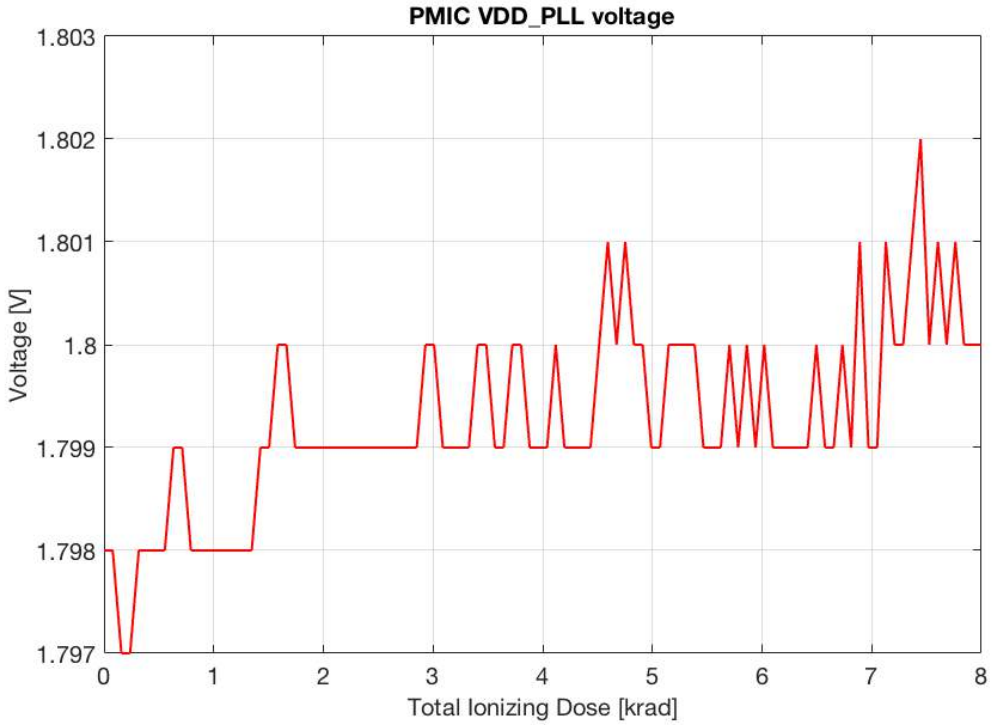


Figure 6.6: Voltage of VDD_PLL test point during radiation test.

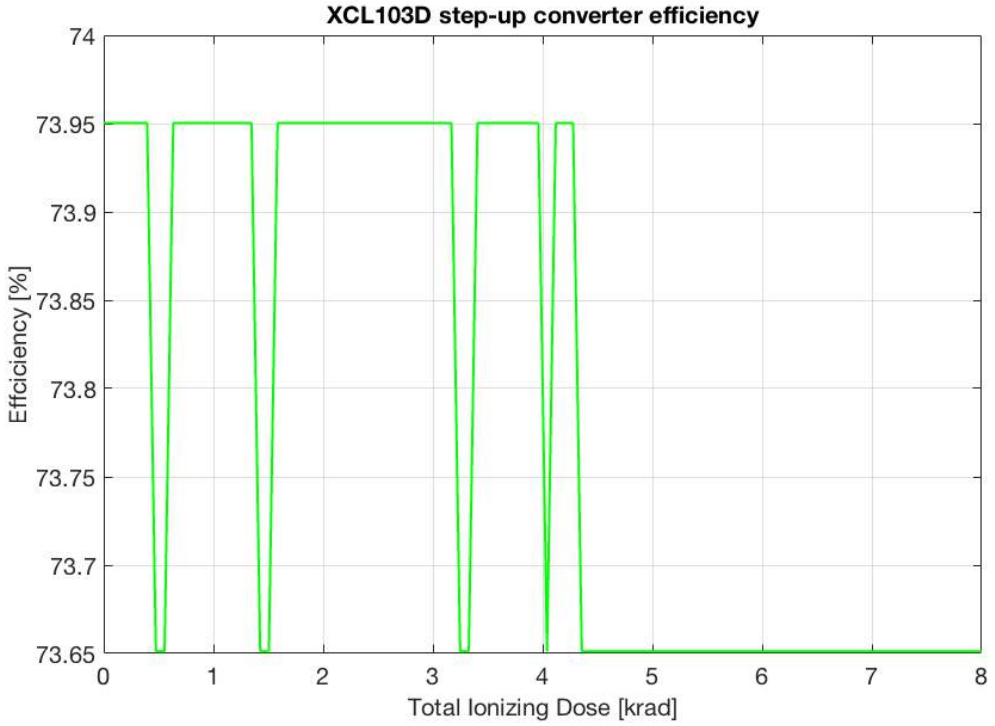


Figure 6.7: Efficiency of the step-up converter during radiation test.

Chapter 7

Conclusion

The objective of this Master Thesis was to design, manufacture and test an On-Board Computer that complied with all the requirements of the DTUSat-3 satellite, that ran in Linux, so that it was easier for students to develop software; and that it was built using COTS components, in order to reduce cost.

First of all, a block diagram of the OBC was developed based on the PocketBeagle. This board includes the Octavo SiP as well as a microSD connector to store the Linux operating system. However, the PocketBeagle alone does not fulfill all the requirements for the DTUSat-3 satellite hence a CAN transceiver, a stack connector and a step-up converter were added to the board.

Then, the PCB for the OBC was designed in KiCad. The circuit schematics and PCB layout were developed using the PocketBeagle board as a base, but adding the required components and modifying the size and shape of the board so that it complies with the mechanical constraints. Once the PCB was manufactured, the components were soldered to it, in a process which consisted on both reflow soldering and hand soldering. Moreover, the BGA solder joints were inspected using X-radiography and a preliminary functional test was carried out that ensured the correct soldering and functioning of all the components in the board. However, it was found that the step-up converter cannot deliver the necessary current during system boot when the capacitors inside the Octavo SiP are discharged. If these capacitors are charged, which is achieved by powering the board several times, the Octavo SiP boots normally and is able of performing the necessary tasks.

The last step consisted of testing and qualifying the board. First, a FMEA analysis identified the potential failures in the OBC as well as their severity and plausible solutions. Then, a Standard Function Test was designed which verifies if a potential failure mode has occurred during any qualification test. Finally, the OBC was subjected to a Total Ionizing Dose test, which revealed that, with increasing radiation, the board slightly increases power

consumption while the efficiency of the step-up-converter is slightly decreased .

In conclusion, the designed OBC meets the specified requirements: it has the desired size and shape to fit into the satellite's structure, it is able of communicating with and powering up through the subsystem carrier board and it endures the radiation dose for the specific orbit and the mission duration. Therefore, if the board is powered cycled several times to resolved the step-up converter problematic, the designed OBC can be used in stratospheric balloon flights. However, the board is not ready yet for space application since there are some improvements and qualifications that need to be carried out first, as explained in Chapter 8.

Chapter 8

Future works

Throughout the design, implementation and testing of the OBC for DTUsat-3 several issues and potential opportunities for optimization were identified. This chapter discusses these issues and opportunities and summarizes tasks for future work.

8.1 PCB design

For the design of the PCB, several components were added to the original PocketBeagle board in order for the board to fulfill DTUSat-3 specifications. However, there are some components in the PocketBeagle, that are not used during flight operation, hence they should be removed in the next revision. These are: the expansion headers, the LEDs, both the USER and the power LEDs, and the power button. Furthermore, throughout the implementation and testing of the OBC, it came clear that several components should be added, such as an eMMC memory, as well as that the dual architecture should be implemented in order to increase redundancy and reliability.

- Remove unused components

Removing the unused components on the board is essential because space is needed to add other important components. The reasons for removing the above-mentioned components are given next.

First of all, the power button should be removed since it is not used during flight operation and can be a source of errors. If necessary, the Electric Power Subsystem could be able of powering the OBC down. Moreover, the LEDs give information about the status of the board and they are helpful for error detection and debugging, but they are completely useless in flight. There are other ways to detect that, for example, the board

has been powered, than using a LED. Finally, even though the expansion headers were used to access the RX and TX ports of the UART as well as the board ground, they are not needed in flight. Once the subsystem carrier board is finished it can be used to communicate with the board using UART through the stack connector.

- Add a flash memory

As mention in Section 6.1, in order to mitigate the potential failure of the microSD card, which would imply the lost of the mision since the system cannot boot, another flash memory, such an eMMc, should be added. This memory will store a second image of the operating system allowing the bootloader to boot the system even if the microSD card fails.

- Implement the dual architecture

As concluded in Section 4.1, the dual architecture is recommend to be implemented in the next revision of the board. With this, DTUSat-3 should have two OBCs in parallel as well as a watchdog timer to control the master-slave configuration. Moreover, the master-slave configuration should only be inverted when the master's functions are completely lost, i.e. the master fails to boot.

8.2 Step-up converter

During the development of this project, it was found that during boot the XCL103D step-up converter shuts down as a safety feature due to over-current. Therefore, two solutions to this issue are proposed in this report so that one of them is implemented in the next revision of the board.

It is undeniable that a boost converter is needed between the stack connector and the Octavo SiP in order to be able of providing the 5 V that the Octavo SiP requires to boot the system. Therefore, the two solutions proposed here involve either changing the DC/DC converter to one that allows a higher current in its output or dealing with the problematic of the XCL103D.

1. Change the step-up converter

It has been verified that the XCL103D is not the optimal step-up converter for the OBC, since it cannot provide enough current during the system boot. Therefore, the first proposed solution is to impalement another boost converter. Three DC/DC boost converters with a current limit above 1.6 A, which is the current that the Octavo SiP asks for during boot, are presented next.

- **Texas Instrument TPS61085A-Q1 step-up DC/DC converter**: it has a current limit of 2.6 A in its output and an efficiency of 86% approximately. However, this boost converter is bigger than the XCL103D, it does not have the inductor built-in and it requires a rectifier diode. Therefore, the circuitry is much more complicated and will take much more space in the board. Moreover, the capacitors, inductor and rectifier diode need to be selected so that the output voltage is 5 V.

- **Texas Instrument TPS61256A step-up converter**: it has a current limit of 2.3 A in its output, a fixed output voltage of 5 V and an efficiency of 93% approximately. Moreover, the inductor is not built-in and needs to be designed. However, the circuitry is not as complicated as for the previous one and the package is smaller than the XCL103D, which means that it may not take that much space in the board.

- **STMicroelectronics STBB1-APUR buck-boost DC-DC converter**: this is a converter that can operate with input voltages higher than, equal to or lower than the output voltage. It has a current limit up to 2.3 A and an efficiency of 90% approximately. However, this boost converter is bigger than the XCL103D and it does not have the inductor built-in. Therefore, it will take much more space in the board. Moreover, the capacitors and the inductor need to be selected so that the output voltage is 5 V.

Based on this preliminary analysis, this report recommends the Texas Instrument TPS61256A step-up converter. However, all of the proposed DC/DC boost converters have different advantages as well as drawbacks, therefore a more exhaustive study should be carried out in order to be able of selecting the optimal device.

2. Power cycle the OBC

The XCL103D has proved to have a high efficiency and survived the radiation test, hence the second proposed solution is to still use the XCL103D step-up converter and power cycle the board, i.e. disconnect and reconnect the power, several times before the system can actually boot.

In order to determine how may times the OBC should be power cycled, the following procedure was followed. The board was left unpowered for a period of time, and afterwards it was powered up, counting how many power cycles the board needed before it could actually boot. Table 8.1 shows the results. As it can be seen, the OBC needs to be powered between 2 to 10 times. Moreover, the longer the board has been without power, the more times it needs to be powered.

Time without power	Power cycles
3 weeks	10
1 day	2
2 hours	2
30 minutes	2
5 minutes	2

Table 8.1: Power cycles as function of how long the board has been without power.

In conclusion, if this solution is to be implemented, the OBC should be power cycled around 15 times, as standard protocol, to ensure that the system actually booted.

8.3 Total Ionizing Dose test

This project suggests that another Total Ionizing Dose test should be carried out in order to have a more precise understanding of the behavior of the components when being radiated. The performed test only reached 8 krad, when the minimum tolerance requirement is 10 krad, therefore a test that reaches at east 10 krad should be carried out. The are also other reasons to suggest another test and they are explained next.

First of all, during the radiation test that was carried out, two of the test points, in particular VDD_MPU and VDD_CORE, and the power consumption of the board could

not be monitored. For this reason, further testing should be carried out, where the power consumption of the board and all the test points can be monitored at the same time as the board is being radiated.

Moreover, it was identify an slight increase in the Power Management IC voltage supply, which suggests an increase in the power consumption of the board. For this reason, it is interesting to develop another Total Ionizing Test in order to determine if this voltage increase keeps going on while more radiation is applied or if it reaches a steady state in which it does not increase more.

Finally, some of the measurement data seem to have noise due to a insufficient resolution of the measuring devices, therefore, further testing should be carried out in order to clarify this.

8.4 System integration

It has been found that one of the main reasons behind most of the CubeSats failures is the lack of standard practices when it comes to system integration testing (Swartwout, 2016). For this reason, a system integration should be carry out, in which it is tested that the OBC is capable of communicating successfully with other systems and relaying the result of the interaction to a receiver, which must be different from the receiver used during normal operation.

In order to be able of developing a system integration test, the Subsystem Carrier Board and the OBC software as well as other subsystems, should be developed so that communication can be established.

8.5 Thermal and vibration tests

A preliminary qualification campaign consisting of a radiation test has been carried out on the developed board. However, in order to guarantee the correct functioning of the OBC in the space environment, another two tests should be performed: a thermal test and a vibration test.

Temperature in space differs significantly from temperature on the Earth's surface.

While orbiting the Earth, the satellite will pass through zones with sunlight and zones that are in shadow. Furthermore, in Sun-synchronous orbits one face of the satellite is directed towards the Sun, therefore heating up, while the opposite face is directed towards deep space, therefore cooling down. This way, there are be huge temperature differences inside the satellite and also with respect to orbital time. For this reason, a thermal test should be conducted in order to guarantee that the OBC can withstand the expected thermal conditions in space.

Moreover, when launching the satellite, the OBC will be subjected to extreme vibration conditions. Therefore, a vibration test should be carry out in order to guarantee that the OBC can withstand these vibrations.

Chapter 9

References

Aalbers, Gerard and Georgi N Gaydadijev (2006). "CDHS Design for a university nanosatellite". In: *Proc. 57th International Astronautical Congress*. Valencia, Spain, pp. 1–12 (cit. on pp. 3, 6, 19, 20).

Agez, Florian (2020). "Testing Pocket Beagle Real Time Performances". Technical University of Denamrk (DTU) (cit. on pp. 108, 109).

Agustin, Javier et al. (2014). "A built-in CMOS Total Ionization Dose smart sensor". In: *IEEE Sensors*. Vol. 2014-Decem. December, pp. 70–73. DOI: 10.1109/ICSENS.2014.6984935 (cit. on p. 67).

Altium (2018). *Preventing Ground Loops in Your PCB Design*. [Accessed: 26th December 2019]. URL: https://resources.altium.com/pcb-design-blog/preventing-ground-loops-in-your-pcb-design (cit. on p. 41).

Apell, Marc C. (2004). "Considerations for Lead-Free Reflow Soldering". In: *Circuits Assembly*, pp. 28–30 (cit. on p. 43).

Aragón, Víctor Miguel et al. (2011). "Researching a Robust Communication Link for Cubesats : OPTOS , a new Approach". In: *The Third International Conference on Advances in Satellite and Space Communications*. c, pp. 45–50. ISBN: 9781612081281 (cit. on p. 5).

Aragón, Víctor Miguel et al. (2012). "OPTOS communications: A high-performance solution". In: *Microwave And Optical Technology Letters* 54.4, pp. 943–946. ISSN: 0895-2477. DOI: 10.1002/mop (cit. on p. 5).

Bangert, Philip (2012). "Attitude Determination System of UWE-3: Development, Test and Veri cation". PhD thesis. University of Wuurzburg, pp. 1–68 (cit. on p. 6).

Baylakoglu, Ilknur (2007). "Reliability concerns of lead-free solder use in aerospace applications". In: *3rd International Conference on Recent Advances in Space Technologies, RAST 2007*, pp. 158–164. ISBN: 1424410576. DOI: 10.1109/RAST.2007.4283969 (cit. on p. 43).

BeagleBoard (2019). *PocketBeagle®*. [Accessed: 7th September 2019]. URL: https://beagleboard.org/pocket (cit. on pp. 12, 25).

Becker, Heidi N., Tom Elliott, and James W. Alexander (2006). "Electron-induced displacement damage effects in CCDs". In: *IEEE Transactions on Nuclear Science* 53.6, pp. 3764–3770. ISSN: 00189499. DOI: 10.1109/TNS.2006.886208 (cit. on p. 67).

Benn, Mathias (2005). "DTUSat-2 System Topology Study". PhD thesis. Danmarks Tekniske Universitet, pp. 1–10. URL: www.campusnet.dtu.dk (cit. on p. 3).

Bouwmeester, J., G. T. Aalbers, and W. J. Ubbels (2008). "Preliminary mission results and project evaluation of the Delfi-C 3 nano-satellite". In: *European Space Agency, (Special Publication) ESA SP*. 660 SP. ISBN: 9789292212247 (cit. on p. 6).

Breukelen, Eddie van et al. (2006). *Delfi-C3: Delft University of Technology's Nanosatellite* (cit. on p. 6).

Brouwer, G F and J Bouwmeester (2009). "From the Delfi-C3 Nano-satellite towards the Delfi-n3Xt Nano-satellite". In: *23rd Annual AIAA/USU Conference on small Satellites*, pp. 1–9 (cit. on p. 6).

Busch, S. et al. (2015). "UWE-3, in-orbit performance and lessons learned of a modular and flexible satellite bus for future pico-satellite formations". In: *Acta Astronautica* 117, pp. 73–89. ISSN: 00945765. DOI: 10.1016/j.actaastro.2015.08.002. URL: http://dx.doi.org/10.1016/j.actaastro.2015.08.002 (cit. on pp. 6, 7, 21).

Busch, Stephan and Klaus Schilling (2013). "Robust and effcient OBDH core module for the flexible picosatellite bus UWE-3". In: *IFAC Proceedings Volumes (IFAC-PapersOnline)*. Vol. 19. PART 1. Wuurzburg, Germany: IFAC, pp. 218–223. ISBN: 9783902823465. DOI: 10.3182/20130902-5-DE-2040.00107 (cit. on pp. 6, 7, 21, 22).

CERN (2019). *Radiation Hardness Assurance*. [Accessed: 9th January 2020]. URL: http://lhcb-elec.web.cern.ch/lhcb-elec/html/radiation_hardness.htm (cit. on p. 68).

Dialog Semiconductor, DS (2015). *Application note: PCB Layout Guidelines*. Tech. rep., pp. 1–21 (cit. on pp. 40–42).

DTU (2010). *DTUsat Project*. [Accessed: 21st August 2019]. URL: http://www.dtusat.dtu.dk/index.php?id=home (cit. on p. 1).

DTUSat (2006). *DTUSat-2 System Requirements Document (SDR)*. Tech. rep. DTUSat Internal Document, pp. 1–168 (cit. on pp. 2–4, 14, 68).

— (2007). "Solving the Mystery of Bird Migration : Tracking Small Birds from Space". In: 1, pp. 1–13 (cit. on p. 3).

— (2019). *DTUsat-3 System Requirements Document*. Tech. rep. DTUSat Internal Document (cit. on pp. 14, 68, 69).

ECSS, European Cooperation for Space Standardization (2008). *ECSS-Q-ST-70-38C. High-reliability soldering for surface-mount and mixed technology*. Tech. rep. March, pp. 1–33 (cit. on pp. 53, 55, 58).

— (2009). *ECSS-Q-ST-30-02C. Failure modes, effects (and criticality) analysis (FMEA/FMECA)*. Tech. rep. Marchl, pp. 1–25 (cit. on pp. 62, 63, 101, 102).

— (2012). *ECSS-Q-ST-60-15C. Radiation hardness assurance - EEE components*. Tech. rep. October, p. 32 (cit. on p. 66).

— (2017). *ECSS-Q-ST-40C Rev.1. Safety*. Tech. rep. February, pp. 1–79. DOI: ECSS-Q-ST-30-11CRev1 (cit. on p. 63).

Ehrlich, Willa K. et al. (1998). "Software reliability assessment using accelerated testing methods". In: *Journal of the Royal Statistical Society. Series C (Applied Statistics)* 47.1, pp. 15–30 (cit. on p. 108).

Eickhoff, Jens (2011). *Onboard Computers, Onboard Software and Satellite Operations: An introduction*. Springer Science & Business Media, pp. 1–282. ISBN: 9783642251696 (cit. on pp. 17, 18).

EoPortal Directory, EPD (2014a). *Delfi-C3 (Triple-unit CubeSat Configuration of TU Delft)*. [Accessed: 26th December 2019]. URL: https://earth.esa.int/web/eoportal/satellite-missions/d/delfi-c3 (cit. on p. 6).

— (2014b). *OPTOS (Optical Nanosatellite)*. [Accessed: 26th December 2019]. URL: https://earth.esa.int/web/eoportal/satellite-missions/o/optos (cit. on p. 5).

— (2015). *DTUSat-2 (Danish Technical University Satellite-2)*. [Accessed: 21st August 2019]. URL: https://directory.eoportal.org/web/eoportal/satellite-missions/d/dtusat-2 (cit. on pp. 2, 3).

EoPortal Directory, EPD (2017). *CanX-2 (Canadian Advanced Nanosatellite eXperiment-2)*. [Accessed: 26th December 2019]. URL: https://directory.eoportal.org/web/eoportal/satellite-missions/c-missions/canx-2 (cit. on p. 7).

— (2019). *UWE-4 (University Wurzburg Experimental satellite-4)*. [Accessed: 26th December 2019]. URL: https://directory.eoportal.org/web/eoportal/satellite-missions/u/uwe-4 (cit. on p. 7).

ESA (2019a). *Mitigating space debris generation*. [Accessed: 12th January 2020]. URL: https://www.esa.int/Safety_Security/Space_Debris/Mitigating_space_debris_generation (cit. on p. 16).

— (2019b). *Space Environment Information System*. [Accessed: 12th January 2020]. URL: https://www.spenvis.oma.be/ (cit. on p. 13).

Essentra Components, EC (2018). *Your PCB substrate: a guide to materials*. [Accessed: 26th December 2019]. URL: https://www.essentracomponents.com/en-gb/news/guides/your-pcb-substrate-a-guide-to-materials (cit. on p. 38).

Eurocircuits (2018). *Blind and Buried Vias*. [Accessed: 26th December 2019]. URL: https://www.eurocircuits.com/blog/Blind-and-buried-vias/ (cit. on p. 42).

— (2019). *PCB Order Details*. [Accessed: 26th December 2019]. URL: https://www.eurocircuits.com/pcb-services-overview-notes/ (cit. on pp. 40–42).

European Space Agency, ESA (2015). *OnBoar Computer and Data Handling*. [Accessed: 21st August 2019]. URL: https://www.esa.int/Our_Activities/Space_Engineering_Technology/Onboard_Computer_and_Data_Handling/Onboard_Computers (cit. on pp. 2, 17).

Fléron, Réne W. (2019). "Satellite Forensics: Analysing Sparse Beacon Data to Reveal the Fate of DTUsat-2". In: *International Journal of Aerospace Engineering* 2019, p. 12 (cit. on p. 2).

Fortescue, Peter, Graham Swinerd, and John Stark (1992). *Spacecraft Systems Engineering*. Vol. 54. 3-4, p. 481. ISBN: 9780470750124. DOI: 10.1016/0021-9169(92)90028-j (cit. on pp. 65, 66).

Gaillard, R. and Michael Nicolaidis (2011). "Chapter 2. Single Event Effects: Mechanisms and Classification". In: *Soft Errors in Modern Electronic Systems*. Vol. 41. ISBN: 978-1-4419-6992-7. DOI: 10.1007/978-1-4419-6993-4. URL: http://www.springerlink.com/index/10.1007/978-1-4419-6993-4 (cit. on pp. 66, 67).

GE Healthcare (2011). *Solder joint inspection and analysis*. URL: http://www.temasek.com.sg/abouttemasek/faqs{\#} (cit. on pp. 50, 51).

Hansen, Flemming and Denis Tcherniak (2017a). *Ulloriaq SEE Radiation Test Procedure*. Tech. rep., pp. 1–26 (cit. on pp. 67, 68).

— (2017b). *Ulloriaq TID Radiation Test Procedure*. Tech. rep., pp. 1–30 (cit. on pp. 67, 68, 110, 112).

Hansen, Jesper and Tue Appel (2009). "Visualization of DTUsat-2". PhD thesis (cit. on p. 1).

Hausherr, Tom (2007). "Metric Pitch BGA and Micro BGA routing solutions". In: *Printed Circuit Design & Manufacture* 24.11, pp. 36–41 (cit. on p. 40).

Hsieh, Wen Ching et al. (2016). "Performance improvement of total ionization dose radiation sensor devices using fluorine-treated MOHOS". In: *Sensors (Switzerland)* 16.4. ISSN: 14248220. DOI: 10.3390/s16040450 (cit. on p. 67).

IEC, International Electrotechnical Commission (2006). "IEC Standard 60812". In: 2006, p. 13 (cit. on p. 62).

IPC, Association Connecting Electronics Industries (2004). *IPC-A-610D Acceptability of Electronic Assemblies*. Tech. rep. (cit. on pp. 46, 49).

Johnston, A. H. (2001). "Radiation Damage of Electronic and Optoelectronic Devices in Space". In: *4th International Workshop on Radiation Effects on Semiconductor Devices for Space Application*, pp. 1–9. URL: https://www.nepp.nasa.gov/docuploads/D41D389D-04D4-4710-BBCFF24F4529B3B3/Dmg{_}Space-00.pdf (cit. on pp. 67, 68).

Kiadtikornthaweeyot, Warinthorn (2015). "Onboard computer technology for Cubesats". PhD thesis. University of Southampton, p. 309. ISBN: 3333333333 (cit. on pp. 18–21).

KiCad (2014). *Introduction to Pcbnew*. [Accessed: 26th December 2019]. URL: https://docs.kicad-pcb.org/5.1.5/en/pcbnew/pcbnew.html#introduction (cit. on pp. 39, 41).

Kridner, Jason (2019). *PocketBeagle System Reference Manual*. [Accessed: 29th December 2019]. URL: https://www.essentracomponents.com/en-gb/news/guides/your-pcb-substrate-a-guide-to-materials (cit. on pp. 26–28, 73).

Label, Kenneth A. (2004). *Total Ionizing Dose (TID) Effects*. [Accessed: 9th January 2020]. URL: https://radhome.gsfc.nasa.gov/radhome/tid.htm (cit. on p. 68).

Lee, Ning Cheng (1999). "Optimizing the reflow profile via defect mechanism analysis". In: *Soldering and Surface Mount Technology* 11.1, pp. 13–20. ISSN: 09540911. DOI: 10.1108/09540919910254642 (cit. on p. 46).

— (2002). *Reflow Soldering Processes and Troubleshooting- SMT, BGA, CSP and Flip Chip Technologies*, p. 284 (cit. on pp. 42–48).

Ma, Ji Quan et al. (2005). "Detection of defects at BGA solder joints by using X-ray imaging". In: *International Conference on Machine Learning and Cybernetics*, pp. 5139–5143. ISBN: 078039092X. DOI: 10.1109/ICIT.2002.1189898 (cit. on p. 50).

Martín-Ortega, Alberto et al. (2019). "Data Analysis and Results of the Radiation-Tolerant Collaborative Computer On-Board OPTOS CubeSat". In: *International Journal of Aerospace Engineering* 2019. ISSN: 16875974. DOI: 10.1155/2019/1425892 (cit. on p. 5).

Millennium Circuits Limited, MCL (2019). *Types of vias*. [Accessed: 26th December 2019]. URL: https://www.mclpcb.com/types-of-vias/ (cit. on p. 41).

Mozaffari, Fatemeh et al. (2013). "Implementation of FMEA to improve the reliability of GEO satellite payload". In: *Annual Reliability and Maintainability Symposium*, pp. 2–7. ISBN: 9781467347099. DOI: 10.1109/RAMS.2013.6517679 (cit. on p. 62).

NASA (2014). *COTS Components in Spacecraft Systems : Understanding the Risk*. Tech. rep., pp. 10–11 (cit. on p. 1).

Nguty, T. A., N. N. Ekere, and A. Adebayo (1999). "Correlating solder paste composition with stencil printing performance". In: *IEEE/CPMT International Electronics Manufacturing Technology (IEMT) Symposium*, pp. 304–312. ISBN: 0780355032. DOI: 10.1109/iemt.1999.804837 (cit. on pp. 43, 44).

Octavo Systems (2017). *OSD335x-SM Family Datasheet*. Tech. rep., pp. 0–31 (cit. on pp. 29, 71, 95, 97).

Octavo Systems, OS (2015). *OSD335x-SM System-in-Package Smallest AM335x Module, Quickest Design*. [Accessed: 21st August 2019]. URL: http://octavosystems.com/octavo_products/osd335x-sm/ (cit. on pp. 12, 29, 58–61, 164).

Paccagnella, Alessandro, Simone Gerardin, and Giorgio Cellere (2009). "Radiation damage on dielectrics: Single event effects". In: *Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures* 27.1, pp. 406–410. ISSN: 10711023. DOI: 10.1116/1.3054271 (cit. on pp. 66, 67).

Paslaru, Dorin (2015). *Stressapptest*. [Accessed: 9th January 2020]. URL: https://github.com/thenoizz/stressapptest/wiki/Introduction (cit. on p. 108).

Portela-García, Marta et al. (2011). "Sensitivity evaluation method for aerospace digital systems with collaborative hardening". In: *IEEE Transactions on Nuclear Science* 58.3, pp. 1053–1058. ISSN: 00189499. DOI: 10.1109/TNS.2011.2109397 (cit. on p. 6).

Pumpkin Inc, PI (2013). *Begin your CubeSat Mission with the CubeSat Kit*. [Accessed: 26th December 2019]. URL: http://www.cubesatkit.com/2 (cit. on p. 6).

Rankin, Daniel et al. (2005). "The CanX-2 nanosatellite: Expanding the science abilities of nanosatellites". In: *Acta Astronautica* 57.2-8, pp. 167–174. ISSN: 00945765. DOI: 10.1016/j.actaastro.2005.03.032 (cit. on p. 7).

Sarda, Karan et al. (2006). "Canadian advanced nanospace experiment 2: Scientific and technological innovation on a three-kilogram satellite". In: *Acta Astronautica* 59.1-5, pp. 236–245. ISSN: 00945765. DOI: 10.1016/j.actaastro.2006.02.054 (cit. on p. 7).

Shang, Haixia et al. (2008). "Thermal performance of lead-free microelectronic BGA package with defects". In: *17th World Conference on Nondestructive Testing*. 25-28 October. Shanghai, China (cit. on pp. 50, 53).

Shapiro, Andrew A. et al. (2006). "Implications of Pb-free microelectronics assembly in aerospace applications". In: *IEEE Transactions on Components and Packaging Technologies* 29.1, pp. 60–70. ISSN: 15213331. DOI: 10.1109/TCAPT.2005.850514 (cit. on p. 43).

Speretta, Stefano et al. (2016). "CubeSats to PocketQubes: Opportunities and challenges". In: *International Astronautical Congress, IAC*. September (cit. on p. 10).

Srour, J. R. and J. W. Palko (2013). "Displacement damage effects in irradiated semiconductor devices". In: *IEEE Transactions on Nuclear Science* 60.3, pp. 1740–1766. ISSN: 00189499. DOI: 10.1109/TNS.2013.2261316 (cit. on p. 67).

Svasta, Paul and Daniel Simion-Zanescu (2003). "Thermal limits in reflow soldering process". In: *Electronic Components and Technology Conference*, pp. 1839–1842. DOI: 10.1109/ectc.2003.1216553 (cit. on p. 44).

Swartwout, Michael (2016). "Secondary spacecraft in 2016: Why some succeed (And too many do not)". In: *IEEE Aerospace Conference Proceedings*. Vol. 2016-June. ISBN: 9781467376761. DOI: 10.1109/AERO.2016.7500791 (cit. on p. 122).

Texas Instruments, TI (1999). *PCB Design Guidelines For Reduced EMI*. Tech. rep. November, p. 23. URL: http://www.ti.com/lit/an/szza009/szza009.pdf (cit. on pp. 40, 41).

— (2002). *SN65HVD23x 3.3-V CAN Bus Transceivers Datasheet*. Tech. rep. URL: http://www.ti.com/lit/ds/symlink/sn65hvd235.pdf (cit. on p. 37).

The CubeSat Program, CSP (2014). *CubeSat Design Specification* (cit. on p. 1).

Torex (2019). *XCL102/XCL103 Series. Inductor Built-in Step-up âĂIJmicro DC/DCâĂİ Converter (micro DC/DC) Datasheet*. Tech. rep., pp. 1–20 (cit. on pp. 33, 35, 81).

Townsend, Julie, Bryan Palmintier, and Eric Allison (2000). "Effects of a Distributed Computing Architecture on the Emerald Nanosatellite Development Process". PhD thesis. Stanford University, pp. 1–11 (cit. on p. 20).

Trinh, Greenfield T. et al. (2015). "Modular rapidly manufactured small satellite (MRMSS)". In: *53rd AIAA Aerospace Sciences Meeting*, pp. 1–11. DOI: 10.2514/6.2015-0941 (cit. on p. 9).

Wickham, M et al. (1999). *An Investigation Into Ball Grid Array Inspection Techniques*. Tech. rep. September. ESA STM-261 (cit. on pp. 50, 51, 53, 54).

Wuerzburg University, UW (2016). *UWE-3*. [Accessed: 26th December 2019]. URL: http://www7.informatik.uni-wuerzburg.de/forschung/space-exploration/projects/uwe-3/ (cit. on pp. 6, 7).

Yunus, Mohammad et al. (2000). "Effect of voids on the reliability of BGA/CSP solder joints". In: *Twenty Sixth IEEE/CPMT International Electronics Manufacturing Technology Symposium*. Vol. 43. 12, pp. 2077–2086. ISBN: 0780364821. DOI: 10.1016/S0026-2714(03)00124-0 (cit. on p. 53).

Zenteno, Antonio, David Reina, and Gabriel Regalado (2010). "Optimization of PCB via design considering its physical length parameters". In: *Midwest Symposium on Circuits and Systems*. IEEE, pp. 256–259. ISBN: 9781424477715. DOI: 10.1109/MWSCAS.2010.5548778 (cit. on p. 41).

Zumbahlen, Hank (2008). "Printed Circuit-Board Design Issues". In: *Linear Circuit Design Handbook*, pp. 821–895. DOI: 10.1016/b978-0-7506-8703-4.00012-2 (cit. on p. 41).

Zweig, Gil (2002). "Enhance your BGA x-ray inspection process". In: *Circuits Assembly* 13.5, pp. 47–50. ISSN: 10540407 (cit. on pp. 52, 53).

Zweig, Gil (2003). "Using Signature Identification for Rapid and Effective X-Ray Inspection of Ball Grid Arrays". In: *SMTA International* (cit. on pp. 52–57).

Appendices

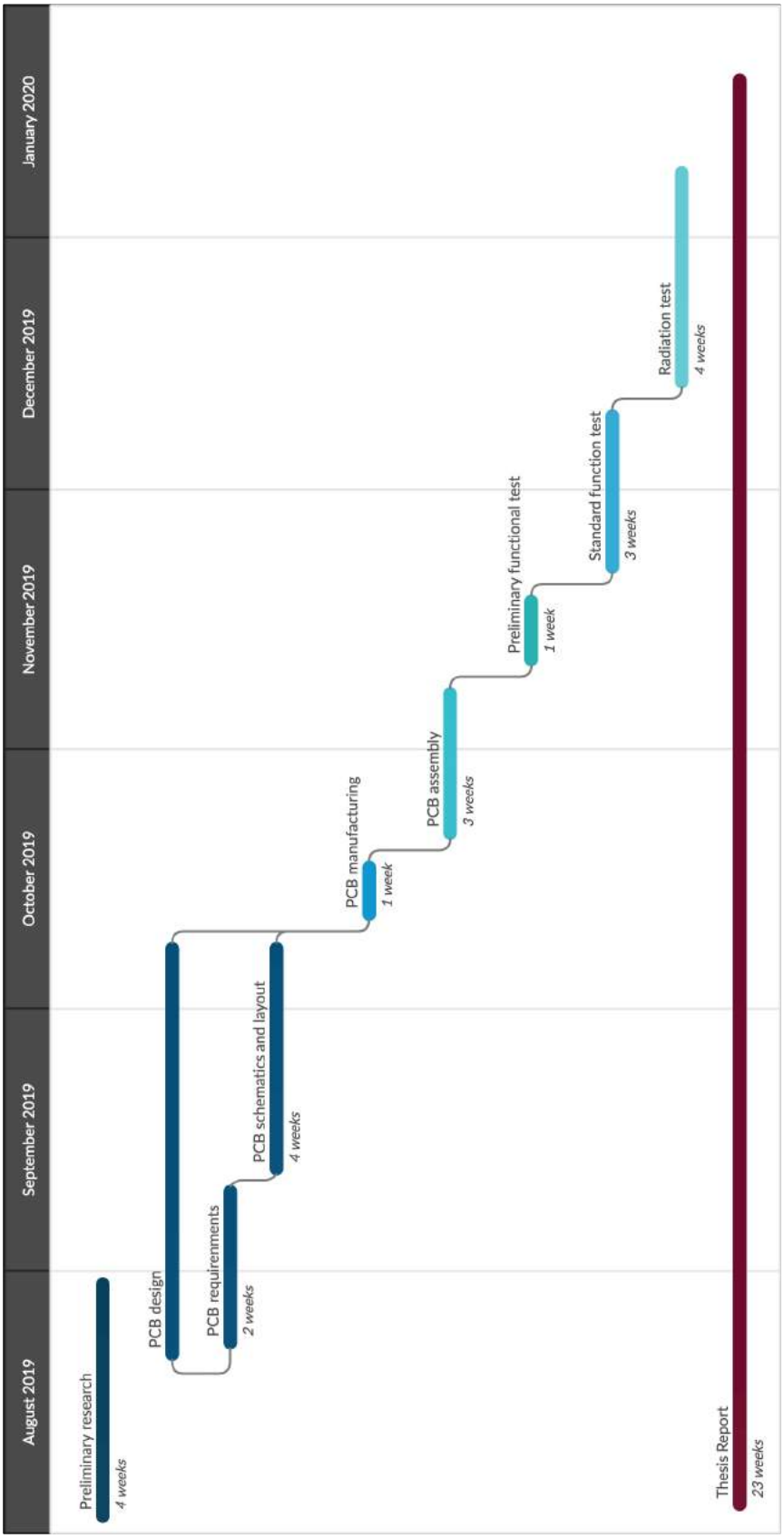
Appendix A

Abbreviations

BGA	Ball Grid Array
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide-Semiconductor
COTS	commercial Off The Shelf Components
DD	Displacement Damage
EDAC	Error Detection and Correction
FMEA	Failure Mode and Effects Analysis
FMECA	Failure Mode, Effects and Criticality Analysis
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
LEO	Low Earth Orbit
MCU	Microcontroller Unit
PCB	Printed Circuit Board
PMIC	POwer Management Integrated Circuit
SEE	Single Event Effect
SEGR	Single Event Gate Rupture
SEL	Single Event Latch-up
SEU	Single Event Upset
SMC	Surface Mounted Component
SPI	Serial Peripheral Interface
SSCB	Subsystem Carrier Board
TID	Total Ionizing Dose
TUW	Toggle Watchdog Unit
UART	Universal Asynchronous Receiver-Transmitter

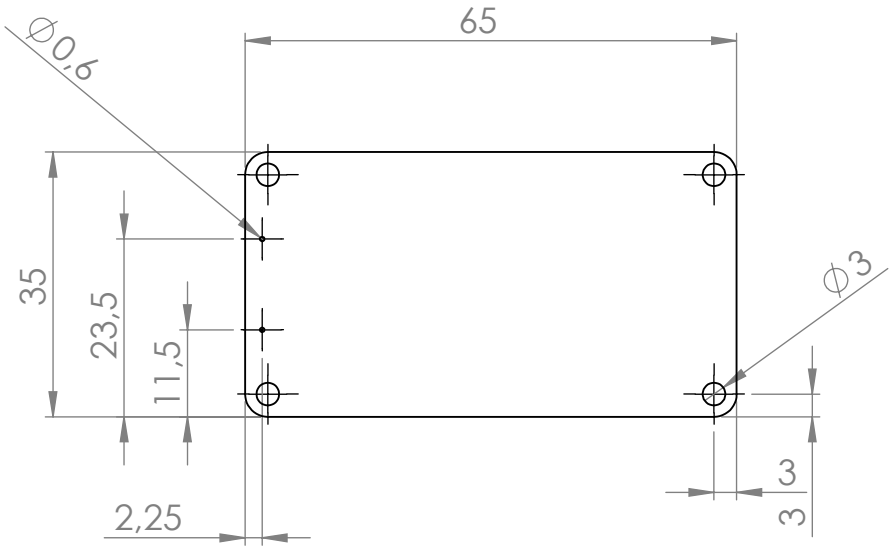
Appendix B

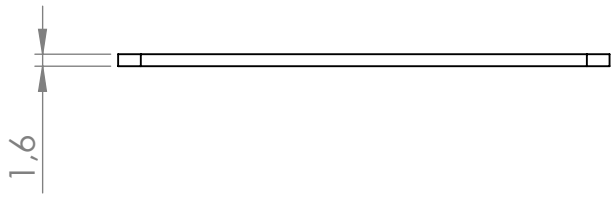
Project's Gantt Diagram

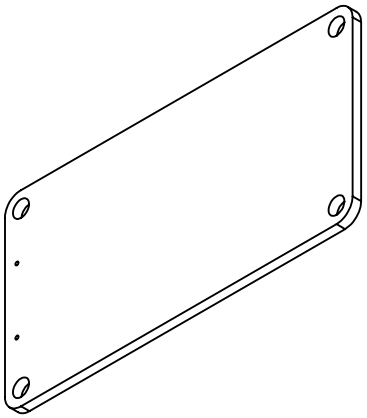

August 2019
September 2019
October 2019
November 2019
December 2019
January 2020
Preliminary research
4 weeks
PCB design
PCB requirenments
2 weeks
PCB schematics and layout
4 weeks
PCB manufacturing
1 week
PCB assembly
3 weeks
Preliminary functional test
1 week
Standard function test
3 weeks
Radiation test
4 weeks
Thesis Report
23 weeks

Appendix C

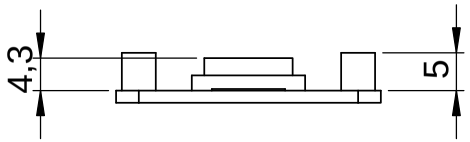
Board mechanical drawings

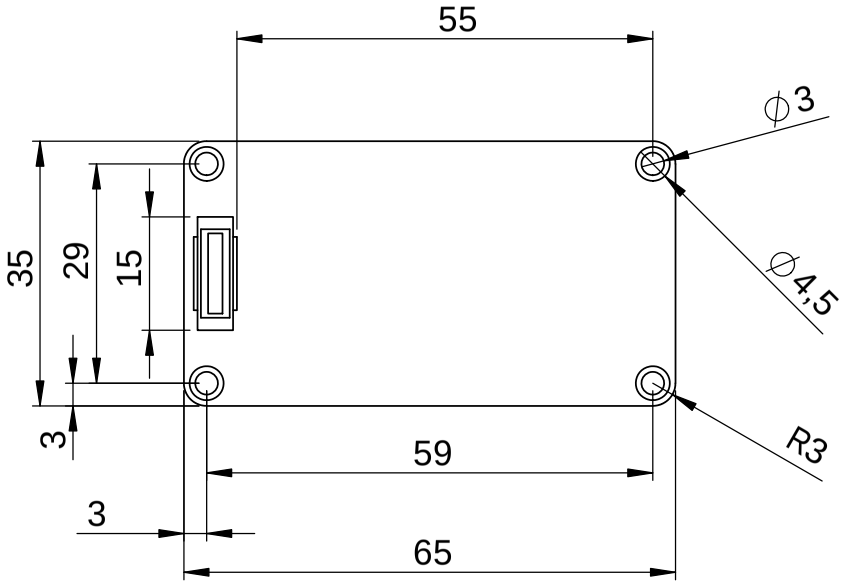


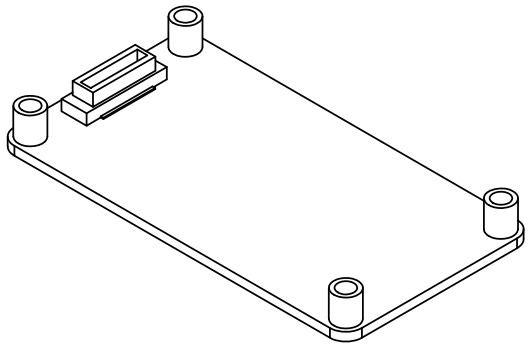




UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS SURFACE FINISH: TOLERANCES: LINEAR: ANGULAR:	FINISH:		DEBUR AND BREAK SHARP EDGES		DO NOT SCALE DRAWING	REVISION
	NAME	SIGNATURE	DATE		TITLE:	
DRAWN						
CHK'D						
APPV'D						
MFG						
Q.A				MATERIAL:	DWG NO. PCB 35x65	A4
				WEIGHT:	SCALE:1:1	SHEET 1 OF 1







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	NAME	SIGNATURE	DATE
DRAWN			
CHK'D			
APPV'D			
MFG			
Q.A			

DO NOT SCALE DRAWING	REVISION
TITLE:	
MATERIAL:	
DWG NO. PCB 35x65_v1	A4
WEIGHT:	SCALE:1:1
	SHEET 1 OF 1

Appendix D

SPENVIS

In this appendix, the SPENVIS graphs that were obtained and from which the Total Ionizing Dose for the OBC of DTUSat-3 was estimated are presented.

D.1 Coordinate generators

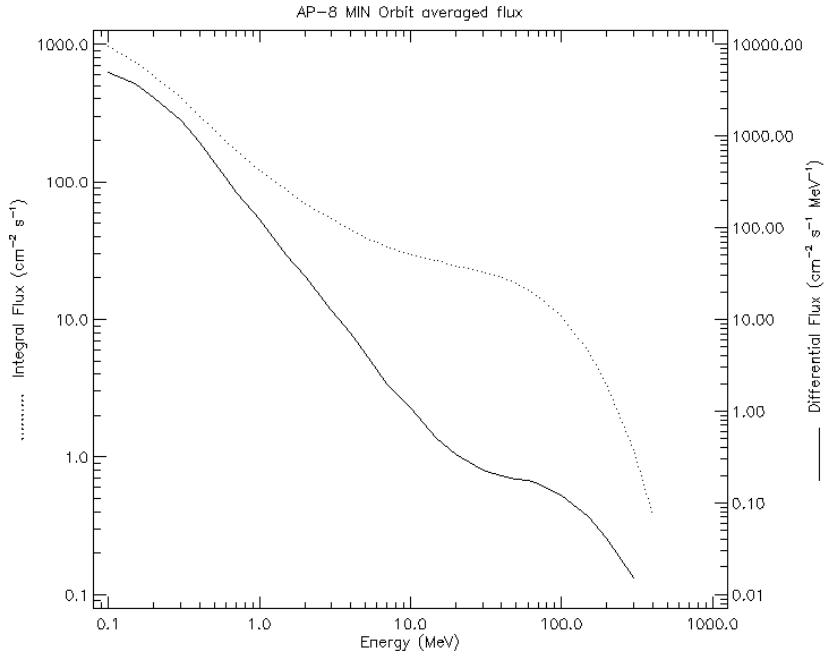
First of all, a mission was created in SPENVIS. For this, in the "Spacecraft trajectories" coordinate generator, the design parameters shown in the following table were introduced. Moreover, no solar radiation pressure and no atmospheric drag were considered.

Orbit type	General
Orbit start	11/01/2020 at 00:00:00
Number of orbits	10
Altitude specification	Circular orbit
Altitude	550 - 700 km
Inclination	98°

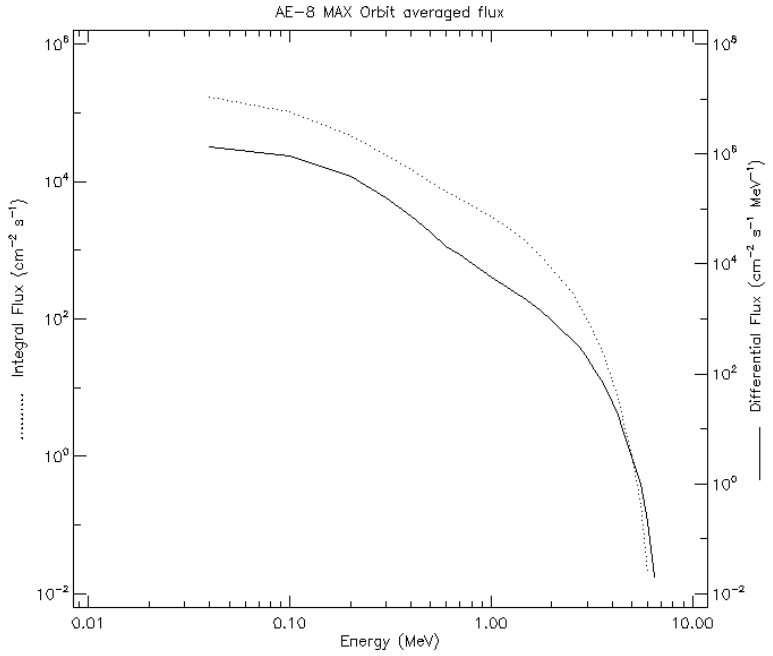
D.2 Trapped protons and electron fluxes

Next, the "Trapped protons and electron fluxes" model was run. Here, the AP-8 solar maximum model was used for the protons and the AE-8 solar minimum model was used for the electrons.

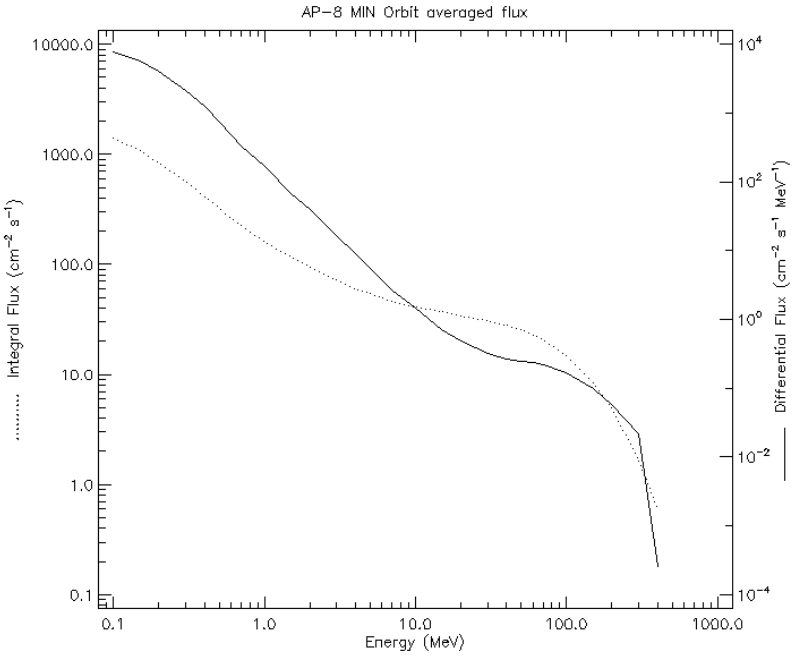
Trapped protons at 550 km



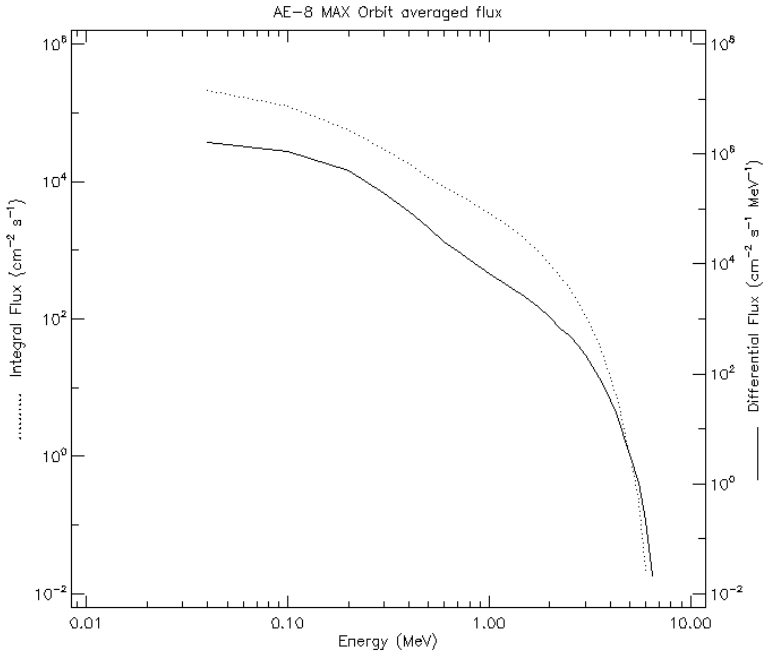
Electron fluxes at 550 km



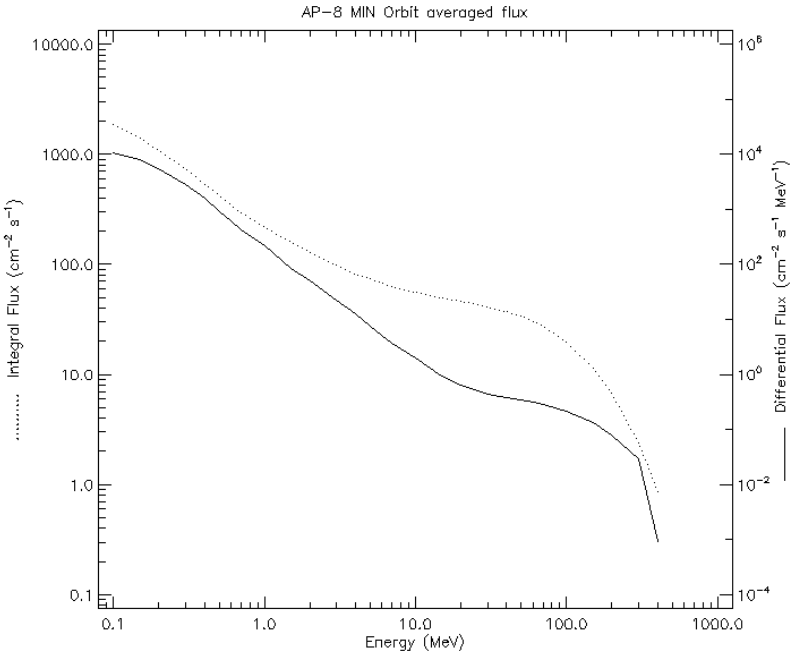
Trapped protons at 600 km



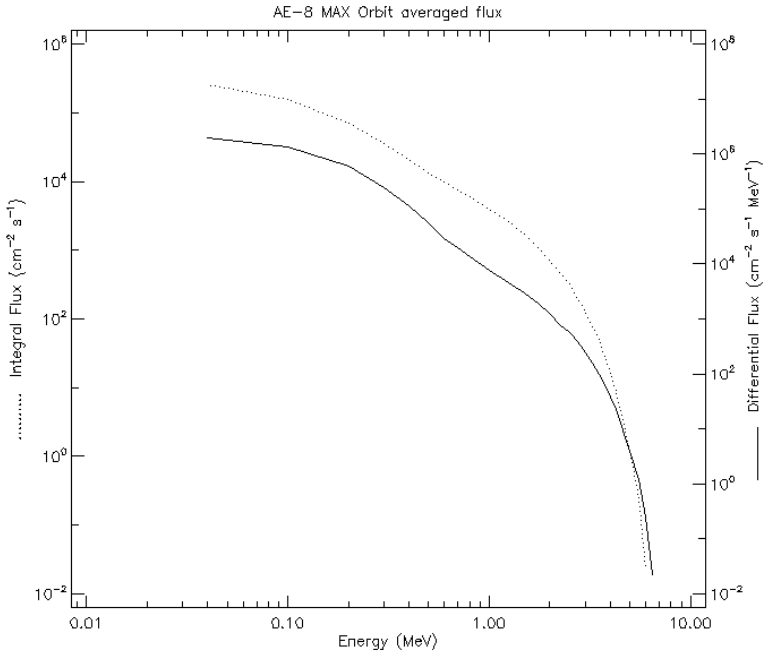
Electron fluxes at 600 km



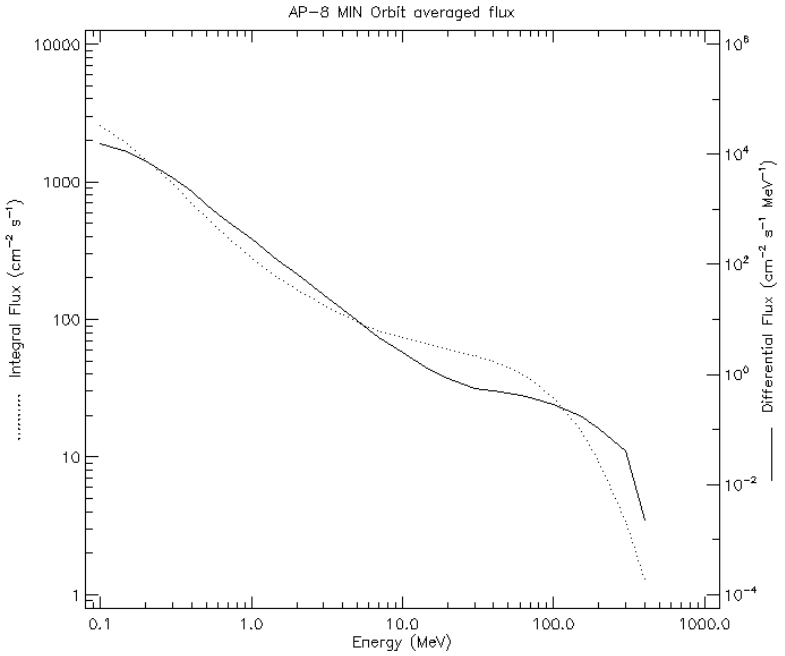
Trapped protons at 650 km



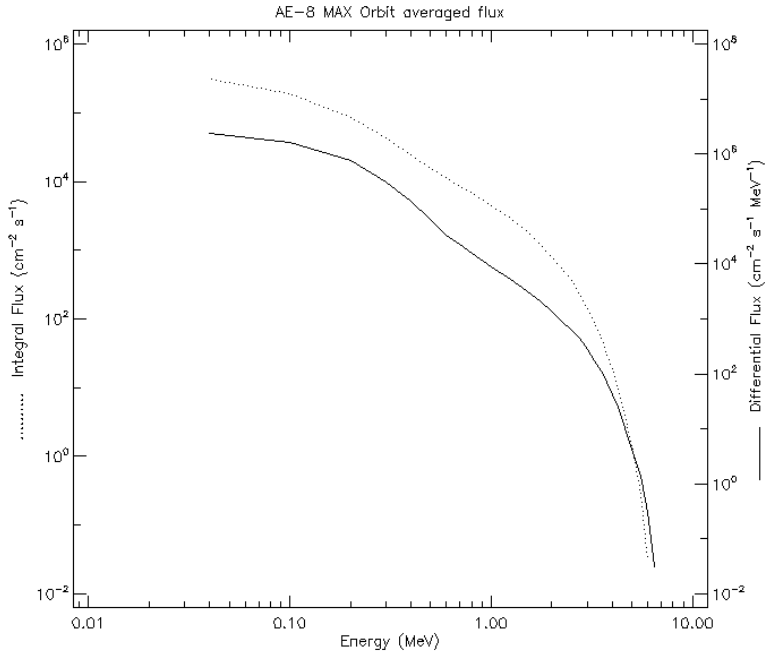
Electron fluxes at 650 km



Trapped protons at 700 km



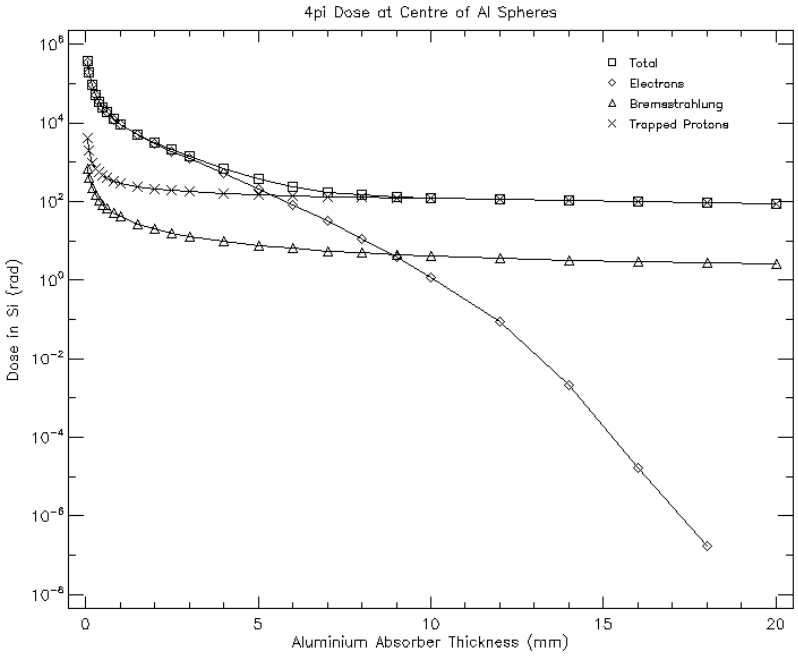
Electron fluxes at 700 km



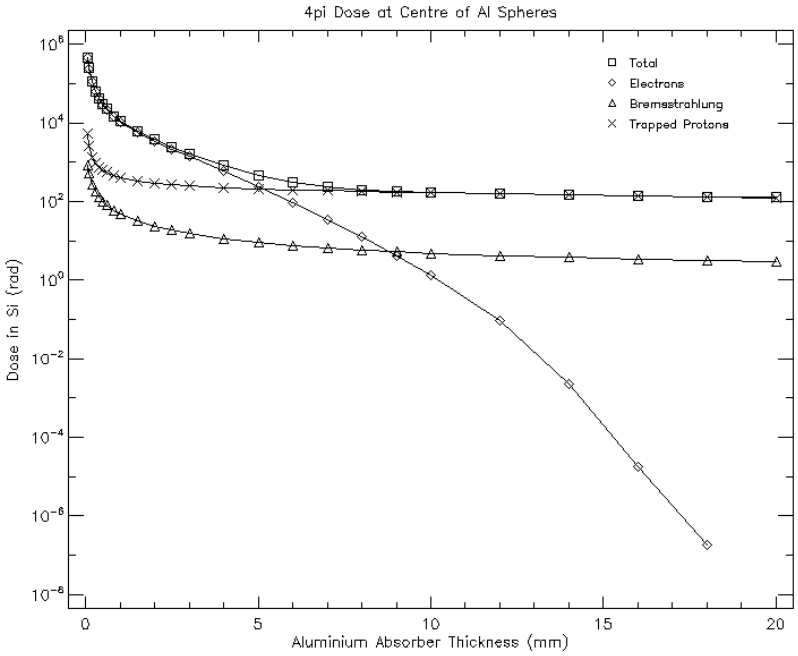
D.3 Ionizing dose for simple geometries

Finally, the "Ionizing dose for simple geometries" model was run, using SHIELDOSE-2, with Silicon as the target material and shielding configuration as center of aluminum sphere.

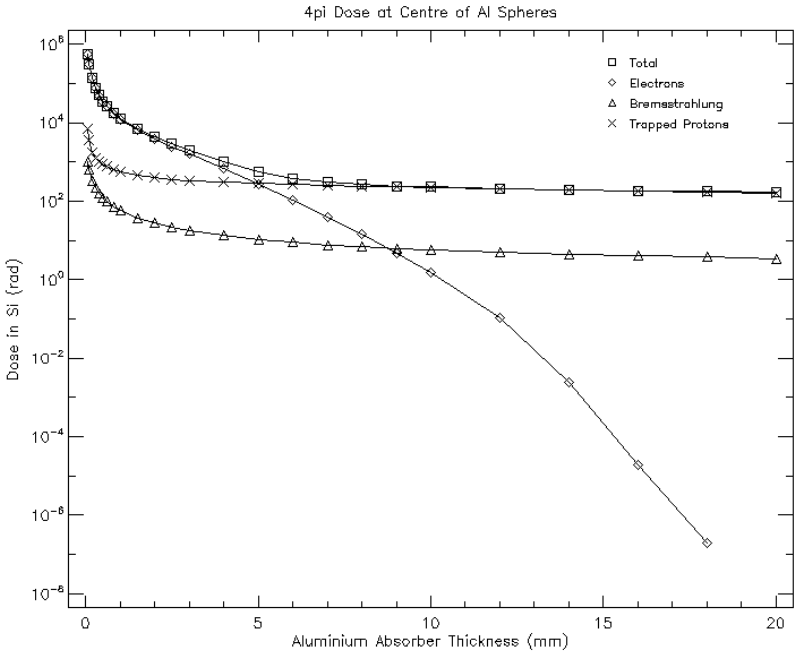
Ionizing dose for 1.5 years at 550 km



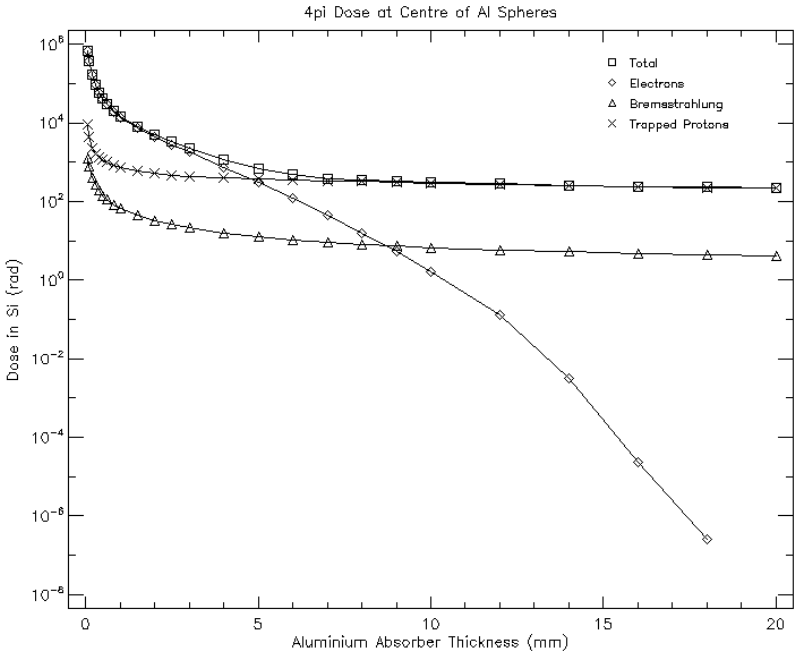
Ionizing dose for 1.5 years at 600 km



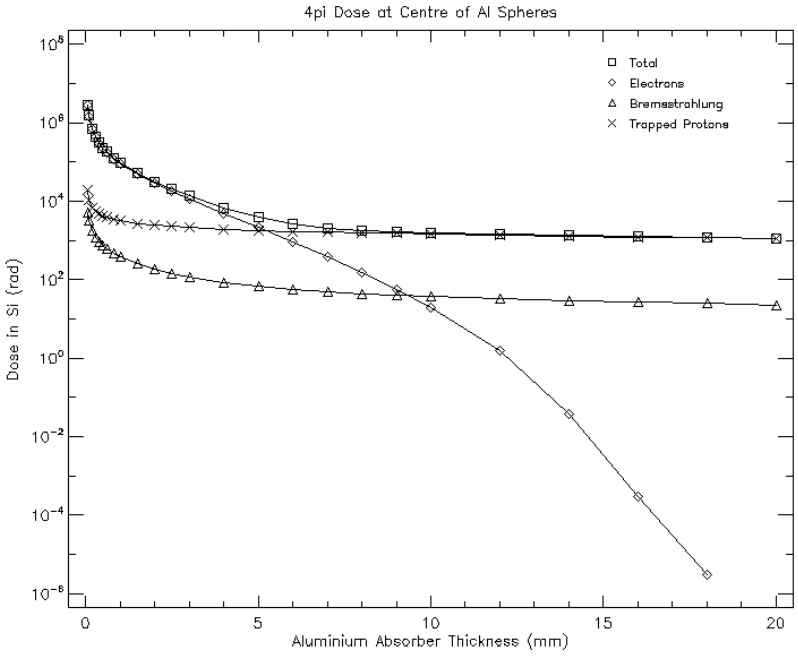
Ionizing dose for 1.5 years at 650 km



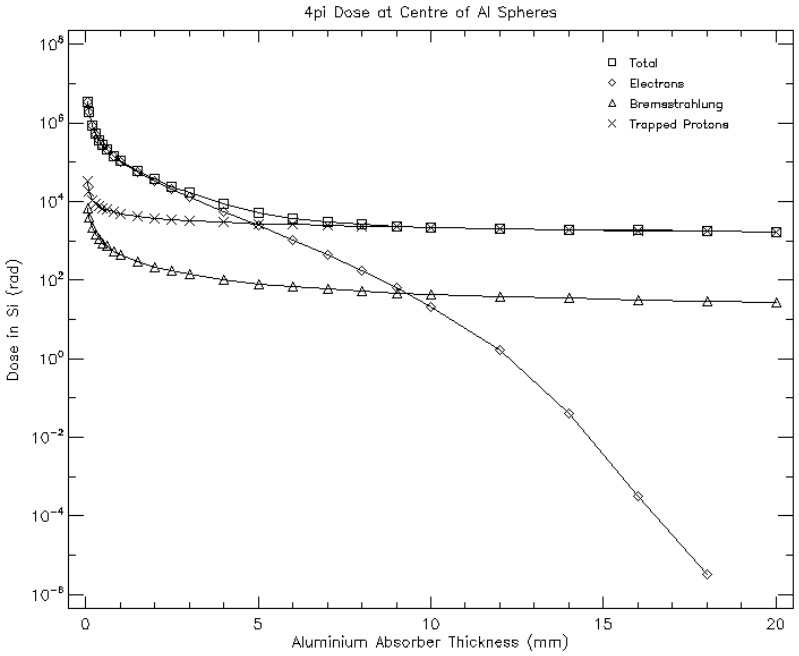
Ionizing dose for 1.5 years at 700 km



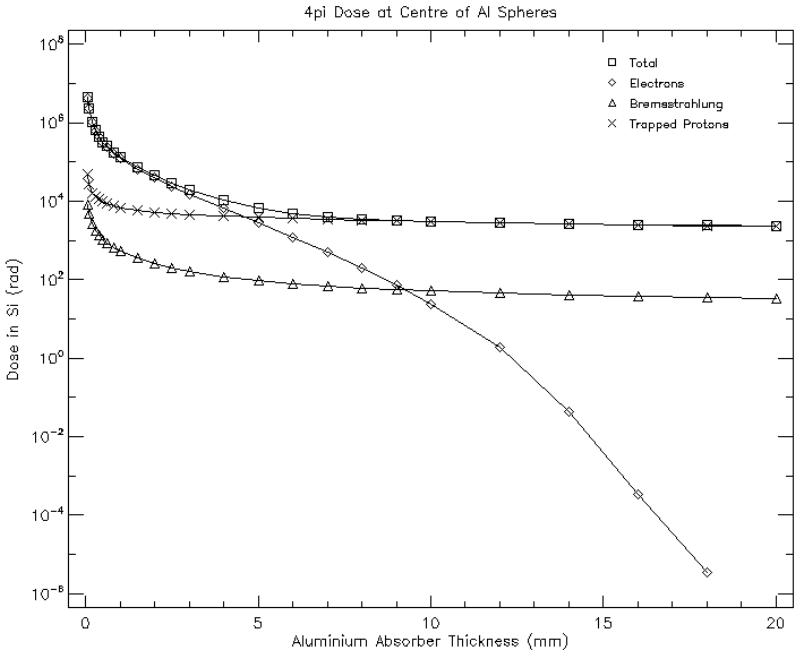
Ionizing dose for 27 years at 550 km



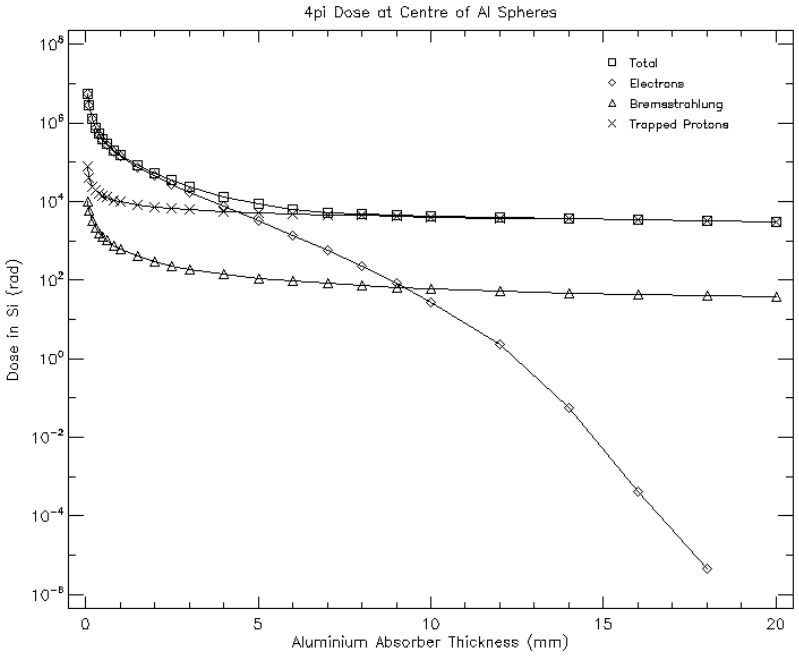
Ionizing dose for 27 years at 600 km



Ionizing dose for 27 years at 650 km



Ionizing dose for 27 years at 700 km



Appendix E

Bill of Materials

Designator	Manufacturer/MPN	Description
C1,C5,C7	YAGEO CC0402KRX7R7BB104	Cap,100nF,10%,16V,X7R,0402,YAGEO
C2,C3	YAGEO CC0402JRNPO9BN180	CAP 18pF 5% 50V COG 0402 SMD
C4	YAGEO CC0402KRX5R5BB105	CAP,1UF,+/-10%,X5R,6.3V,SMD0402
C8	AVX 04023C104KAT2A	0.1µF ±10% 25V Ceramic Capacitor X7R 0402 (1005 Metric)
C6,C9,C10	AVX 0805ZC106KAT2A	10µF ±10% 10V Ceramic Capacitor X7R 0805 (2012 Metric)
FB1,FB2	Laird LI0603G121R-10	FERRITE BEAD 120 OHM 0603 1LN
POWER	C&K Components KMR231GLFS	SWITCH TACTILE SPST-NO 0.05A 32V
R1	YAGEO RC0402FR-071KL	RES,1K,+/-1%,1/16W,SMD0402
R2	YAGEO RC0402FR-071ML	RES,1M,+/-1%,1/16W,SMD0402
R3,R12	YAGEO RC0402FR-0710KL	RES,10K,+/-1%,1/16W,SMD0402
R4	YAGEO YC124-JR-071KL	RES 4 Arrays,1K,+/-5%,1/16W,SMD0804(0402X4)
R5,R10,R11	YAGEO YC124-JR-0710KL	RES 4 Arrays,10K,+/-5%,1/16W,SMD0804(4x0402)
R6,R7,R8,R9	YAGEO YC124-JR-07100KL	RES 4 Arrays,100K,+/-5%,1/16W,SMD0804(0402X4)
R13, R14	Panasonic ERJ-2RKF1002X	10 kOhms ±1% 0.1W, 1/10W Chip Resistor 0402 (1005 Metric) Automotive AEC-Q200 Thick Film
U1	Octavo Systems OSD3358-512M-BSM	IC,the smallest System-In-Package (SiP) device in the OSD335x Family,OSD3358-512M-BSM,BGA256,SMD,0-85ºC
U2	Texas Instruments SN74LVC1G07DCKR	IC,SINGLE BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT,SN74LVC1G07DCKR,SC-70,SMD
U3	Texas Instruments TPD4S012DRYR	IC,4-CHANNEL ESD SOLUTION FOR USB OTG,TPD4S012DRYR,6SON,SMD
U4	Texas Instruments SN65HVD234D	3.3V CAN Transceiver
U5	Torex Semiconductor Ltd XCL103D503CR-G	Non-Isolated PoL Module DC DC Converter 1 Output 4.9 ~ 5.1V 500mA 0.9V - 6V Input
USR0,USR1,USR2,USR3,PWR	Lite-On Inc. LTST-C191TBKT	Blue 470nm LED Indication - Discrete 3.3V 0603 (1608 Metric)
X1	MTCONN UBAF-06082, FCI 10118192-0001LF	Conn,Micro USB B,5pin,RA, SMT
J2	Molex 5033981892	9 (8 + 1) Position Card Connector microSD™ Surface Mount, Right Angle Gold
Y1	Interquip 5XBB24000183TF50Q3	24MHz crystal, SMD, 5x3.2mm
J1	Hirose DF17(2.0)-40DP-0.5V(57)	40 Position Connector Header, Outer Shroud Contacts Surface Mount Gold

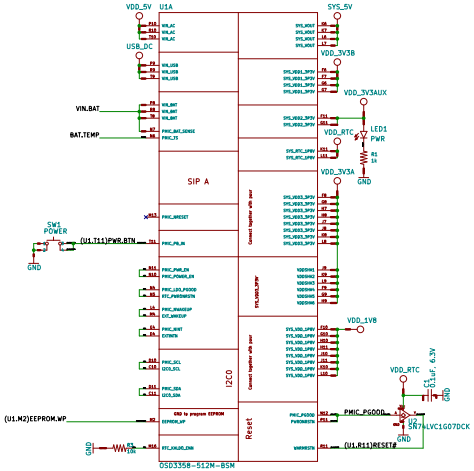
Appendix F

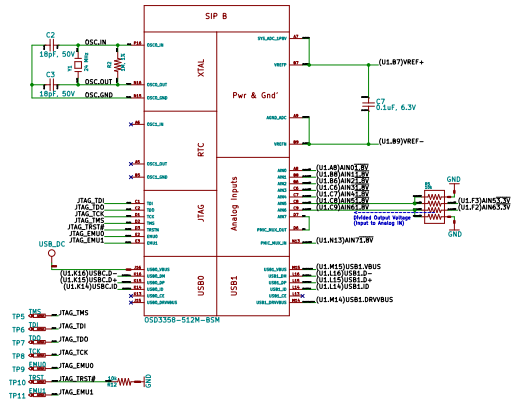
KiCad circuit schematics

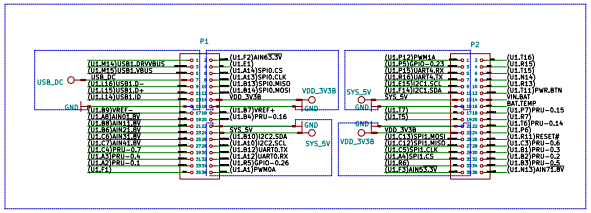
DTUSat OBC Rev. 3

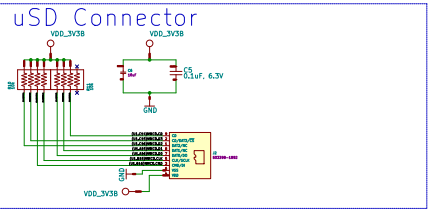
By Blanca Alejo Gago

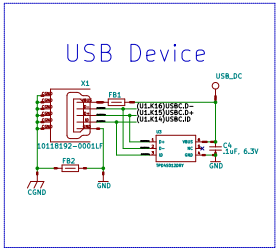
October 2019

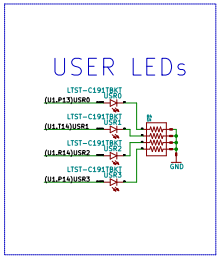


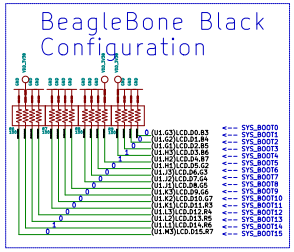


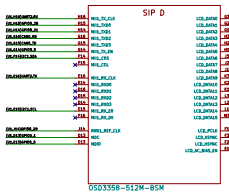


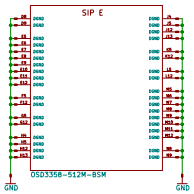


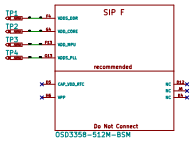


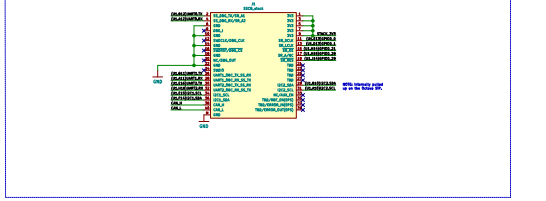


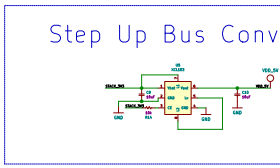


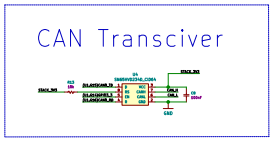












Designed by: Blanca Alejo Gago

Sheets: /

File: PocketBeagle.sch

Title: DTUSat OBC Rev. 3

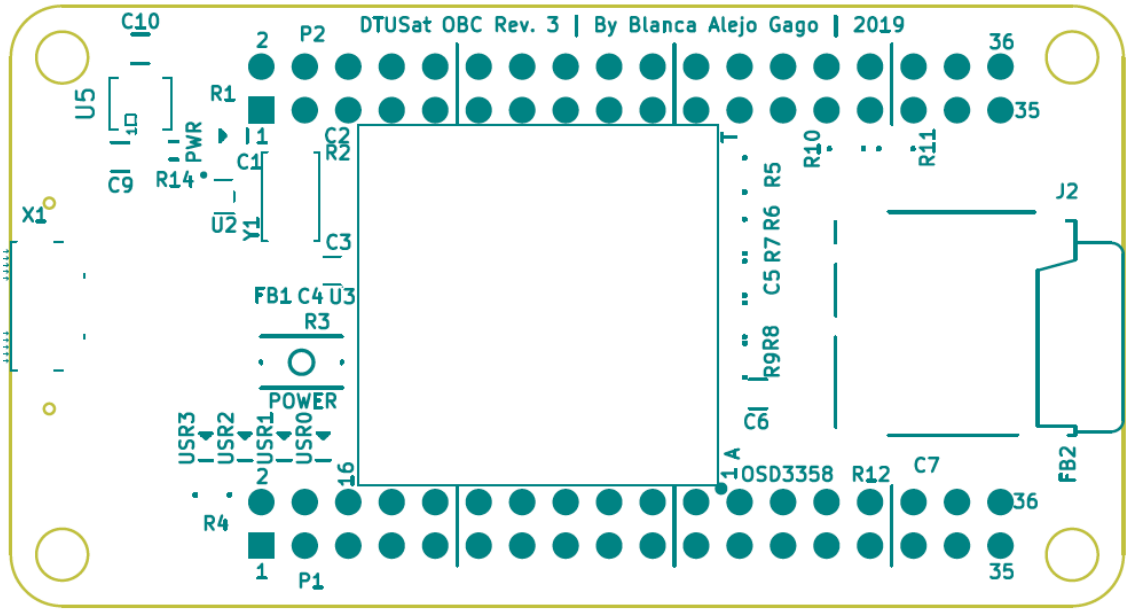
Size: D | Date: 2019-10-24 | Rev:

KiCad E.D.A. kicad (5.1.4-0) | Id: 1/1

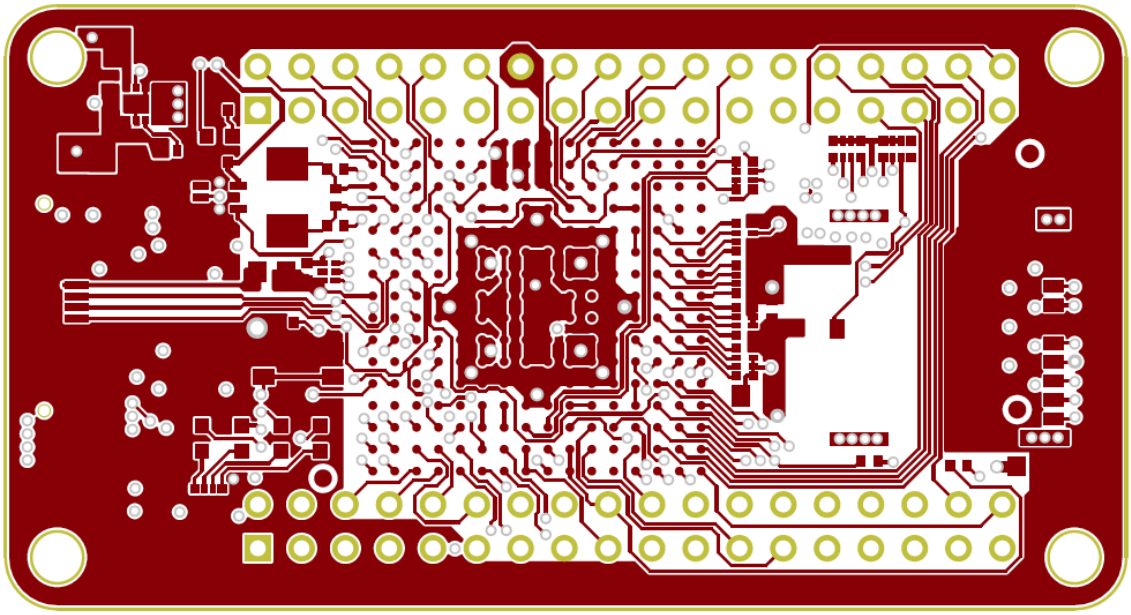
Appendix G

KiCad PCB layout

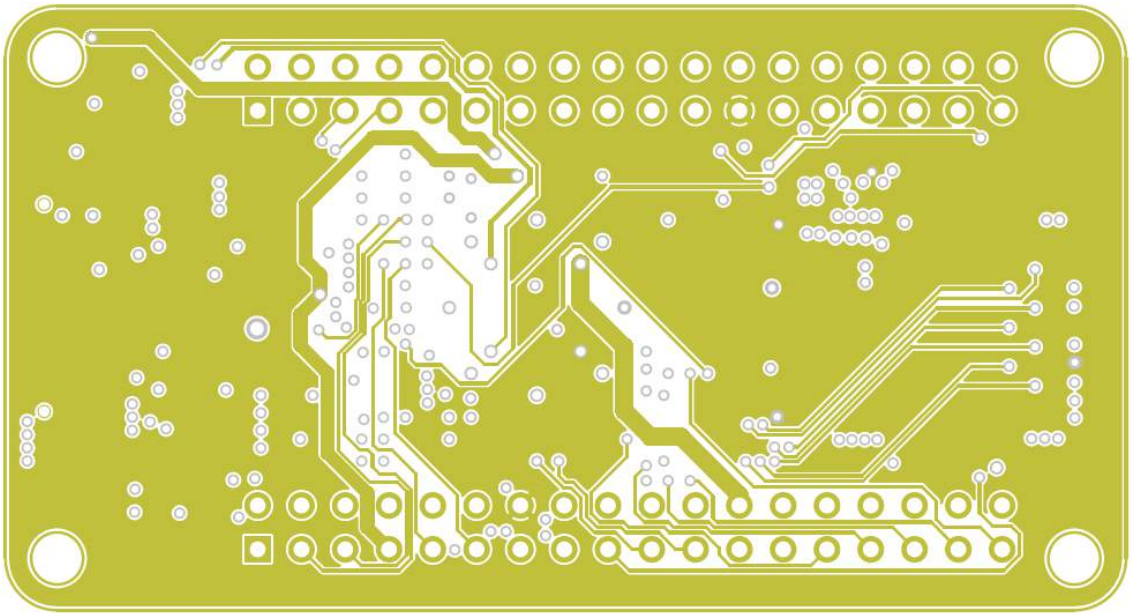
G.1 Front silk screen



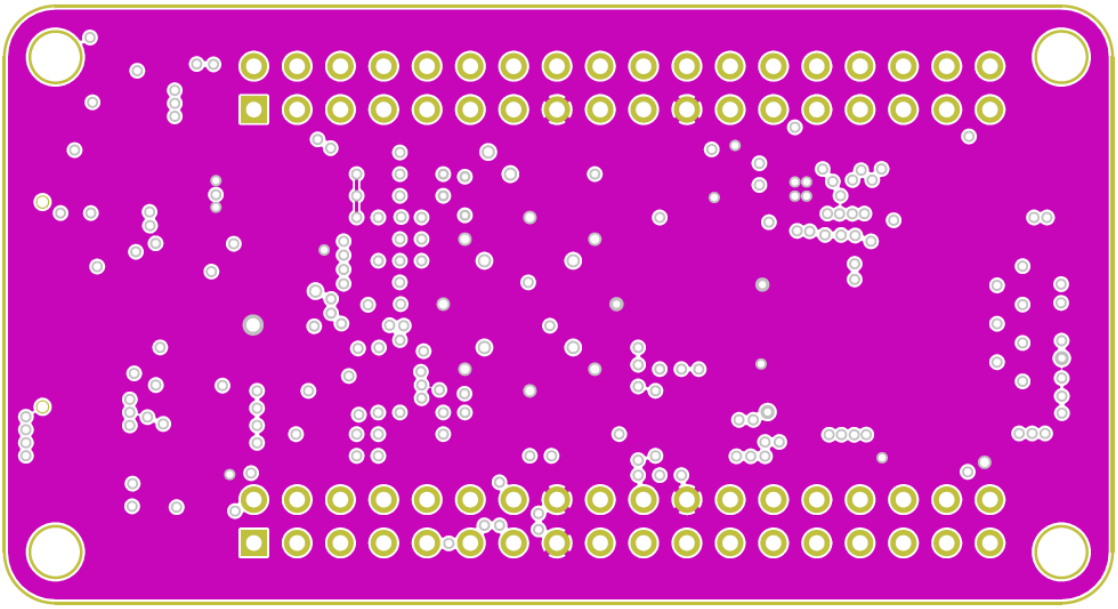
G.2 Cooper layer 1: Top



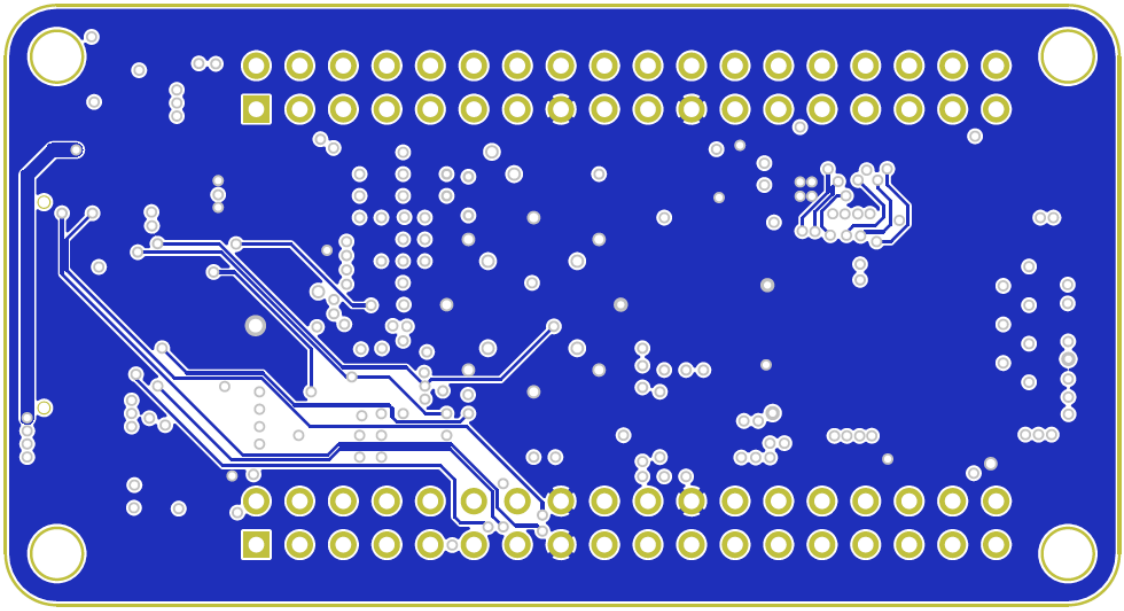
G.3 Cooper layer 2: main power



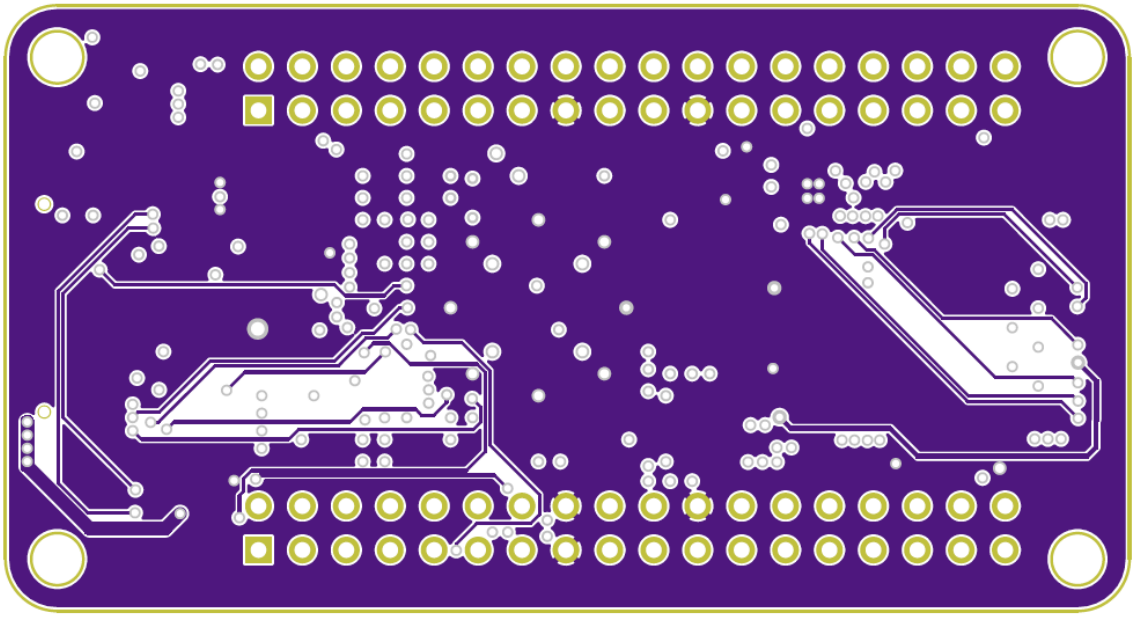
G.4 Cooper layer 3: ground



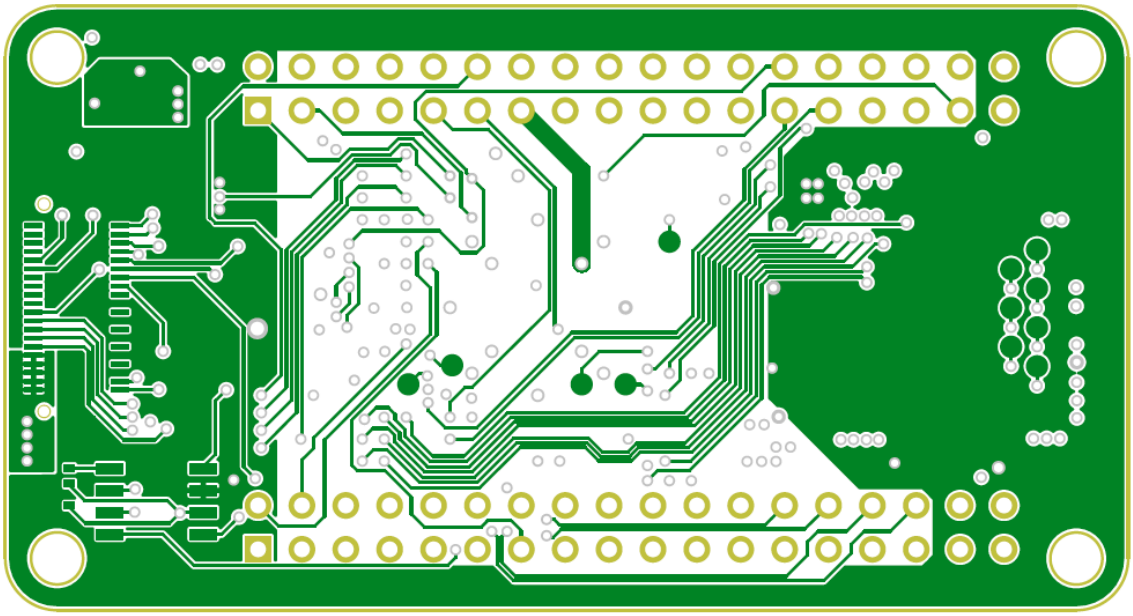
G.5 Cooper layer 4: ground



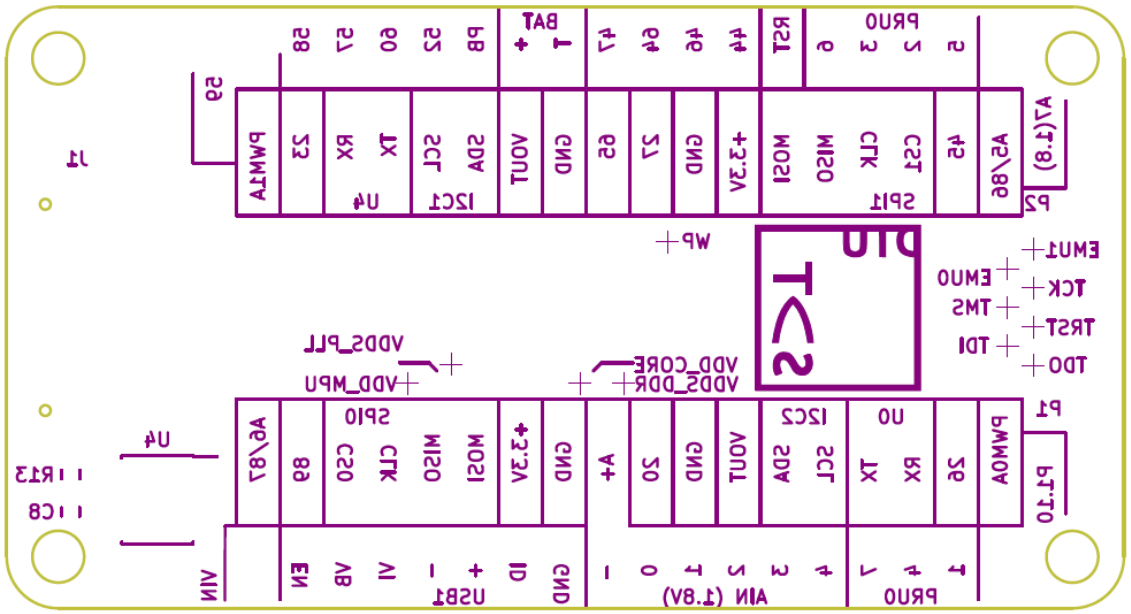
G.6 Cooper layer 5: ground



G.7 Cooper layer 6: bottom

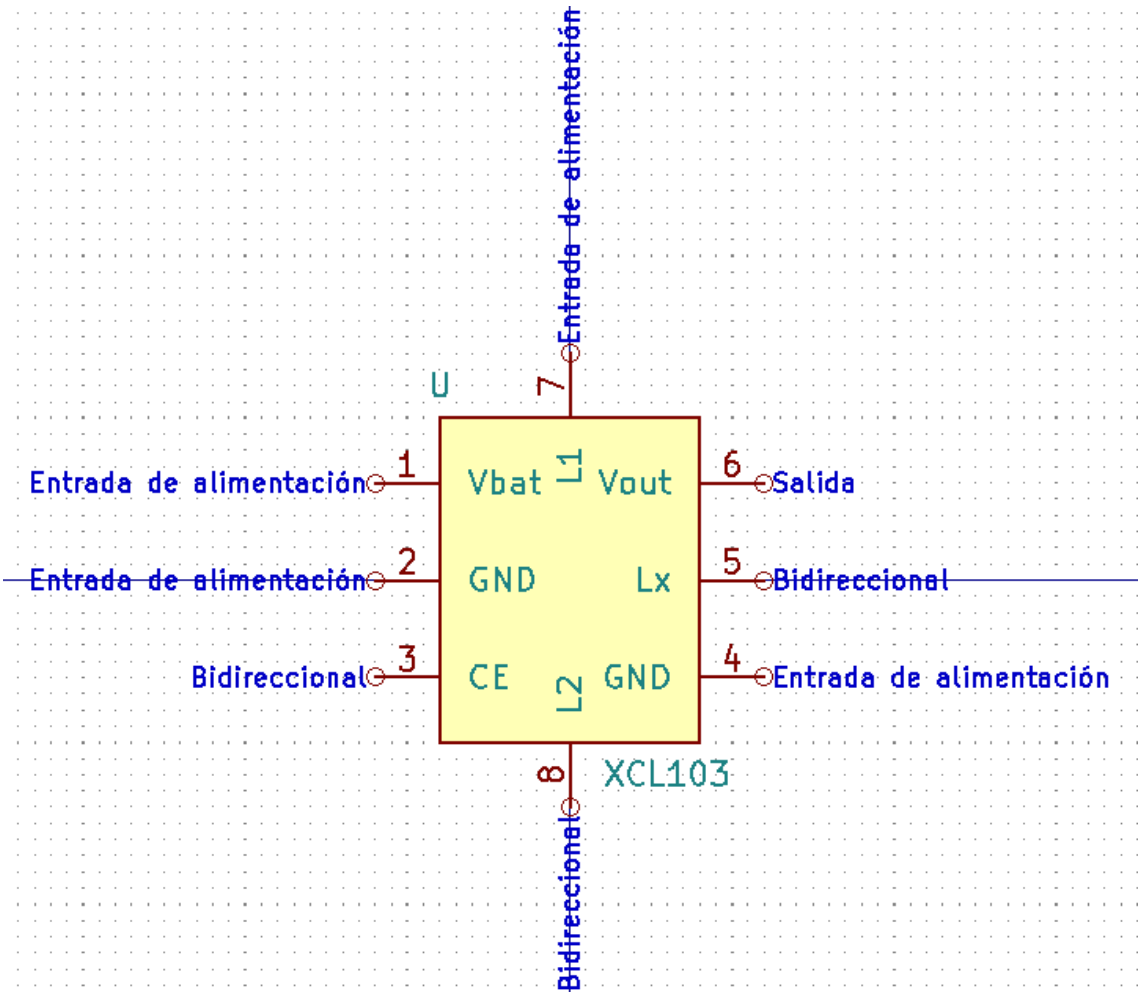


G.8 Back silk screen



Appendix H

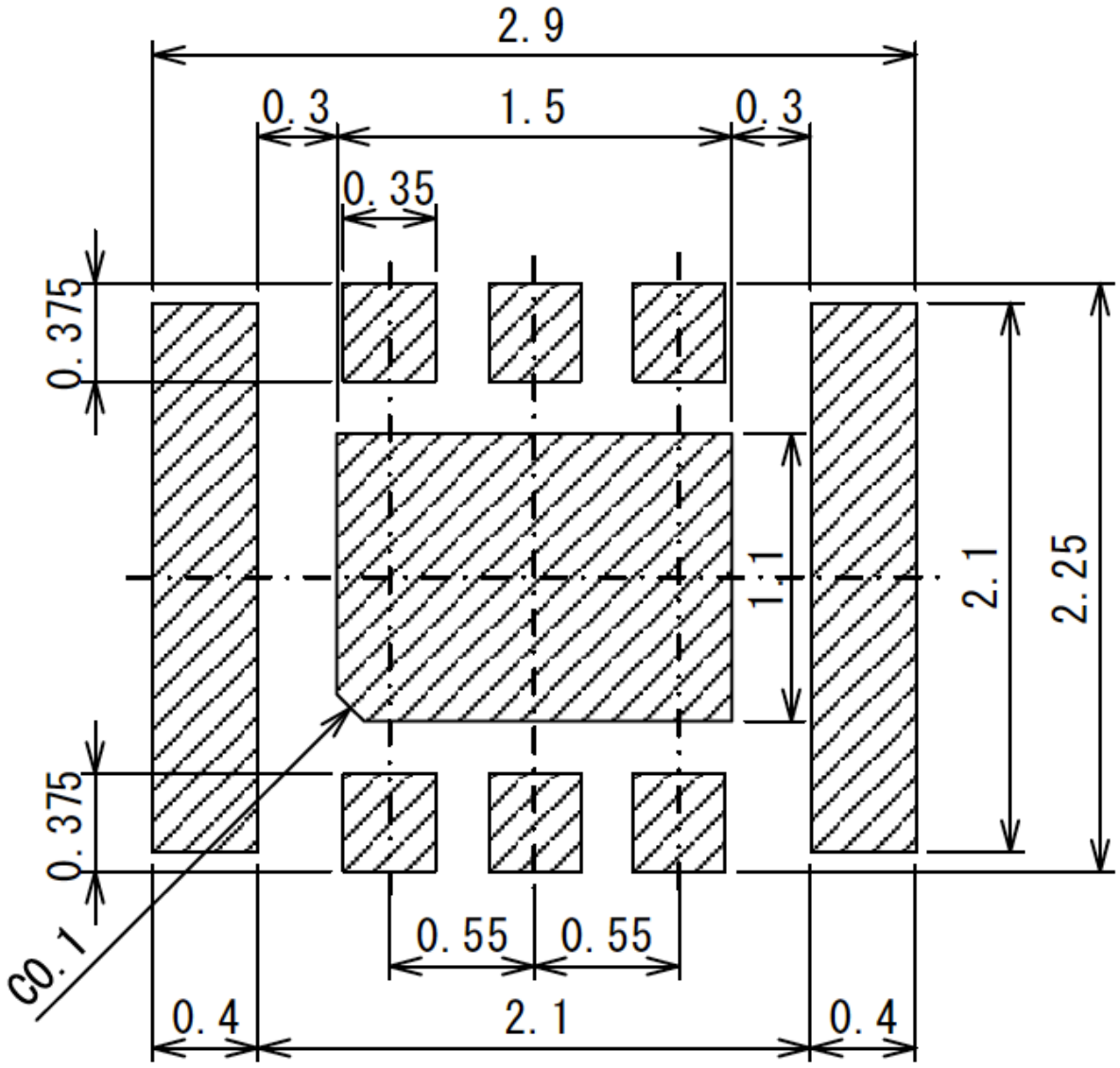
XCL103D step-up converter symbol design

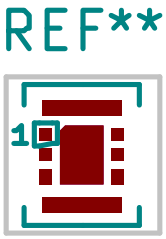


Número	Nombre	Electrical Type	Graphic Style	Orientación	Posición X	Posición Y
1	Vbat	Entrada de alimentación	Línea	Derecha	-0,325 in	0,150 in
2	GND	Entrada de alimentación	Línea	Derecha	-0,325 in	0,000 in
3	CE	Bidireccional	Línea	Derecha	-0,325 in	-0,150 in
4	GND	Entrada de alimentación	Línea	Izquierda	0,325 in	-0,150 in
5	Lx	Bidireccional	Línea	Izquierda	0,325 in	0,000 in
6	Vout	Salida	Línea	Izquierda	0,325 in	0,150 in
7	L1	Entrada de alimentación	Línea	Abajo	0,000 in	0,375 in
8	L2	Bidireccional	Línea	Arriba	0,000 in	-0,375 in

Appendix I

XCL103D step-up converter footprint design


2.9
0.3
1.5
0.3
0.35
0.375
1.1
2.1
2.25
0.375
C0.1
0.55
0.55
0.4
2.1
0.4



Converter_DCDC_Stepup_XCL103_2x2.5mm

Appendix J

Booting Linux for the first time

This section explains the process of getting a printed circuit board (PCB) to boot for the first time after manufacturing, and it is based on the application note *OSD335x EEPROM During Boot* from (Octavo Systems, 2015).

When booting a board for the first time there are several challenges involved, but one that is common to all designs is how to properly load and configure software drivers during boot. It is important for the software running on the new design to recognize the set of peripherals and components used on the PCB so that the drivers can be correctly loaded and configured. The BeagleBoard Linux image used for the OSD335x identifies designs by a code, a board ID, that is stored within an EEPROM attached to the I2C0 bus. This board ID is then used within U-Boot to configure the system, as explained in Section 4.6.2 of Chapter 4. However, all EEPROMs are initially unprogrammed when placed on a board, i.e the board ID is blank. This way, when U-Boot first reads the board ID, it finds a value that does not match any board ID causing the boot process to pause. Therefore, the Linux kernel is never booted.

To avoid this issue, there are several steps that should be followed when booting a board for the first time.

J.1 Step 1: Recognizing a blank board ID

In this first step, U-Boot is modified to ignore the board ID information within the EEPROM, so that the Linux kernel can be booted normally. For this, U-Boot is updated to recognize the board ID value as blank. In order to do this, three patches must be downloaded and applied to the U-Boot code base. Two of these patches are part of the U-Boot build process while the third one configures U-Boot to recognize the unprogrammed

EEPROM value as a blank board. Once the three patches are applied, the Linux kernel can be booted.

However, modifying U-Boot so that it ignores the board ID is a short-term solution since U-Boot will initialize the software drivers that belong to a BeagleBone and not the ones belonging to a PocketBeagle. This way, after booting, U-Boot complains about not finding certain components that can be found in a BeagleBone but not in a PocketBeagle, such as an eMMC flash memory. For this reason, Step 2 is necessary.

J.2 Step 2: Reprogram the EEPROM

The second step is to program the EEPROM to have the correct board ID information for the given board. For this, once U-Boot has booted successfully, the I2C command is used to program the EEPROM with the appropriate values, that are hexadecimal ASCII values. In this case, the name and version fields of the EEPROM data structure are written with the same values found in the PocketBeagle EEPROM, so that U-Boot can initialize the proper software drivers.

At this point, the board has been successfully programmed so that it can now boot the Linux image.

Appendix K

MATLAB code for TID plots

```
clc;
clear all;
close all;

%%%%% LOAD THE DATA FROM THE EXCEL SHEET %%%%%
data = xlsread('/Users/blancaalejo/Dropbox/TFM 2019/3. Proyecto/7. Test/Radiation.xlsx');
VDD_DDR = data(:,1);
VDD_PLL = data(:,2);
STACK_V = data(:,3);
STACK_A = data(:,4);
STEPUP_5V = data(:,5);
R = 100/6;
P_IN = times(STACK_V, STACK_A);
P_OUT = times(STEPUP_5V, STEPUP_5V)./R;
STEPUP_EFF = P_OUT ./ P_IN * 100;
TID = linspace(0,8,length(VDD_DDR));

%%%%% VDD_DDR VS. DOSE GRAPH %%%%%
fig = figure;
figure(1)
plot(TID, VDD_DDR,'b', 'LineWidth',2), grid on, hold on
ylabel('Voltage [V]')
xlabel('Total Ionizing Dose [krad]')
title('PMIC VDD\_DDR voltage')
set(findall(fig,'-property','FontSize'),'FontSize',20)
```

```
%%%%% VDD_PLL VS. DOSE GRAPH %%%%%
fig = figure;
figure(2)
plot(TID, VDD_PLL, 'r', 'LineWidth',2), grid on, hold on
ylabel('Voltage [V]')
xlabel('Total Ionizing Dose [krad]', 'FontSize', 20)
title('PMIC VDD\_PLL voltage')
set(findall(fig,'-property','FontSize'),'FontSize',20)

%%%%% STEP-UP CONVERTER EFFICIENCY VS. DOSE GRAPH %%%%%
fig = figure;
figure(3)
plot(TID, STEPUP_EFF, 'g', 'LineWidth',2), grid on, hold on
ylabel('Effciciency [%]')
xlabel('Total Ionizing Dose [krad]', 'FontSize', 20)
title('XCL103D step-up converter efficiency')
set(findall(fig,'-property','FontSize'),'FontSize',20)
```