COMILLAS
UNIVERSIDAD PONTIFICIA
ICAI ICADE CIHS

Syllabus
2022 - 2023

GENERAL INFORMATION

Data of the subject	
Subject name	Digital Systems I
Subject code	DEA-GITT-214
Mainprogram	Bachelor's Degree in Engineering in Telecommunication Technologies
Involved programs	Grado en Ingeniería en Tecnologías de Telecomunicación [Second year] Grado en Ingeniería en Tecnologías de Telecom. y Grado en Análisis de Negocios/Business Analytics [Second year] Grado en Ingeniería en Tecnologías de Telecom. y Grado en Análisis de Negocios/Business Analytics [Second year]
Level	Reglada Grado Europeo
Quarter	Semestral
Credits	6,0 ECTS
Type	Compulsory
Department	Department of Electronics, Control and Communications
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Office hours	Request an appointment by email

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DESCRIPTION OF THE SUBJECT

Contextualization of the subject

Course contents

Contents

Theory

Introduction

1. Introduction to digital technique.
2. Bits and logic levels.
3. Technologies to implement digital circuits
4. Design levels.

Boolean algebra

1. Definitions and theorems of boolean algebra.
2. Non-basic logic functions.
3. Normal forms of a boolean function.
4. Simplification using Karnaugh diagrams.

Number systems

1. Positional number systems.
2. Base Conversion.
3. Range of unsigned numbers.
4. Hexadecimal and octal systems.
5. Mathematical operations with binary numbers.
6. Representation of integers.
7. Range in signed numbers.
8. Mathematical operations with signed numbers.
9. Other binary codes.

Introduction to VHDL

1. Design flow.
2. File structure.
3. Examples.

4. Data types, constants and operators.
5. Concurrent sentences.

Arithmetic Circuits

1. One-bit adder.
2. n-bit adder.
3. n-bit subtracter.
4. n-bit Adder/Subtracter.
5. Multipliers.
6. BCD Adder.

Combinational Blocks

1. Multiplexers.
2. Demultiplexers.
3. Encoders.
4. Decoders.
5. Comparators.

Sequential circuits. Fundamentals

1. Introduction.
2. Basic concepts.
3. Bistable.

Digital Circuits Timing

1. Introduction.
2. Timing hazards.
3. Synchronous Design.
4. Technological parameters of flip-flops.
5. Synchronous design and clock period.
6. Clock skew and clock distribution.
7. Synchronization of asynchronous inputs.

Finite State Machines

1. Nomenclature.
2. Design of finite state machines.
3. Description in VHDL.
4. Sequence detector.
5. Sequence detector using edge detectors.

Registers

1. Introduction.
2. Parallel input/output registers.
3. Shift Registers.

Counters

1. Ascending binary counter.
2. Descending binary counter.
3. Up/down counter.
4. Counters with enable.
5. M module counters.
6. Cascade counters connection.
7. Counters with parallel load.
8. Arbitrary Sequence Counters.

Complex system design: data path + control

1. Introduction.
2. Control of a parking barrier.
3. Bull quality control.
4. Binary to BCD converter.
5. Interconnection of devices through SPI.

Laboratory

Lab 1: Introduction to logic gates and the digital oscilloscope
Lab 2: Introduction to schematic capture and compilation with Quartus II.
Lab 3: Introduction to simulation and physical implementation with Quartus II.
Lab 4: Combinational circuits. Design with VHDL.
Lab 5: Arithmetic circuits. 5 bit adder.
Lab 6: Arithmetic circuits. 5 bit multiplier.
Lab 7: Arithmetic circuits. 5 bit ALU.
Lab 8: Introduction to flip-flops.
Lab 9: Electronic lock.
Lab 10: Parking control.
Lab 11: Timer for a microwave oven.

EVALUATION AND CRITERIA

Evaluation activities	Evaluation criteria	Weight
• Final Exam	• Understanding of concepts. • Application of concepts to the resolution of practical problems. • Analysis and interpretation of the results obtained in solving problems. • Presentation and written communication.	42 %
	• Understanding of concepts. • Application of concepts to the resolution of	

• Short controls (in class). • Mid-semester exam.	practical problems. • Analysis and interpretation of the results obtained in solving problems. • Presentation and written communication.	18 %
• Lab Tests. • Working of the circuits implemented in the lab. • Documentation of the results. • Final laboratory exam.	• Understanding of concepts. • Application of concepts to the resolution of practical problems and to carrying out practices in the laboratory. • Handling of laboratory tools. • Analysis and interpretation of the results obtained in the laboratory. • Group work capacity. • Presentation and written communication.	40 %

Grading

Final grade

The evaluation of the student consists of two parts: theory and laboratory.

To evaluate the theory, the following tests will be carried out:

- Short exercises in class (10 minutes). The objective of these exercises is that the student knows what he knows (and what he doesn't know). The average of these exercises gives the class grade n_c.
- A mid-term exam, from which the grade n_i will be obtained.
- A final exam that will include all the material taught in the course. From this exam the grade n_e will be obtained.

To obtain the final mark of the theory, a weighted average of the previous marks will be obtained according to the following formula:

$n\_t = n\_i * 0.2 + n\_e * 0.7 + n\_c * 0.1$

The laboratory evaluation is made from:

- The previous work of the practice, which is evaluated by means of a 10-minute test at the beginning of the lab. From the mean of all test the grade n_t is obtained.
- Documentation and operation of the designed circuits. From the average of all the practices, the note n_p is obtained.
- The final laboratory exam, n_ex

The final laboratory grade is obtained from the weighted average of the previous grades, as long as the final exam grade of laboratory is greater than or equal to four, according to the following formula:

$n\_l = n\_ex * 0.5 + n\_t * 0.3 + n\_p * 0.2$

If the grade of the final laboratory exam is less than four, then the final grade of the laboratory will be the grade of said exam:

$n\_l = n\_ex$

It is mandatory to deliver all practices. If any of them has not been delivered, the laboratory grade will be a zero.

To pass the course, the marks n t and n l must be greater than 5. If this condition is met, the final mark for the course is calculated:

n_end = n_t * 0.6 + n_l * 0.4
Otherwise, the final grade will be the lower of the two grades n_t and n_l .

Extraordinary evaluation

The extraordinary call is considered as a second opportunity in case the student has failed one or both
parts of which the subject is composed.
If the student has failed the theory, she will take the theoretical exam n jt and the new theory mark will be obtained according to the formula:
nt = njt * 0.8 + n i * 0.1 + n c * 0.1
If the student has failed the laboratory, she will take the laboratory exam n jl and the new laboratory grade will be obtained according to the
formula:
nl = njl * 0.65 + nt * 0.15 + np * 0.2
As long as the laboratory test grade is greater than or equal to four. Otherwise, the laboratory grade will be the grade of
said test:
nl = njl
The final mark for the extraordinary call will be obtained in the same way as for the ordinary call: if the marks n t and n l are greater than 5, the final mark of the subject is calculated:
n end = n t * 0.6 + n l * 0.4
Otherwise, the final grade will be the lower of the two grades n t and n l .

Attendance Rules

Class attendance is mandatory, according to the Academic Regulations of ICAI. The attendance requirements will be applied independently for the theory and laboratory sessions:

In the case of theory sessions, failure to comply with this rule may prevent taking the exam in the ordinary call.

In the case of laboratory sessions, failure to comply with this rule may prevent them from taking the exam in the ordinary and extraordinary calls. In any case, unjustified absences from laboratory sessions will be penalized in the evaluation.

BIBLIOGRAPHY AND RESOURCES

Basic References

- José Daniel Muñoz Frías. Introducción a los sistemas digitales. Un enfoque usando lenguajes de descripción de hardware. (2017)

CRONOGRAMA Sistemas Digitales I. 2º GITT

PROGRAMA DE TEORIA	S1	S2	S2	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14
Tema 1. Introducción.														
Tema 2. Álgebra de Boole.														
Tema 3. Sistemas de numeración.														
Tema 4. Introducción al lenguaje VHDL														
Tema 5. Circuitos aritméticos														
Tema 6. Bloques combinacionales														
Tema 7. Circuitos secuenciales. Fundamentos														
Tema 8. Temporización de circuitos digitales														
Tema 8. Máquinas de estados finitos														
Tema 9. Registros														
Tema 10. Contadores														
Tema 11. Diseño de sistemas complejos: ruta de datos y control														

Nota. El cronograma se da por semanas de clase.

Fechas clave teoría

En amarillo	Controles de clase
En Naranja	Intercuatrimestrales

PROGRAMA DE LABORATORIO	S1	S2	S2	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14
P1. Introducción a las puertas lógicas integradas y al osciloscopio digital.														
P2. Introducción a la captura de esquemas y la compilación con Quartus II.														
P3. Introducción a la simulación y a la implantación física con Quartus II.														
P4. Circuitos combinacionales. Diseño con VHDL.														
P5. Circuitos aritméticos. Sumador de 5 bits.														
P6. Circuitos aritméticos. Multiplicador de 5 bits.														
P7. Circuitos aritméticos. ALU de 5 bits.														
P8. Introducción a los biestables.														
P9. Cerradura electrónica.														
P10. Control de aparcamiento.														
P11. Temporizador para horno microondas.														

Fechas clave laboratorio

En Azul	Se da teoría en lugar de laboratorio
En Naranja	Intercuatrimestrales