Syllabus
2023 - 2024

GENERAL INFORMATION

Data of the subject	
Subject name	Digital Systems II
Subject code	DEA-GITT-224
Mainprogram	Bachelor's Degree in Engineering in Telecommunication Technologies
Involved programs	Grado en Ingeniería en Tecnologías de Telecomunicación [Second year] Grado en Ingeniería en Tecnologías de Telecom. y Grado en Análisis de Negocios/Business Analytics [Second year]
Level	Reglada Grado Europeo
Quarter	Semestral
Credits	6,0 ECTS
Type	Obligatoria (Grado)
Department	Department of Electronics, Control and Communications
Coordinator	José Daniel Muñoz Frías
Office hours	Request an appointment by email

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DESCRIPTION OF THE SUBJECT

Contextualization of the subject

Prerequisites

A solid basic knowledge of digital circuits is needed for this course. The student should be confident with:

- Combinational circuits.
- Sequential circuits.
- State machines.
- VHDL.

Course contents

Contents

theory

Introduction to digital systems verification.

1. Introduction.
2. Verification in the design process.
3. Testbench in VHDL.
4. Procedures and functions in VHDL.
5. File access in VHDL.
6. Verification in the manufacturing process.

Integrated memory

1. Introduction to integrated memory.
2. Classification and technological characteristics.
3. RAM memory.
4. ROM memory.
5. Memory applications.
6. Description of memories in VHDL.
7. Memory geometry.

Introduction to computer architecture

1. Introduction.
2. Von Newman's architecture.
3. Instruction coding.

ICAI-RISC-V programming

1. Introduction.
2. Arithmetic operations.
3. Logic and shift Instructions.
4. Memory Access.
5. Decision making.
6. Loops.
7. Function calls.

RISC-V architecture

1. Introduction.
2. Base architecture and extensions.
3. The RV32I architecture.

ICAI–RISC–V organization

1. Introduction.
2. ICAI–RISC–V data path.
3. Execution stages of an instruction.
4. Control circuit.

Systems on Chip

1. Introduction.
2. The memory map.
3. Separation between processor and RAM.
4. Parallel input and output ports design.
5. Connecting peripherals to the ICAI–RISC–V.
6. Standard buses for SoCs.
7. Bridge circuit between the ICAI–RISC–V and the APB2 bus.
8. Modifications in the ICAI–RISC–V to connect the APB2 bus.

Exceptions and interrups. The Zicsr extension

1. Introduction.
2. Processor privilege levels.
3. Control and status registers.
4. CSR instructions.
5. Interrupt processing.
6. Writing interrupt service routines.

Laboratory

- LAB 1- Serial transmitter.
- LAB 2- Serial receiver.
- LAB 3- Design of a multiplexed display system.
- LAB 4- Design of a 32-bit ALU for the ICAI-RISC-V processor.
- LAB 5- Implementation of the ICAI-RISC-V processor.
- LAB 6- Final design. System on a chip based on the ICAI-RISC-V.

EVALUATION AND CRITERIA

Evaluation activities	Evaluation criteria	Weight
Mid-grade and final exams	• Understanding of concepts. • Application of concepts to the resolution of practical problems. • Analysis and interpretation of the results obtained in the resolution of problems. • Presentation and written communication.	54
Short tests	• Understanding of concepts. • Application of concepts to the resolution of practical problems. • Analysis and interpretation of the results obtained in the resolution of problems. • Presentation and written communication.	6
Lab work	• Understanding of concepts. • Application of concepts to problem solving and laboratory work. • Analysis and interpretation of the results obtained in laboratory work. • Presentation and written communication. • Handling of laboratory tools. • Team work.	40

Grading

Final Grade

The evaluation of the student consists of two parts: theory and laboratory.

To evaluate the theory, the following tests will be carried out:

- Short exercises in class (10 minutes). The objective of these exercises is that the student knows what he knows (and what he doesn't know). The average of these exercises gives the class grade n_c.
- A mid-term exam, from which the grade n_i will be obtained.

- A final exam that will include all the material taught in the course. From this exam the grade n_e will be obtained.

To obtain the final mark of the theory, a weighted average of the previous marks will be obtained according to the following formula:

n_t = n_i * 0.2 + n_e * 0.7 + n_c * 0.1

The laboratory evaluation is made from:

- The previous work of the lab, which is evaluated by means of a 10-minute test at the beginning of the lab.From the average of all test the grade n_t is obtained.
- Documentation and operation of the designed circuits. From the average of all the lab works, the note n_p is obtained.
- The final laboratory exam, n_ex

The final laboratory grade is obtained from the weighted average of the previous grades, as long as the final exam grade of laboratory is greater than or equal to four, according to the following formula:

n_l = n_ex * 0.5 + n_t * 0.3 + n_p * 0.2

If the grade of the final laboratory exam is less than four, then the final grade of the laboratory will be the grade of said exam:

n_l = n_ex

It is mandatory to deliver all practices. If any of them has not been delivered, the laboratory grade will be a zero.

To pass the course, the marks n_t and n_l must be greater than 5. If this condition is met, the final mark for the course is calculated:

n_end = n_t * 0.6 + n_l * 0.4

Otherwise, the final grade will be the lower of the two grades n_t and n_l .

Extraordinary evaluation

The extraordinary evaluation is considered a second opportunity in case the student has failed one or both parts of which the subject is composed.

If the student has failed the theory, she will take the theoretical exam n_jt and the new theory mark will be obtained according to the formula:

nt = n_jt * 0.8 + n_i * 0.1 + n_c * 0.1

If the student has failed the laboratory, she will take the laboratory exam n_jl and the new laboratory grade will be obtained according to the formula:

nl = n_jl * 0.65 + n_t * 0.15 + n_p * 0.2

As long as the laboratory test grade is greater than or equal to four. Otherwise, the laboratory grade will be the grade of said test: nl = n_jl

The final mark for the extraordinary call will be obtained in the same way as for the ordinary call: if the marks n_t and n_l are greater than 5, the final mark of the subject is calculated:

n_end = n_t * 0.6 + n_l * 0.4

Otherwise, the final grade will be the lower of the two grades n_t and n_l

Attendance Rules

Class attendance is mandatory, according to the Academic Regulations of the Higher Technical School of Engineering (ICAI). the requirements of attendance will be applied independently for theory and laboratory sessions:

- In the case of theory sessions, failure to comply with this rule may prevent them from taking the exam in the ordinary period.
- In the case of laboratory sessions, failure to comply with this rule may prevent you from taking the exam both in the normal and re-sit period.
- In any case, unjustified absences from laboratory sessions will be penalized in the evaluation

BIBLIOGRAPHY AND RESOURCES

Basic References

- Introducción a los sistemas digitales. Un enfoque usando lenguajes de descripción de hardware. José Daniel Muñoz Frías.
- Apuntes de la asignatura Sistemas Digitales II. José Daniel Muñoz Frías.

Cronograma orientativo Sistemas Digitales II. 2º GITT

PROGRAMA DE TEORIA	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	SS	S14	S15
Tema 1. Verificación de circuitos digitales																
Tema 2. Memorias																
Tema 3. Introducción a la arquitectura de ordenadores																
Tema 4. Programación del ICAI-RISC-V																
Tema 5. Arquitectura RISC-V																
Tema 6. La organización ICAI-RISC-V																
Tema 7. Sistemas en un chip																
Tema 8. Circuitos aritméticos																

Nota. El cronograma se da por semanas de clase.

Fechas clave

En amarillo	Controles de clase
En Naranja	Intercuatrimestrales
En Gris	Vacaciones semana santa

PROGRAMA DE LABORATORIO	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	SS	S14	S15
P1. Receptor serie RS-232																
P2. Trasmisor serie RS-232																
P3. Display alfanumérico multiplexado																
P4. Diseño de una ALU de 32 bits para el procesador ICAI-RISC-V																
P5. Implementación del microprocesador ICAI-RISC-V																
P6. Diseño final. Sistema en un chip basado en el ICAI-RISC-V																

Fechas clave laboratorio

En Gris	Festivos
En Naranja	Intercuatrimestrales
Entrega de la propuesta de diseño final	Semana 11
Entrega final del diseño	Último día de laboratorio
Entrega del informe del diseño final	Último día de clase